DATA ACQUISITION HANDBOOK

NATIONAL SEMICONDUCTOR

DATA ACQUISITION HANDBOOK

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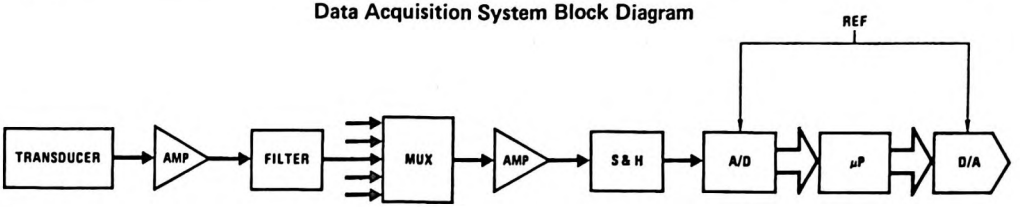
Introduction

It's a rapidly changing world — and a moment's reflection reminds us that, principally, it is *electronics* that is causing the changes in our world. Electronic systems are changing too, from all-analog and all-digital types, to a world where analog and digital disciplines co-exist to make inexpensive but powerful systems and products that impact even our daily lives. This Handbook is dedicated to the engineers who design the data acquisition and control systems that will play a major role in shaping and improving the future.

Data Acquisition System Block Diagram

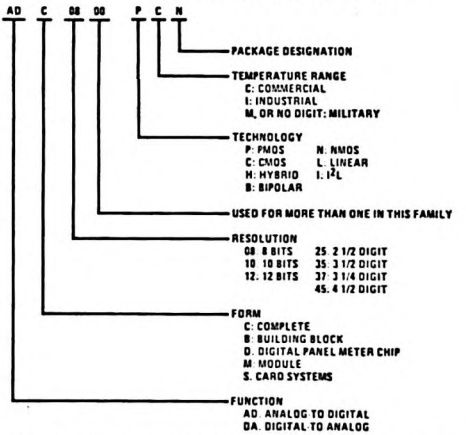


National Semiconductor brings to the marketplace a unique combination of qualifications to supply the sophisticated components required by Data Acquisition and Control systems — high technology devices, mass produced by one of the world's largest semiconductor companies. We have committed to design and source all the building blocks required from transducer to processor — this handbook is evidence of our total systems approach. The products detailed in this book include those devices in the direct analog signal path before (and after) the digital processor; devices are fabricated using many technologies including BI-FET™, linear bipolar, CMOS, CMOS with trimmed thin film, I^2L, laser trimmed thick and thin film hybrid and other state-of-the-art processes. Microprocessor, Linear, Discrete, and other functions are covered by their respective databooks and are not duplicated herein.

Reliability — National manufactures components to exacting quality and reliability standards. Most of the devices included offer extended temperature range performance versions and are built to conform with the requirements of MIL-M-38510 and can be ordered with extra reliability screening including MIL-STD-883 Level A and B processing. National's A+ and B+ industrial reliability programs can be specified for standard and industrial temperature range devices. Consult your representative for processing details and availability of these cost-effective programs.

Sales and Technical Assistance — All National devices are available through our extensive network of local distributors. Technical assistance in selecting and applying devices may be obtained by contacting the nearest National representative or sales office or by contacting the factory.

Converter Products Part Numbering System



Future Products — This handbook contains only devices in production as of July, 1978. As this book goes to press, development continues on many advanced Data Acquisition/Conversion products — contact your distributor or representative for information concerning new product introductions.

For information on National's part numbering system for non-converter devices, please consult the latest OEM price list.

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Section 1

Selection Guides

1

RESOLUTION (BITS)	NATIONAL PART NUMBER	ALTERNATE SOURCE PART NUMBER	LINEARITY @ 25°C (MAX) (%)	INTERNAL REFERENCE	OUTPUT OP AMP	SUPPLIES (V)	TEMPERATURE RANGES AVAILABLE (°C)	COMMENTS
D/A CONVERTER								
8	DAC0802	DAC-08A, DAC-08H	0.1			±5 to ±15	0 to +70, −55 to +125	High Speed Multiplying
8	DAC0800	DAC-08, DAC-08E	0.19			±5 to ±15	0 to +70, −55 to +125	High Speed Multiplying
8	DAC0801	DAC-08C	0.39			±5 to ±15	0 to +70	High Speed Multiplying
8	DAC0806	MC1408-6	0.78			±5 to ±15	0 to +70	Multiplying
8	DAC0807	MC1408-7	0.39			±5 to ±15	0 to +70	Multiplying
8	DAC0808	MC1508-8/MC1408-8	0.19			±5 to ±15	0 to +70, −55 to +125	Multiplying
10	DAC1020	AD7520L/AD7530L	0.05			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
10	DAC1021	AD7520K/AD7530K	0.1			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
10	DAC1022	AD7520J/AD7530J	0.2			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1220	AD7521L/AD7531L	0.05			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1221	AD7521K/AD7531K	0.1			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1222	AD7521J/AD7531J	0.2			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1200		0.012	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1201		0.049	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1285	DAC85 (Binary)	0.012	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1280	DAC80 (Binary)*	0.024	•	•	±15, 5	−25 to +85	Complete DAC
3-Digits	DAC1202		0.01	•	•	±15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1203		0.05	•	•	±15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1286	DAC85 (BCD)	0.05	•	•	±15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1287	DAC80 (BCD)*	0.1	•	•	±15, 5	−25 to +85	Complete BCD DAC

*Note. Minor specification differences

RESOLUTION (BITS)	BASIC TYPE	LINEARITY @ 25°C (MAX) (%)	CONVERSION TIME (TYP)	OUTPUT LOGIC LEVELS	SUPPLIES (V)	TEMPERATURE RANGES AVAILABLE (°C)	COMMENTS
A/D CONVERTER							
8	ADC0800 (MM5357B)	0.8	100 μs	TTL TRI-STATE®	+5, −12	0 to +70, −55 to +125	
8	ADC0808	0.2	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	Includes 8-Channel MUX
8	ADC0809	0.4	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	Includes 8-Channel MUX
8	ADC0816	0.2	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	16-Channel MUX, S and H Port
8	ADC0817	0.4	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	16-Channel MUX, S and H Port
8†	TP3000	†	†	TTL	±12	0 to +70	†Companding Coder-Decoder
12	ADC1210	0.012	100 μs	CMOS	+5 to ±15	−25 to +85, −55 to +125	10-Bit Conversion in 30 μs
12 (10)	ADC1211	0.049	100 μs	CMOS	+5 to ±15	−25 to +85, −55 to +125	
12	LF13300	0.01	N/A	N/A	±15	0 to +70	Dual Slope ADC
	ADB1200	N/A	36 ms	TTL TRI-STATE	+5, −15	0 to +70	12-Bit Logic for LF13300
3 1/2-Digits	ADC3511	0.05	200 ms	TTL TRI-STATE	+5	0 to +70	Integrating μP ADC
3 3/4-Digits	ADC3711	0.05	400 ms	TTL TRI-STATE	+5	0 to +70	Integrating μP ADC
V-F	LM131	0.01	N/A	N/A	+5 to +40	0 to +70, −25 to +85, −55 to +125	Voltage-to-Frequency Converter, 100 kHz Max
DIGITAL VOLTMETER							
3 1/2-Digits	ADD3501	0.05	200 ms	7-Segment LED Drive	+5	0 to +70	3 1/2-Digit LED DPM
3 3/4-Digits	ADD3701	0.05	400 ms	7-Segment LED Drive	+5	0 to +70	3 3/4-Digit LED DPM
4 1/2-Digits	LF13300	0.005	N/A	N/A	±15	0 to +70	Dual Slope ADC
	ADB4511	N/A	500 ms	7-Segment LED Drive	+5	0 to +70	4 1/2-Digit DPM Logic for LF13300

REVERSE BREAKDOWN VOLTAGE V_R at I_R	DEVICE	VOLTAGE TOLERANCE MAX, T_A = 25°C	VOLTAGE TEMPERATURE DRIFT – ppm/°C MAX or mV MAX CHANGE OVER TEMPERATURE RANGE		CURRENT RANGE, I_R	DYNAMIC IMPEDANCE
			DRIFT (MAX)	TEMPERATURE RANGE		
1.22	LM113	±5%	100 (typ)	−55°C to +125°C	500 µA to 20 mA	0.3Ω
1.22	LM313	±5%	100 (typ)	0°C to +70°C	500 µA to 20 mA	0.3Ω
1.22	LM113-1	±1%	50 (typ)	−55°C to +125°C	500 µA to 20 mA	0.3Ω
1.22	LM113-2	±2%	50 (typ)	−55°C to +125°C	500 µA to 20 mA	0.3Ω
2.49	LM136	±2%	18 mV	−55°C to +125°C	400 µA to 10 mA	0.2Ω
2.49	LM136A	±1%	18 mV	−55°C to +125°C	400 µA to 10 mA	0.2Ω
2.49	LM236	±2%	9 mV	−25°C to +85°C	400 µA to 10 mA	0.2Ω
2.49	LM236A	±1%	9 mV	−25°C to +85°C	400 µA to 10 mA	0.2Ω
2.49	LM336	±4%	6 mV	0°C to +70°C	400 µA to 10 mA	0.2Ω
2.49	LM336B	±2%	6 mV	0°C to +70°C	400 µA to 10 mA	0.2Ω
5.0	LM136-5.0	±2%	36 mV	−55°C to +125°C	400 µA to 10 mA	0.2Ω
5.0	LM136A-5.0	±1%	36 mV	−55°C to +125°C	400 µA to 10 mA	0.2Ω
5.0	LM236-5.0	±2%	18 mV	−25°C to +85°C	400 µA to 10 mA	0.2Ω
5.0	LM236A-5.0	±1%	18 mV	−25°C to +85°C	400 µA to 10 mA	0.2Ω
5.0	LM336-5.0	±4%	12 mV	0°C to +70°C	400 µA to 10 mA	0.2Ω
5.0	LM336B-5.0	±2%	12 mV	0°C to +70°C	400 µA to 10 mA	0.2Ω
6.90	LM129A	+3%, −2%	10	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM129B	+3%, −2%	20	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM129C	+3%, −2%	50	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM329B	±5%	20	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.90	LM329C	±5%	50	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.90	LM329D	±5%	100	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.95	LM199A	+1%, −2%	0.5	−55°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199A	+1%, −2%	10	85°C to +125°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199	+1%, −2%	1	−55°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199	+1%, −2%	15	85°C to +125°C	0.5 mA to 10 mA	0.5Ω
6.95	LM299A	+1%, −2%	0.5	−25°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM299	+1%, −2%	1	−25°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM399A	±5%	1	0°C to +70°C	0.5 mA to 10 mA	0.5Ω
6.95	LM399	±5%	2	0°C to +70°C	0.5 mA to 10 mA	0.5Ω
6.95	LM3999	±5%	5	0°C to +70°C	0.6 mA to 10 mA	0.6Ω
10.00	LH0070-0	0.1%	20 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω
10.00	LH0070-1	0.1%	10 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω
10.00	LH0070-2	0.05%	4 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω
10.24	LH0071-0	0.1%	20 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω
10.24	LH0071-1	0.1%	10 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω
10.24	LH0071-2	0.05%	4 mV	−25°C to +85°C*	0 mA to 20 mA	0.2Ω

*Devices are specified for operation over entire −55°C to +125°C range.

REVERSE BREAKDOWN VOLTAGE V_R at I_R	DEVICE	VOLTAGE TOLERANCE MAX, T_A = 25°C	VOLTAGE TEMPERATURE DRIFT – ppm/°C MAX or mV MAX CHANGE OVER TEMPERATURE RANGE		CURRENT RANGE, I_R	DYNAMIC IMPEDANCE
			DRIFT (MAX)	TEMPERATURE RANGE		
LOW CURRENT ZENER DIODES						
1.8	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
2.0	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
2.2	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
2.4	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
2.7	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
3.0	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
3.3	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
3.6	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
3.9	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
4.3	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
4.7	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
5.1	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω
5.6	LM103	±10%	–5 mV/°C (typ)	–55°C to +125°C	10 μA to 10 mA	15Ω

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
Dual SPST					
10	±10	AH0141/DG141	TTL	−18, 12	0.8/1.1µs
30	±10	AH0133/DG133	TTL	−18, 12	0.5/0.9µs
80	±10	AH0134/DG134	TTL	−18, 12	0.5/0.9µs
15	±7.5	AH0151/DG151	TTL	±15	0.8/1.1µs
50	±7.5	AH0152/DG152	TTL	±15	0.5/0.9µs
*30	±7.5	AM181/DG181	TTL	±15, 5	180/150 ns
*75	±10	AM182/DG182	TTL	±15, 5	300/150 ns
Triple SPST					
*100	15 mA	AH5015	15V TTL		150/300 ns
*150	5 mA	AH5016	TTL		150/300 ns
Quad SPST					
200-600	±10	AH0015	TTL	−20, 10, 5	100/400 ns
*200	±10	LF11201	TTL	±15	90/500 ns
*200	±10	LF11202	TTL	±15	90/500 ns
*200	±10	LF11331	TTL	±15	90/500 ns
*200	±10	LF11332	TTL	±15	90/500 ns
*200	±10	LF11333	TTL	±15	90/500 ns
*250	±10	LF13201	TTL	±15	90/500 ns
*250	±10	LF13202	TTL	±15	90/500 ns
*250	±10	LF13331	TTL	±15	90/500 ns
*250	±10	LF13332	TTL	±15	90/500 ns
*250	±10	LF13333	TTL	±15	90/500 ns
280	±7.5	CD4066	CMOS	±7.5	
850	±7.5	CD4016	CMOS	±7.5	
*100	15 mA	AH5011/AM9711	15V TTL		150/300 ns
*100	10 mA	AM97C11	CMOS		150/300 ns
*150	5 mA	AH5012/AM9712	TTL		150/300 ns
*150	3 mA	AM97C12	CMOS		150/300 ns
*30	±7.5	AM193	TTL	±15, 5	180/150 ns
*75	±10	AM194	TTL	±15, 5	300/150 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
SPDT					
10	±10	AH0146/DG146	TTL	−18, 12	0.8/1.1µs
30	±10	AH0144/DG144	TTL	−18, 12	0.5/0.9µs
80	±10	AH0143/DG143	TTL	−18, 12	0.5/0.9µs
15	±7.5	AH0161/DG161	TTL	±15	0.8/1.1µs
50	±7.5	AH0162/DG162	TTL	±15	0.5/0.9µs
100	±9	AH2114 (Sw. 1) (Sw. 2)	15V TTL	±15	35/600 ns 1.2µs/50 ns
*30	±7.5	AM187/DG187	TTL	±15, 5	180/150 ns
*75	±10	AM188/DG188	TTL	±15, 5	300/150 ns
Dual SPDT					
*30	±7.5	AM190/DG190	TTL	±15, 5	180/150 ns
*75	±10	AM191/DG191	TTL	±15, 5	300/150 ns
Triple SPDT					
280	±7.5	CD4053	CMOS	±7.5	150/150 ns
Dual DPST					
10	±10	AH0140/DG140	TTL	−18, 12	0.8/1.1µs
30	±10	AH0129/DG129	TTL	−18, 12	0.5/0.9µs
80	±10	AH0126/DG126	TTL	−18, 12	0.5/0.9µs
15	±7.5	AH0153/DG153	TTL	±15	0.8/1.1µs
50	±7.5	AH0154/DG154	TTL	±15	0.5/0.9µs
200-600	±10	AH0019	TTL	−20, 10, 5	100/400 ns
*30	±7.5	AM184/DG184	TTL	±15.5	180/150 ns
*75	±10	AM185/DG185	TTL	±15.5	300/150 ns
Dual DPDT					
10	±10	AH0145/DG145	TTL	−18, 12	0.8/1.1µs
30	±10	AH0139/DG139	TTL	−18, 12	0.5/0.9µs
80	±10	AH0142/DG142	TTL	−18, 12	0.5/0.9µs
15	±7.5	AH0163/DG163	TTL	±15	0.8/1.1µs
50	±7.5	AH0164/DG164	TTL	±15	0.5/0.9µs
200-600	±10	AH0014	TTL	−20, 10, 5	350/400 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
MULTIPLEXERS					
3-Channel					
*100	15 mA	AH5013	15V TTL		150/300 ns
*150	5 mA	AH5014	TTL		150/300 ns
4-Channel					
*100	15 mA	AH5009/AM9709	15V TTL		150/300 ns
*100	10 mA	AM97C09	CMOS		150/300 ns
*150	5 mA	AH5010/AM9710	TTL		150/300 ns
*150	3 mA	AM97C10	CMOS		150/300 ns
4-Channel Differential					
280	±7.5	CD4052	CMOS	±7.5	150/150 ns
*350	12,−15	LF11509	TTL	±15	1/0.2µs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
6-Channel					
250-1500	50 mA	AM2009/MM4504/ MM5504	TTL	−15, 5	
8-Channel					
250-400	±5	AM3705	TTL	−15, 5	300/600 ns
*350	12,−15	LF11508	TTL	±15	1/0.2µs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
280	±7.5	CD4051	CMOS	±7.5	150/150 ns

Notes:

R_{ON} max @ T_A = 25°C

V_A/I = maximum voltage or current to be safely switched

Part number = basic number/alternate number (i.e., AM181/DG181). May be ordered by either number.

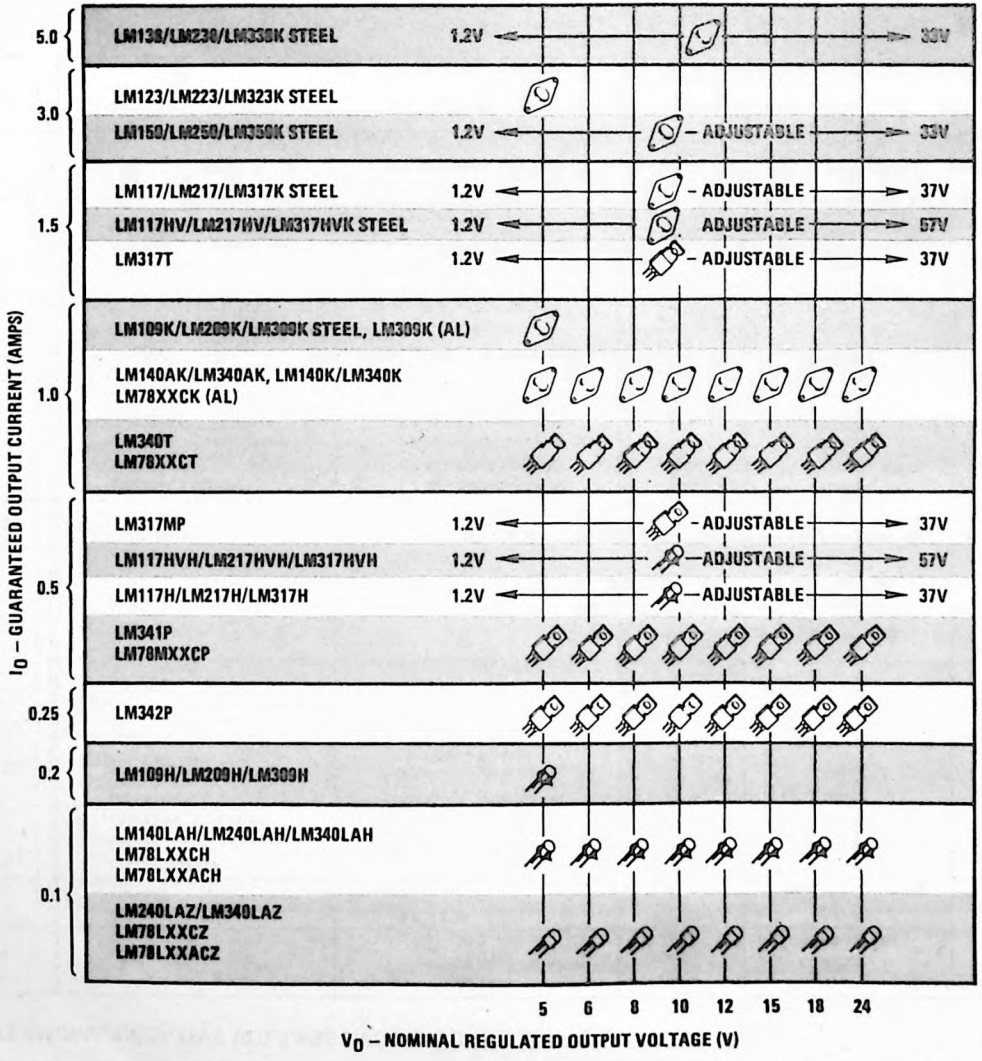
*Preferred devices

3-TERMINAL POSITIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation		V_{IN} (V) Max	Ripple Rejection (dB)
				Line (Note 1) % V_{OUT}/V_{IN}	Load (Note 2) % V_{OUT}		
5	LM138, LM238	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM338	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
3	LM150, LM250	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM350	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM123K, LM223K	5	6	0.01	0.5	20	75
	LM323K	5	4	0.01	0.5	20	75
1.5	LM117, LM217	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HV, LM217HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM317HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM109K, LM209K	5	6	0.004	1.0	35	80
	LM309K	5	4	0.004	1.0	35	80
	LM140K	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	66–80
	LM140AK	5, 6, 8, 10, 12, 15, 18, 24	2	0.002	0.1	35, 40 (24V)	66–80
	LM340	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	66–80
	LM340A	5, 6, 8, 10, 12, 15, 18, 24	2	0.002	0.1	35, 40 (24V)	66–80
	LM78XXC	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	66–80
0.5	LM117H, LM217H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HVH, LM217HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317M	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM341	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	
	LM78MXX	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	
0.25	LM342	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	53–64
0.20	LM109H, LM209H	5	6	0.004	0.4	35	80
	LM309H	5	4	0.004	0.4	35	80
0.10	LM140L, LM240L	5, 6, 8, 10, 12, 15, 18, 24	2	0.02	0.25	35, 40 (24V)	48–62
	LM340L	5, 6, 8, 10, 12, 15, 18, 24	2	0.02	0.25	35, 40 (24V)	48–62
	LM78LXXA	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.25	35, 40 (24V)	45–60

Note 1: Line regulation is the change in output voltage for a change in input voltage.

Note 2: Load regulation is the change in output voltage due to a change in load current from no load to full load.

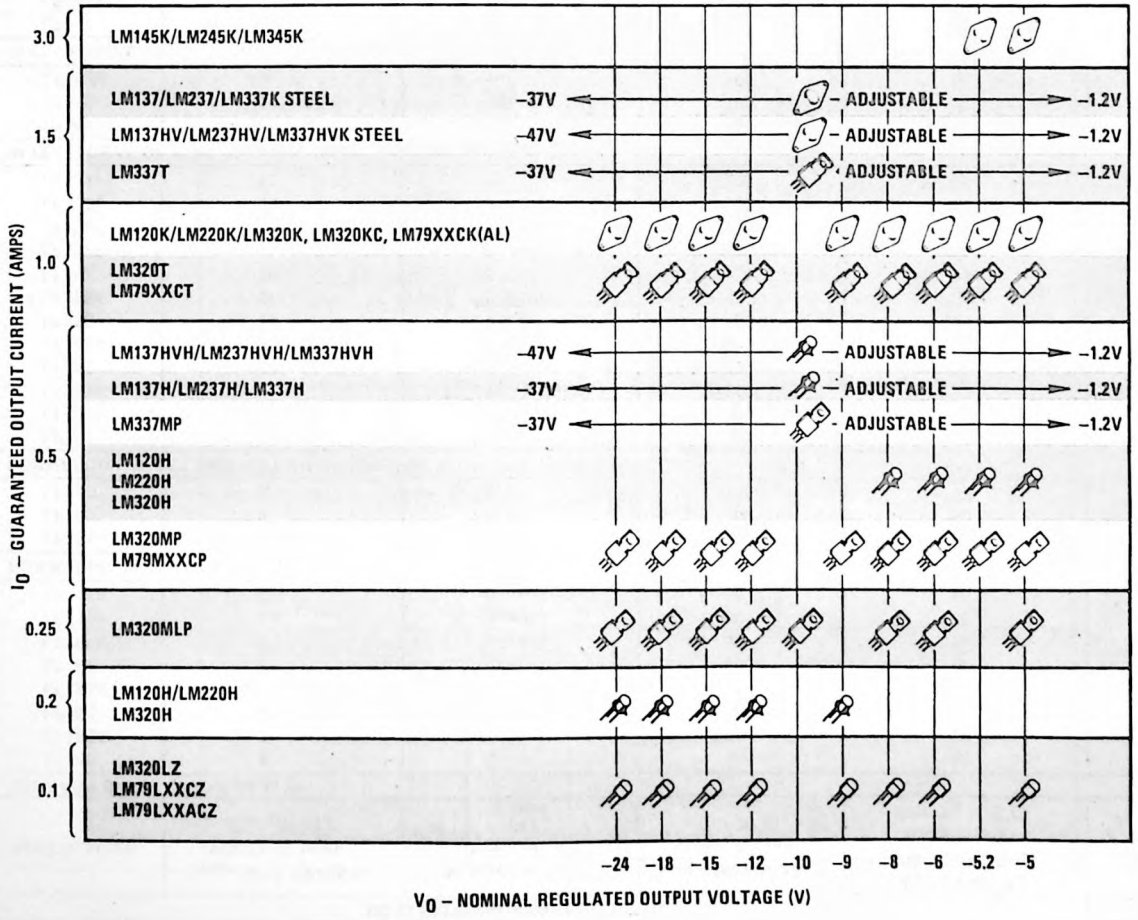


	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-99 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation: Line (Note 1) % V_{OUT}/V_{IN}	Regulation: Load (Note 2) % V_{OUT}	V_{IN} (V) Max	Ripple Rejection (dB)
3	LM145K, LM245K	−5.0, −5.2	2	0.008	0.6	20	68
	LM345K	−5.0, −5.2	4	0.008	0.6	20	68
1.5	LM137, LM237	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HV, LM237HV	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HV	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM120K, LM220K	−5, −5.2, −6, −8, −9	2	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V)	80
						40 (15V, 18V)	75
						42 (24V)	70
	LM320K	−5, −5.2, −6, −8, −9,	4	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V)	80
						40 (15V, 18V)	75
						42 (24V)	70
	LM320T	−5, −5.2, −6, −8, −9	4	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V, 15V, 18V)	75–80
						40 (24V)	70
	LM79XXC	−5, −5.2, −6, −8, −9	4	0.03	0.4	35, 40 (24V)	66–70
		−12, −15, −18, −24					
0.5	LM137H, LM237H	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337H	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HVH, LM237HVH	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HVH	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM337M	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM120H, LM220H	−5.0, −5.2, −6, −8	2	0.02	0.6	25	64
	LM320H	−5.0, −5.2, −6, −8	4	0.02	0.6	25	64
	LM320M	−5, −5.2, −6, −8	4	0.02	0.6	25	60–64
		−9, −12, −15, −18, −24	4			35, (9V, 12V, 15V, 18V)	70–80
						40 (24V)	
	LM79MXX	−5, −6, −8, −12, −15, −24	4	0.03	0.7	35, 40 (24V)	58–60
0.25	LM320ML	−5, −6, −8, −10,	4	0.01	0.5	35, 40 (24V)	50–60
		−12, −15, −18, −24					
0.20	LM120H, LM220H	−9, −12	2	0.02	0.1	35 (9V, 12V)	70–80
	LM320H	−15, −18, −24	4	0.02	0.1	40 (15V, 18V)	
						42 (24V)	
0.10	LM320L	−5, −6, −8, −9	4	0.01	0.5	35, 40 (24V)	60–65
		−12, −15, −18, −24					
	LM79LXXA	−5, −12, −15, −18, −24	4	0.02	0.6	35, 40 (24V)	50–55



	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-99 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

PART NUMBER	DC ELECTRICAL CHARACTERISTICS				AC ELECTRICAL CHARACTERISTICS	
	V_{OS} – MAX OFFSET VOLTAGE (mV) (T_A = 25°C)	$\Delta V_{OS}/\Delta T$ – T.C. OF V_{OS} (µV/°C) TYP	I_B – MAX BIAS CURRENT (pA) (T_J = 25°C)	A_{VOL} LARGE SIGNAL VOLTAGE GAIN (V/mV) MIN (T_A = 25°C)	SR – SLEW RATE (V/µs)	e_n – EQUIV. INPUT NOISE VOLTAGE (nV/√Hz) (Note 2)
MILITARY BI-FET OP AMP (Note 1)						
LF155	5	5	100	50	5	20
LF155A	2	5 (max)	50	50	5	20
LF156	5	5	100	50	12	12
LF156A	2	5 (max)	50	50	12	12
LF157	5	5	100	50	50	12
LF157A	2	5 (max)	50	50	50	12
LFT155	0.5	5 (max)	50	50	5	20
LFT156	0.5	5 (max)	50	50	12	12
INDUSTRIAL BI-FET OP AMP (Note 1)						
LF255	5	5	100	50	5	20
LF256	5	5	100	50	12	12
LF257	5	5	100	50	50	12
COMMERCIAL BI-FET AND BI-FET II OP AMP (Note 3)						
LF351	10	10	200	25	13	16
LF351A	2	10	100	25	13	16
LF351B	5	10	200	25	13	16
LF355	10	5	200	25	5	25
LF355A	2	5 (max)	50	25	5	25
LF356	10	5	200	25	12	15
LF356A	2	5 (max)	50	25	12	15
LF357	10	5	200	25	50	15
LF357A	2	5 (max)	50	25	50	15
LFT355	0.5	5 (max)	50	50	5	20
LFT356	0.5	5 (max)	50	50	12	12
LF13741	15	10	200	25	0.5	37
BI-FET II DUAL OP AMPS (Characteristics for Each Amplifier) (Note 3)						
LF353	10	10	200	25	13	16
LF353A	2	10	100	25	13	16
LF353B	5	10	200	25	13	16
BI-FET II QUAD OP AMPS (Characteristics for Each Amplifier) (Note 3)						
LF347	10	10	200	25	13	16
LF347A	2	10	100	25	13	16
LF347B	5	10	200	25	13	16

SELECTION BY DESIGN PARAMETER

Max Input Offset Voltage (T_A = 25°C)	**0.5 mV** LFT155/LFT156 LFT355/LFT356	**2 mV** LF155A/LF355A LF156A/LF356A LF357A LF351A LF353A LF347A	**5 mV** LF351B LF347B LF353B LF155/LF156/LF157 LF255/LF256/LF257	**10 mV** LF355/LF356/LF357 LF351 LF353 LF347	**15 mV** LF13741
Max Input Bias Current (T_J = 25°C)	**50 pA** LF155A/LF156A/LF157A LFT155/LFT156 LF355A/LF356A/LF357A	**100 pA** LF155/LF156/LF157 LF255/LF256/LF257 LF351A LF353A LF347A	**200 pA** LF355/LF356/LF357 LF351/LF351B LF347/LF347B LF353/LF353B LF13741		
Typ Equivalent Input Noise Voltage per $\sqrt{Hz}$, f = 1000 Hz, R_S = 100Ω	**12 nV or Less** LF156/LF156A LF157/LF157A LFT156 LF256/LF257	**15 nV To 20 nV** LF356 LF356A LF357 LF357A LF351 LF351A LF351B LF347 LF347A LF347B LF353 LF353A LF353B LF155 LF155A LFT155 LF255	**25 nV To 37 nV** LF355 LF355A LF13741		
Typ Slew Rate	**0.5 V/μs** LF13741	**5 V/μs** LF155/LF155A LFT155 LF255 LF355/LF355A LFT355	**12 V/μs** LF156 LF156A LFT156 LF256 LF356 LF356A LFT356	**13 V/μs** LF351 LF351A LF351B LF353 LF353A LF353B LF347 LF347A LF347B	**50 V/μs** LF157 LF157A LF357 LF357A

ADDITIONAL NS PRODUCTS USING BI-FET TECHNOLOGY

- LF111 Comparator
- LF198 Sample and Hold
- LF11201 Series of Analog Switches
- LF11331 Series of Analog Switches
- LF11508 Series of Analog Multiplexers
- LF152 Instrumentation Amplifier
- LF13300 Integrating A/D Building Block

Pressure Transducer Selection Guide

TRANSDUCER ORDERING INFORMATION

LX1 7 03 A FN

STANDARD OPTIONS

B — Backward Gage Version (PX6B, PX7B)
D — High Common-Mode Differential Version (PX7DD)
F — Fluid-Filled Version (PX6F or PX4F)
N — Nylon Package (PX7N)
S — Stainless Steel Package (PX4S)
DF — Combine "D" and "F" Options (PX7DDF)
FN — Combine "F" and "N" Options (PX7FN)
FS — Combine "F" and "S" Options (PX4FS)

PRESSURE TYPE

A — Absolute
D — Differential
G — Gage

PRESSURE RANGE (See Selection Guide)

PACKAGE TYPE

4 — Rugged Cylindrical Plumbed Fitting (PX4 Series)
6 — Hybrid IC for PCB Mounting (PX6 Series)
7 — Rugged Zinc or Nylon Housing with Optional Plumbing (PX7 Series)

DEVICE TYPE

LX1 — Linear Transducer, Pressure

TRANSDUCER SELECTION GUIDE

MAXIMUM RATINGS

Excitation Voltage	30V
Output Current	
Source	20 mA
Sink	10 mA
Transducer Bias Current	20 mA
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−40°C to +105°C
Lead Soldering Temperature (10 seconds)	260°C

TYPICAL CHARACTERISTICS

Output Voltage Sensitivity to Excitation Voltage	0.5%
Output Impedance	<50Ω
Electrical Noise Equivalent ($0 \leq f \leq 1$ kHz)	0.04% Span
Natural Frequency of Sensor Diaphragm	> 50 kHz
Transducer Bias Current	
LX14XXA	7–10 mA
LX16XXA, D, G	11–15 mA

TRANSDUCER SELECTION GUIDE (Continued)

DEVICE TYPE	OPERATING PRESSURE RANGE	MAXIMUM OVER PRESSURE	GUARANTEED SPECIFICATIONS							
			REFERENCE TEMPERATURE = 25°C, V_E = 15 V_{DC}				OPERATING TEMPERATURE RANGE = 0°C to 85°C, REFERENCE PRESSURE = 0 psi†			
			OFFSET CHARACTERISTICS				SPAN CHARACTERISTICS			
			OFFSET CALIBRATION V	TEMP. COEFFICIENT ±psi/°C	REPEATABILITY ±psi	STABILITY ±psi	SENSITIVITY CALIBRATION mV/psi	TEMP. COEFFICIENT ±psi/°C	LINEARITY HYSTERESIS REPEATABILITY ±psi	STABILITY ±psi
ABSOLUTE PRESSURE DEVICES										
LX1601A(F), LX1701A(F)(N)	10 to 20 psia	40 pisa	2.5 ±0.5†	0.0054	0.05	0.3	1,000 ±20	0.0054	0.05	0.05
LX1602A(F), LX1702A(F)(N)	0 to 15 psia	40 psia	2.5 ±0.3	0.0072	0.06	0.3	670 ±13	0.0072	0.07	0.06
LX1603A(F), LX1703A(F)(N)	0 to 30 psia	60 psia	2.5 ±0.25	0.009	0.1	0.3	333 ±6	0.009	0.16	0.10
LX1610A(F), LX1710A(F)(N)	0 to 60 psia	100 psia	2.5 ±0.25	0.018	0.2	0.6	167 ±3.3	0.018	0.36	0.24
LX1420A(F)(S)	0 to 100 psia	150 psia	2.5 ±0.25	0.030	0.4	1.0	100 ±2	0.03	0.60	0.40
LX1620A(F), LX1720A(F)(N)	0 to 100 psia	150 psia	2.5 ±0.2	0.0216	0.4	1.0	100 ±2	0.0216	0.60	0.40
LX1430A(F)(S)	0 to 300 psia	450 psia	2.5 ±0.25	0.090	1.0	2.0	33.3 ±0.67	0.09	2.0	1.0
LX1730A(F)(N)	0 to 300 psia	450 psia	2.5 ±0.2	0.063	1.0	2.0	33.3 ±0.67	0.063	2.0	1.0
LX1440A(F)(S)	0 to 1000 psia	1500 psia	2.5 ±0.25	0.3	3.5	7.0	10 ±0.2	0.3	6.0	3.0
LX1450A(F)(S)	0 to 2000 psia	3000 psia	2.5 ±0.25	0.6	7.0	14	5 ±0.1	0.6	20.0	7.0
LX1460A(F)(S)	0 to 3000 psia	4500 psia	2.5 ±0.25	0.9	10.0	20.0	3.33 ±0.067	0.9	30.0	10.0
LX1470A(F)(S)	0 to 5000 psia	5000 psia	2.5 ±0.25	1.5	17.0	35.0	2 ±0.04	1.5	75.0	17.0
GAGE PRESSURE DEVICES										
LX1601G(B),LX1701G(B)(N)*	−5 to +5 psig	40 psig	7.5 ±0.5	0.0054	0.05	0.3	1,000 ±20	0.0054	0.05	0.05
LX1611G(B),LX1711G(B)(N)*	−5 to +5 psig	100 psig	7.5 ±0.5	0.0054	0.05	0.3	1,000 ±20	0.0054	0.05	0.05
LX1602G(B),LX1702G(B)(N)*	0 to 15 psig	40 psig	2.5 ±0.3	0.0072	0.06	0.3	670 ±13	0.0072	0.07	0.06
LX1603G(B),LX1703G(B)(N)*	0 to 30 psig	60 psig	2.5 ±0.25	0.009	0.1	0.3	333 ±6	0.009	0.16	0.10
LX1604G(B),LX1704G(B)(N)*	−15 to +15 psig	40 psig	7.5 ±0.25	0.009	0.1	0.3	333 ±6	0.009	0.16	0.10
LX1610G(B),LX1710G(B)(N)*	0 to 60 psig	100 psig	2.5 ±0.25	0.018	0.2	0.6	167 ±3.3	0.018	0.36	0.24
LX1620G(B),LX1720G(B)(N)*	0 to 100 psig	150 psig	2.5 ±0.2	0.0216	0.4	1.0	100 ±2	0.0216	0.60	0.40
LX1730G(B)(N)*	0 to 300 psig	450 psig	2.5 ±0.2	0.063	1.0	2.0	33.3 ±0.67	0.063	2.0	1.0
DIFFERENTIAL PRESSURE DEVICES										
LX1601D(F), LX1701DD(F)	−5 to +5 psid	40 psid	7.5 ±0.5	0.0054	0.05	0.3	1,000 ±20	0.0054	0.05	0.05
LX1611D(F), LX1711DD(F)	−5 to +5 psid	100 psid	7.5 ±0.5	0.0054	0.05	0.3	1,000 ±20	0.0054	0.05	0.05
LX1602D(F), LX1702DD(F)	0 to 15 psid	40 psid	2.5 ±0.35	0.0072	0.06	0.3	670 ±13	0.0072	0.07	0.06
LX1603D(F), LX1703DD(F)	0 to 30 psid	60 psid	2.5 ±0.3	0.009	0.1	0.3	333 ±6	0.009	0.16	0.10
LX1604D(F), LX1704DD(F)	−15 to +15 psid	40 psid	7.5 ±0.3	0.009	0.1	0.3	333 ±6	0.009	0.16	0.10
LX1610D(F), LX1710DD(F)	0 to 60 psid	100 psid	2.5 ±0.25	0.018	0.2	0.6	167 ±3.3	0.018	0.36	0.24
LX1620D(F), LX1720DD(F)	0 to 100 psid	150 psid	2.5 ±0.2	0.0216	0.4	1.0	100 ±2	0.0216	0.60	0.40
LX1730DD(F)	0 to 300 psid	450 psid	2.5 ±0.2	0.063	1.0	2.0	33.3 ±0.67	0.063	2.0	1.0

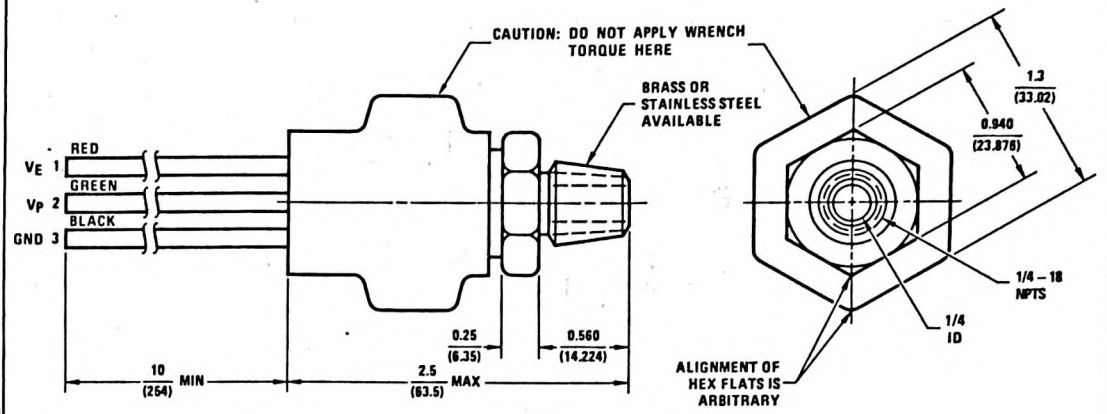
†Reference pressure for LX1601A and LX1701A is 10 psia.
*Available as LX17XXGB or LX17XXGN

PRESSURE TRANSDUCER FEATURE CHART

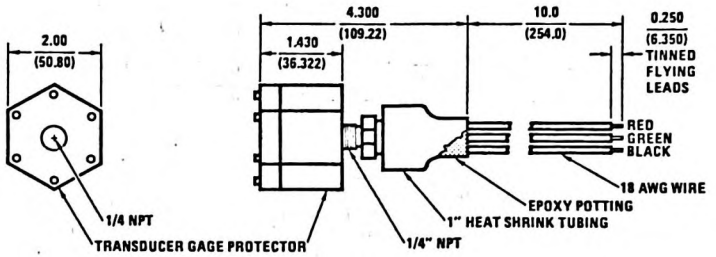
Product \ Feature	Brass Housing	Stainless Steel Housing	Ceramic Package	Nylon Housing	Zinc Housing	High Common-Mode Differential Housing	Fluid-Filled Isolator	Backward Gage Isolator
LX14XX Absolute	LX14XXA	LX14XXAS					LX14XXAF LX14XXAFS	
LX16XX Absolute			LX16XXA				LX16XXAF	
LX16XX Gage			LX16XXG					LX16XXGB
LX16XX Differential			LX16XXD				LX16XXDF	
LX17XX Absolute				LX17XXAN	LX17XXA		LX17XXAF LX17XXAFN	
LX17XX Gage				LX17XXGN	LX17XXG			LX17XXGB (Zinc)
LX17XX Differential						LX17XXDD (Brass)	LX17XXDDF	

Package Key

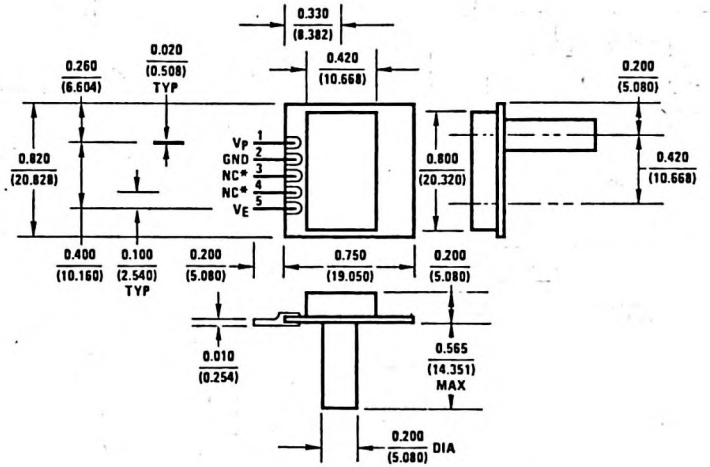
TYPE	PACKAGE
LX14XXA(S) LX14XXAF(S)	PX4(S) PX4F(S)
LX16XXA LX16XXG LX16XXGB LX16XXD(F)	PX6 PX6 PX6B PX6D(F)
LX17XXA(F)(N) LX17XXG(N) LX17XXGB LX17XXDD(F)	PX7(F)(N) PX7(N) PX7B PX7DD(F)



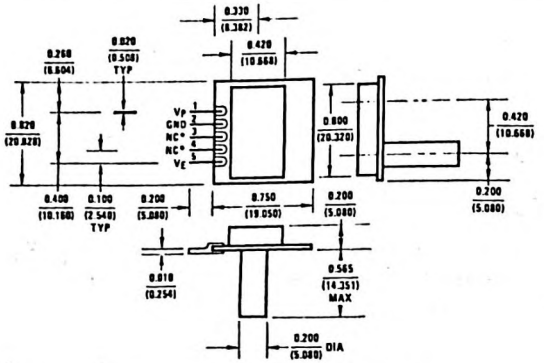
PX4(S)
1/4" NPT Pressure Transducer Package
Wt: 100 G



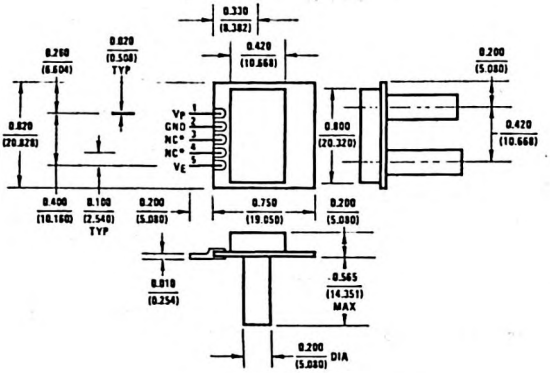
PX4F(S)
1/4" NPT Pressure Transducer Package, Fluid Filled
Wt: 700 G



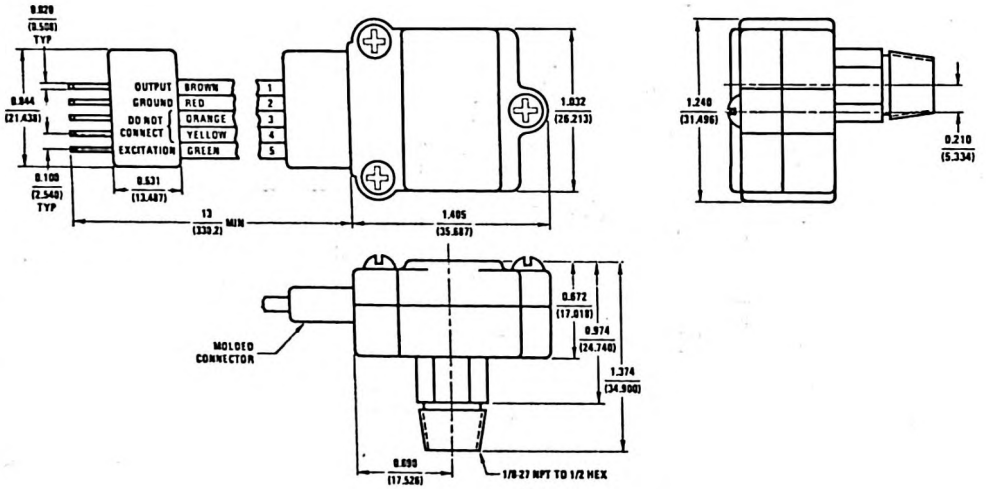
PX6
0.2" Port, Hybrid Pressure Transducer Package
Wt: 5 G



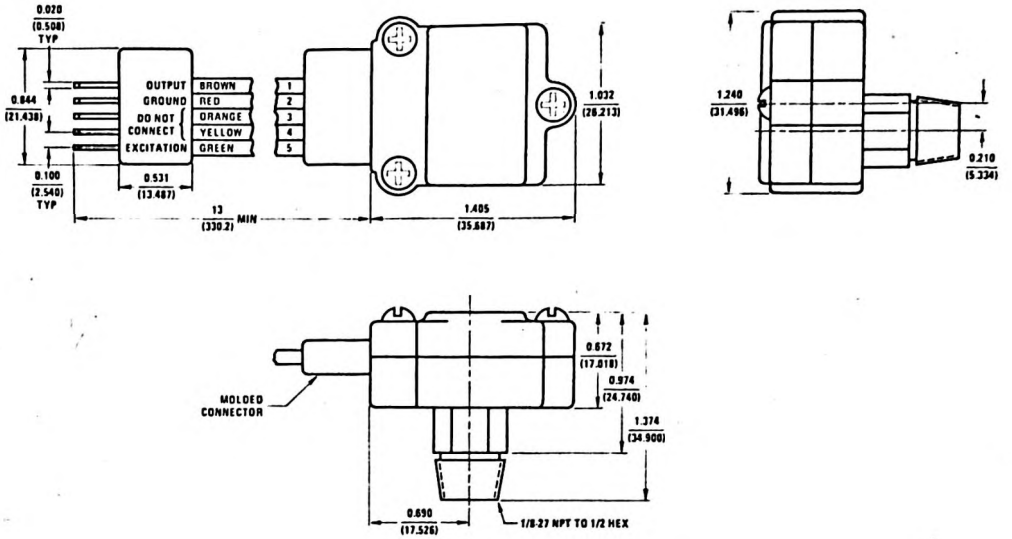
PX6B
0.2" Port, Hybrid Pressure Transducer Package
Wt: 5 G



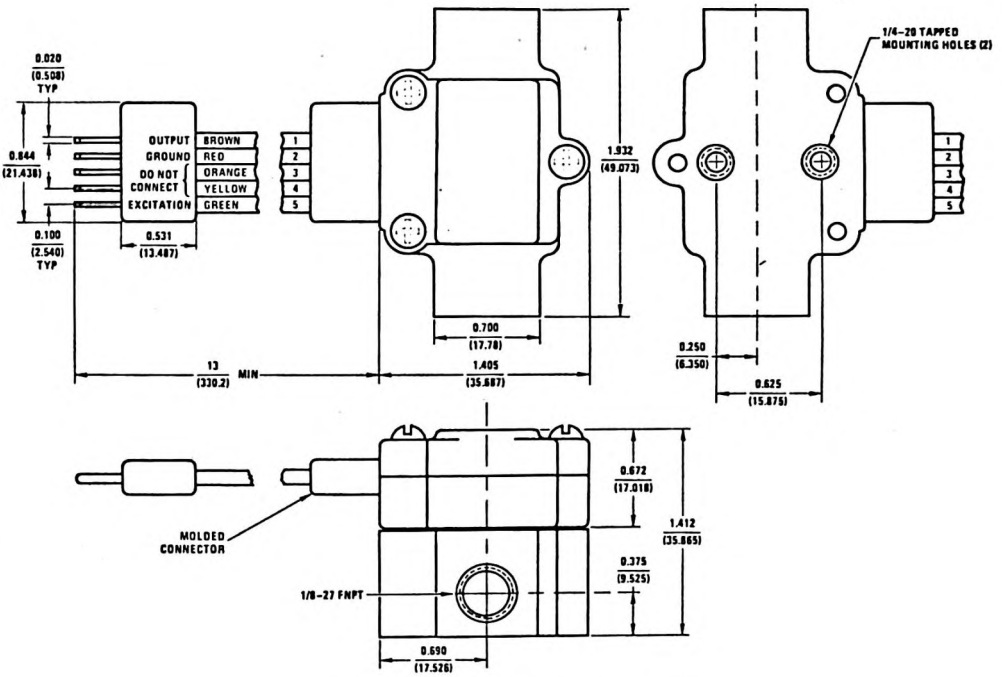
PX6D
0.2" Port, Hybrid Pressure Transducer Package
Wt: 5 G



PX7
1/8" NPT Zinc Cast Pressure Transducer Package
Wt: 100 G (Zinc), 50 G (Nylon — With Identical Mechanical Performance)



PX7B
1/8" NPT Zinc Cast Pressure Transducer Package
Wt: 100 G (Zinc)



PX7DD
1/4" NPT Brass Pressure Transducer Package
Wt: 270 G

Section 2

Analog-to-Digital Converters

2

National Semiconductor

Analog-to-Digital Converters

ADB1200(MM5863) 12-Bit Binary A/D Building Block

general description

The ADB1200 is the digital controller for the LF13300D* analog building block. Together they form an integrating 12-bit A/D converter. The ADB1200 provides all the necessary control functions, plus features like auto zeroing, polarity and overrange indication, as well as continuous conversion. The 12-bit plus sign parallel and serial outputs are TRI-STATE® TTL level compatible. The device also includes output latches to simplify data bus interfacing.

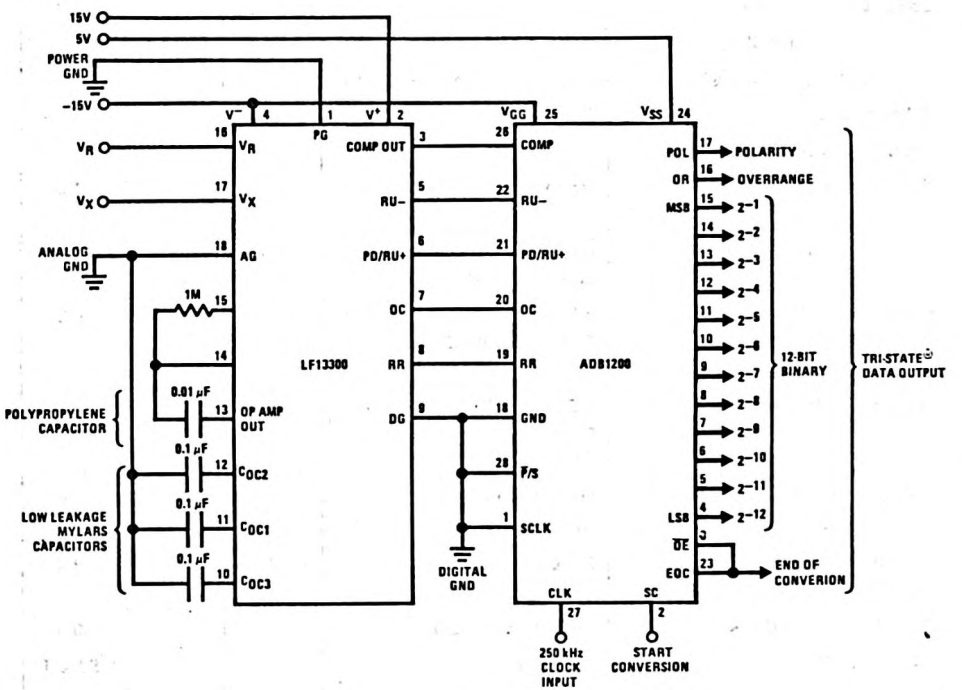
*See LF13300D data sheet for more information

features

- 12-bit binary output
- Parallel or serial output
- TRI-STATE output
- Polarity indication
- Overrange indication
- Continuous conversion capability
- 100% overrange capability
- 5V, −15V power requirements
- TTL compatible
- Clock frequency to 1 MHz

circuit diagram/typical applications

12-Bit A/D Converter



absolute maximum ratings

Supply Voltage (V_{SS})	5.25V
Supply Voltage (V_{GG})	−16.5V
Voltage at Any Input	5.25V
Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

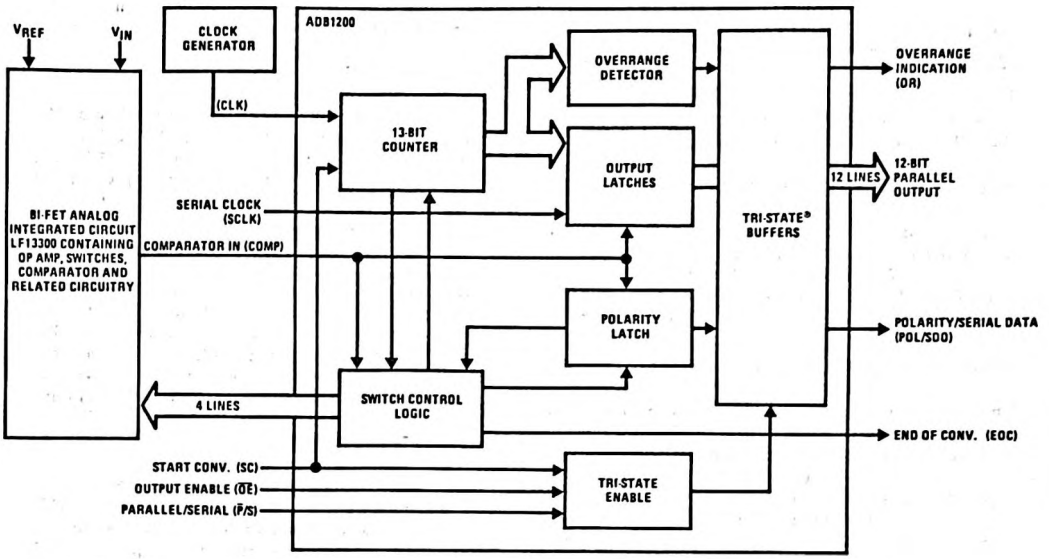
electrical characteristics

V_{SS} = 5V, V_{GG} = −15V, 0°C to +70°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5.00	5.25	V
Power Supply Voltage (V_{GG})		−13.5	−15.00	−16.5	V
Power Supply Current (I_{SS})				28	mA
Power Supply Current (I_{GG})				34	mA
Logic "1" Input Voltage		3.4			V
Logic "0" Input Voltage				0.8	V
Logic "1" Output Voltage	V_{SS} = 4.75V, I_{OH} = 100 μA	3.8			V
Logic "0" Output Voltage	V_{SS} = 5.25V, I_{OL} = −1.6 mA			0.4	V
Width of EOC	Auto Cycle	5/f			sec
Prop. Delay COMP to EOC		4/f		5/f+1 μs	sec
Output Enable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			1.0	μs
Output Disable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			2.4	μs
Output Enable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			0.9	μs
Output Disable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			2.2	μs
Output Enable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			1.0	μs
Output Disable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			2.4	μs
Prop. Delay Serial Clock	SCLK to POL/SDO			0.6	μs
Conversion Time	Full Scale			8966/f	sec
Conversion Time	100% Overrange			13062/f	sec
Maximum Clock Frequency	CLK, Pin 27	500	1000		kHz
Maximum Serial Clock Frequency	SCLK, Pin 1	500	1000		kHz

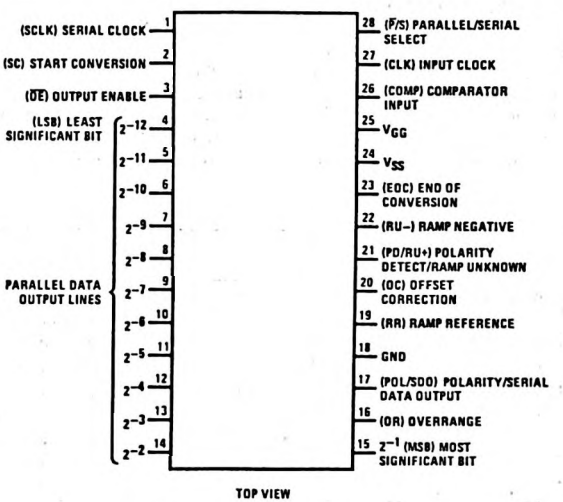
block diagram

Digital Control Integrated Circuit



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number ADB1200PCN
See NS Package N28A

functional description

OPERATION

The ADB1200 is designed for use with the LF13300 analog front end. Four control signals are supplied to the LF13300 and 1 control signal is required from the LF13300. The conversion cycle is composed of 5 distinct phases. They are: Phase I — Offset Correct; Phase II — Polarity Detect; Phase III — Initialization; Phase IV — Ramp Unknown; Phase V — Ramp Reference.

Phase I — Offset Correct (256 Clock Periods)

This phase is initiated by taking the Start Conversion (SC) and the Output Enable ($\overline{OE}$) lines to a logic "1". At this time, Offset Correct (OC) will be a logic "1". The LF13300 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase.

Phase II — Polarity Detect (256 Clock Periods)

This phase is used to determine polarity of the analog input. At the midpoint of this phase, COMP from the LF13300 is examined for polarity. If COMP = logic "1", then the input voltage is positive. If COMP = logic "0", then the input is negative. The Polarity Detect signal (PD/RU+) will be at a logic "1" during this entire phase. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion (see LF13300 data sheet).

Phase III — Initialization (256 Clock Periods)

This phase is identical to Phase I and is used by the LF13300 to eliminate any offsets induced as a result of the Polarity Detect Phase. Offset Correct (OC) will be at a logic "1".

Phase IV — Ramp Unknown (4096 Clock Periods)

The unknown input voltage is integrated for a fixed time, 4096 clock periods, during this phase. The result of the Phase II Polarity Detect Cycle determines whether PD/RU+ or RU— will be at logic "1". If Phase II indicates a positive input, the PD/RU+ signal will be a logic "1". If phase II indicates a negative input, Ramp Negative (RU—) will be a logic "1". These 2 signals will never be at logic "1" simultaneously.

Phase V — Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be in the logic "1" state. When COMP goes to a logic "0" state, or when the internal counter reaches 100% of full scale (8192 clock periods), the Ramp Reference (RR) signal goes to the logic "0" state, the counter output is loaded into the output register, and the End of Conversion (EOC) signal goes to a logic "1". The Polarity Bit will reflect whatever value was determined during Phase II. The output register will hold the data until a new conversion is completed and new data is loaded into the register. The $\overline{OE}$ line must be low in the logic "0" state and SC must be high in the logic "1" state to enable the outputs.

DATA OUTPUTS

Both serial and parallel outputs are available. In either case, $\overline{OE}$ must be low and SC must be high to enable the outputs. For parallel output, the $\overline{P}$/S line must be low in the logic "0" state. For serial outputs, the $\overline{P}$/S line must be high. In the serial mode, the data is shifted out of the Polarity/Serial Output (POL/SDO) line and all other data outputs are in the high impedance state. Each Serial Clock (SCLK) will right shift the output register one bit. Thus, 13 clock pulses are required to fully shift out the data. The data will be shifted out in the following order: Polarity, Overrange, MSB, 2SB, 3SB, . . . , LSB. If $\overline{OE}$ and $\overline{P}$/S are in the logic "0" state and SC in the logic "1" state, all outputs will momentarily go to the logic "1" state for 1 clock period immediately preceding EOC.

CONTINUOUS CONVERT MODE

In this mode, the End of Conversion (EOC) output is connected to the $\overline{OE}$ input. As long as SC is in the logic "1" state, then each EOC will initiate a new conversion. The data outputs will be disabled for the first 5 clock cycles after EOC goes high.

truth table

INPUT	SC	OE	P/S	LSB											MSB	OVER-RANGE	POLARITY
100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
—Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
—100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Any	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Any	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Serial Output
Any	0	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

1 = High
0 = Low
Z = High Impedance
X = Don't Care

timing diagrams

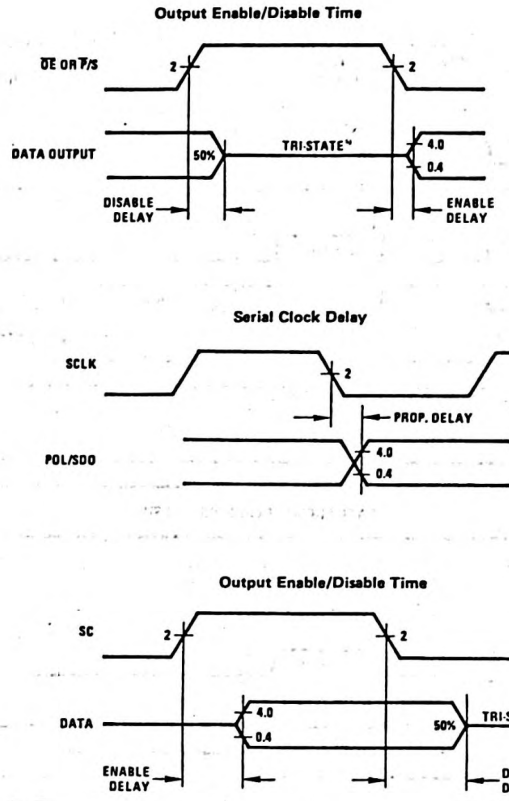


FIGURE 1. Parallel Data

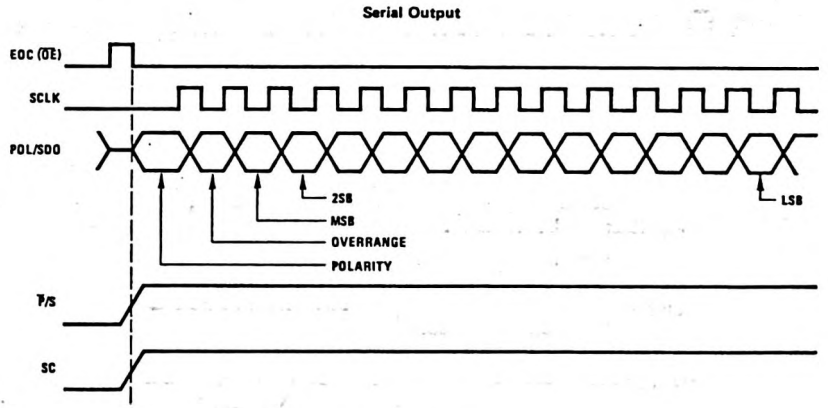
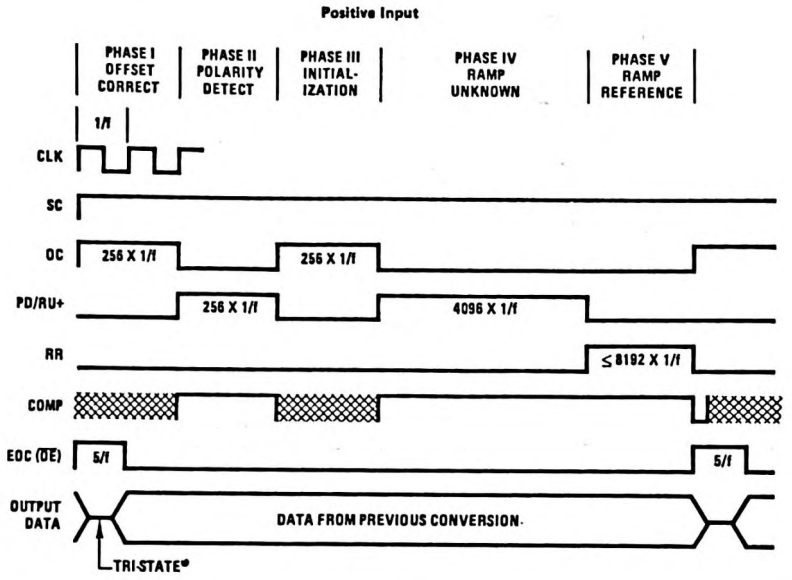


FIGURE 2. Serial Data

timing diagrams (Continued)



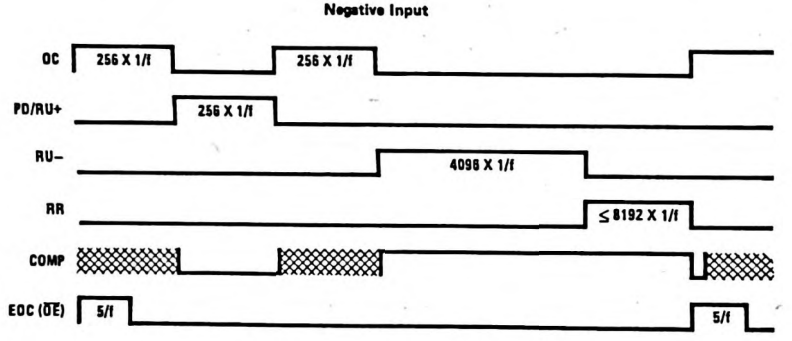


FIGURE 3. Continuous Conversion Mode

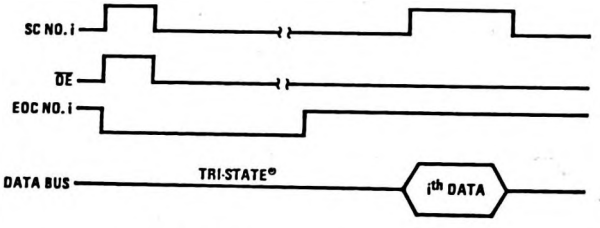
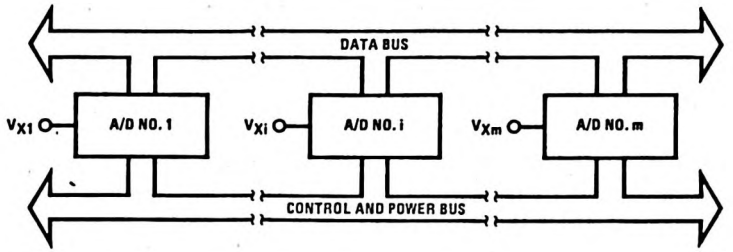


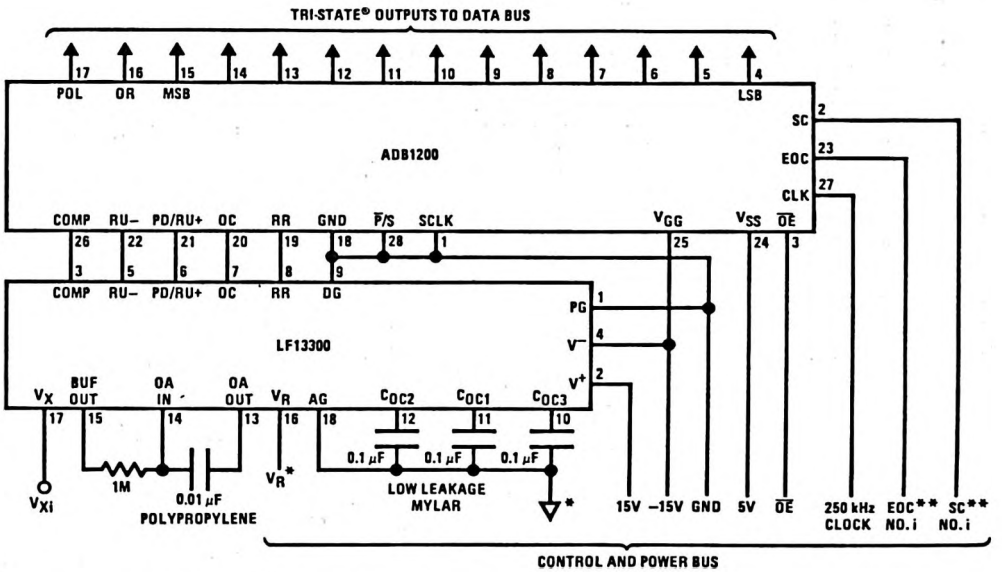
FIGURE 4. i^{th} A/D Converter Data Retrieval Sequence

typical applications (Continued)

Multi A/D Converter System on Common Bus



i^{th} A/D Converter


TRI-STATE® OUTPUTS TO DATA BUS
17 16 15 14 13 12 11 10 9 8 7 6 5 4
POL OR MSB LSB
ADB1200
SC 2
EOC 23
CLK 27
COMP RU− PD/RU+ OC RR GND F/S SCLK V_{GG} V_{SS} OE
26 22 21 20 19 18 28 1 25 24 3
3 5 6 7 8 9
COMP RU− PD/RU+ OC RR DG
LF13300
PG 1
V^- 4
V^+ 2
V_X BUF OUT OA IN OA OUT V_R AG C_{OC2} C_{OC1} C_{OC3}
17 15 14 13 16 18 12 11 10
0.1 μF 0.1 μF 0.1 μF
1M
0.01 μF
POLYPROPYLENE
V_{Xi}
V_R*
LOW LEAKAGE MYLAR
*
15V −15V GND 5V OE
250 kHz CLOCK
EOC** NO. i
SC** NO. i
CONTROL AND POWER BUS

*May be common or separate. Care should be taken to avoid ground currents
**Direct or multiplexed access to the processor
Note. This application is related to *Figure 4* of timing diagrams

National Semiconductor

Analog-to-Digital Converters

ADC0800(MM4357B/MM5357B) 8-Bit A/D Converter

General Description

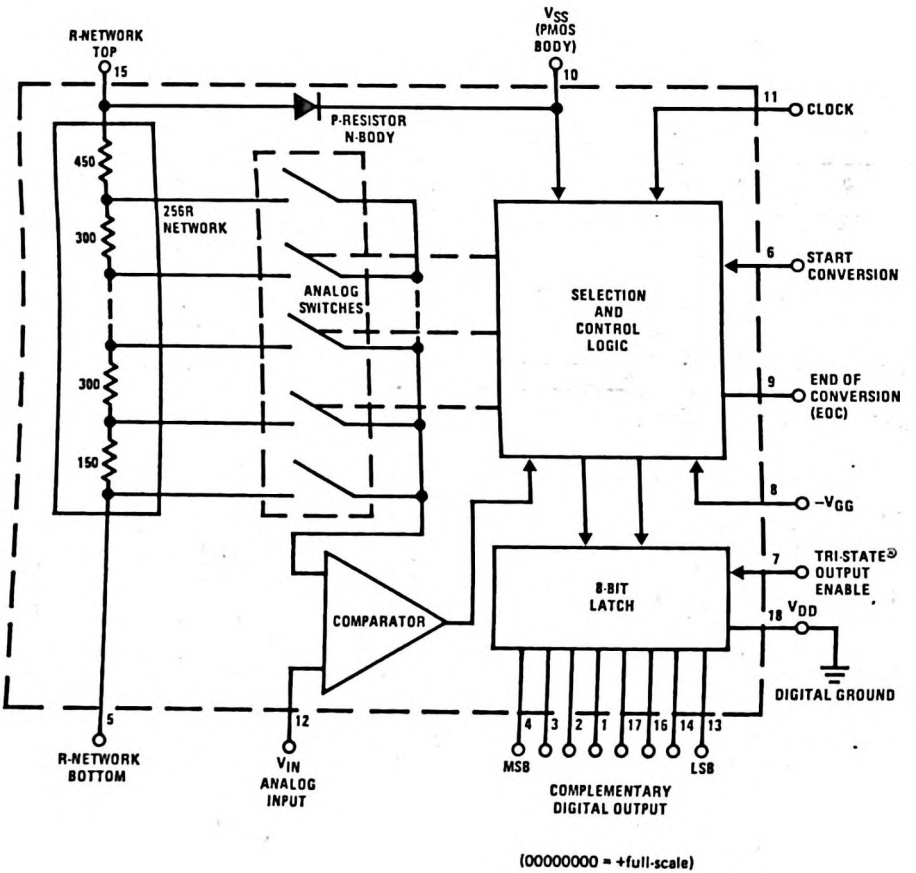
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCN and ADC0800PCD are specified over 0°C to +70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — T_C = 50 μs
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD})	V_{SS}–22V
Supply Voltage (V_{GG})	V_{SS}–22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}–22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	−55°C to +125°C
ADC0800PCN, ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

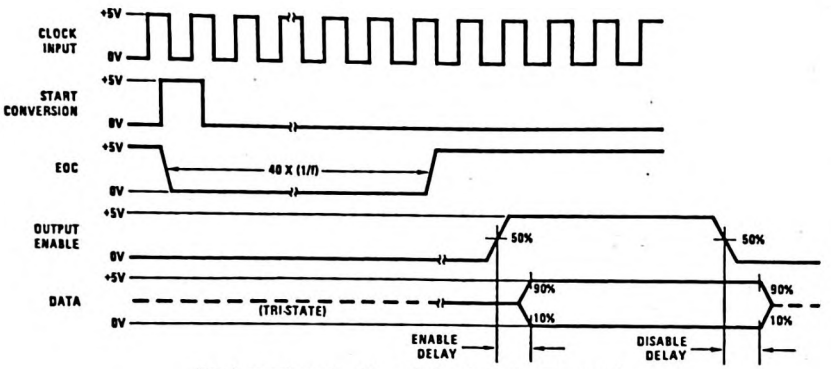
Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = −12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}$ = 5.000 V_{DC} and $V_{R\text{-}NETWORK\ BOTTOM}$ = −5.000 V_{DC}), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCN and the ADC0800PCD.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Non-Linearity	T_A = 25°C, (Note 1)			±1	LSB
	Over Temperature, (Note 1)			±2	LSB
Differential Non-Linearity				±1/2	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 2)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 2)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	V_{SS}–1.0		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}–4.2	V
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} − 10V			1	μA
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4			V
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	V
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2	μA
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800	kHz
	−55°C ≤ T_A ≤ +125°C	100		500	kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 3)	1		3 1/2	Clock Periods
Power Supply Current	T_A = 25°C			15	mA

Note 1: Non-linearity specifications are based on best straight line.
Note 2: Guaranteed by design only.
Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

Timing Diagram



Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time. Conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, which is applied to the top of the R-network (pin 15), must not exceed V_{SS} to prevent forward biasing the on-chip parasitic silicon diode which exists between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp which is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage which is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_s \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_s \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_s > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than (1/44) x f_{CLOCK} automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converts for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

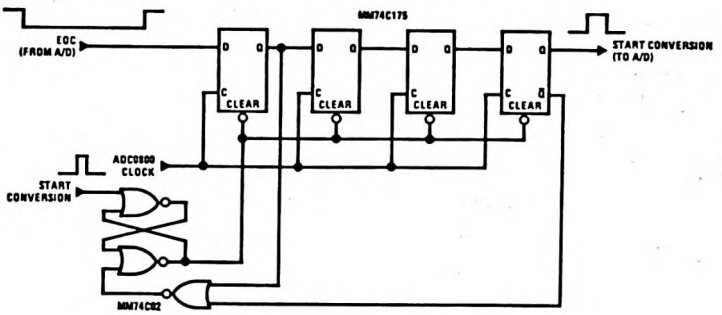


FIGURE 1. Delaying an Asynchronous Start Pulse

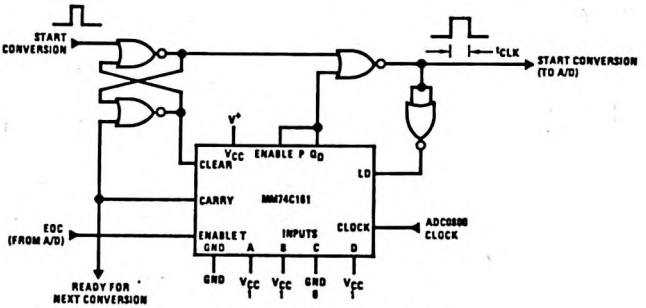


FIGURE 2. A/D Control Logic

Application Hints (Continued)

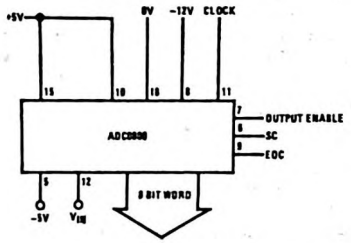
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is 1/2 LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

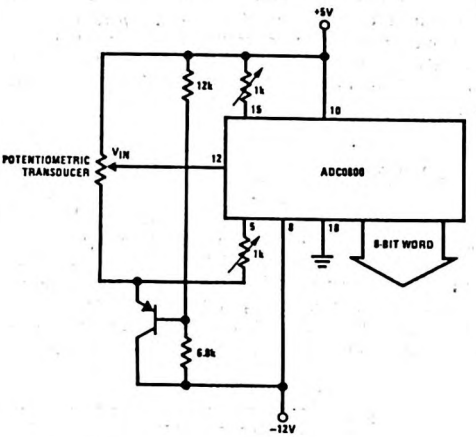
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

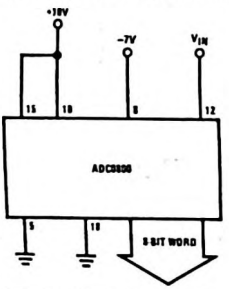
General Connection



Ratiometric Input Signal with Tracking Reference

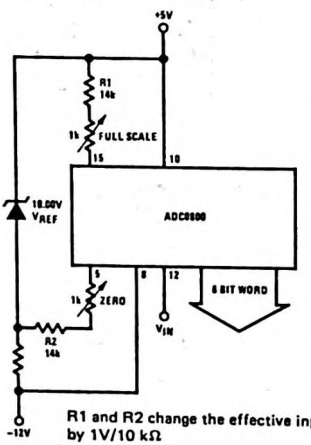


Hi-Voltage CMOS Output Levels



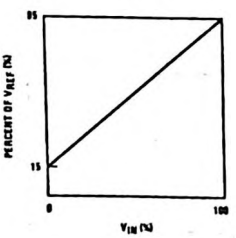
0V to 10V V_{IN} range
0V to 10V output levels

Level Shifted Zero and Full-Scale for Transducers



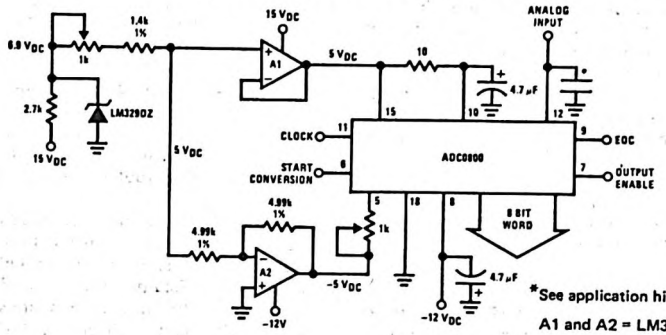
R1 and R2 change the effective input range by 1V/10 kΩ

Level Shifted Input Signal Range



Typical Applications (Continued)

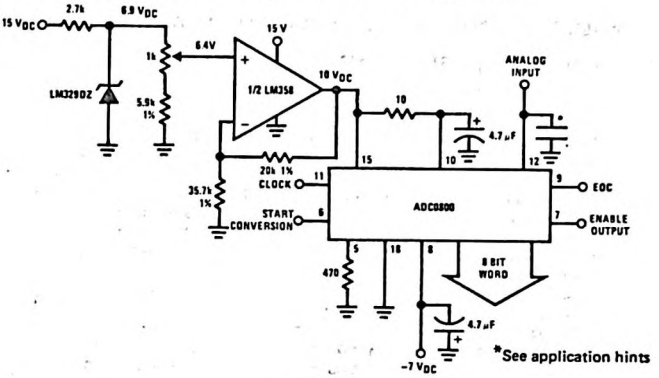
V_{REF} = 10 V_{DC} With TTL Logic Levels



*See application hints

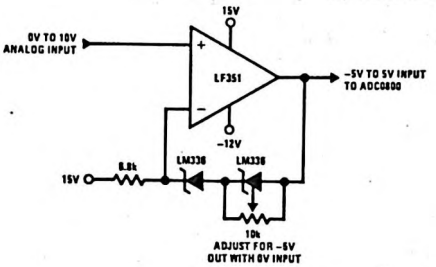
A1 and A2 = LM358N dual op amp

V_{REF} = 10 V_{DC} With 10V CMOS Logic Levels



*See application hints

Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the converter, load the converter's output data into the accumulator, keep track of the number of data bytes entered, complement the data and store this data into sequential memory locations. After 256 bytes have been entered, the control jumps to the user's program where proces-

Typical Applications (Continued)

sing of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→ 02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000→ — full-scale.

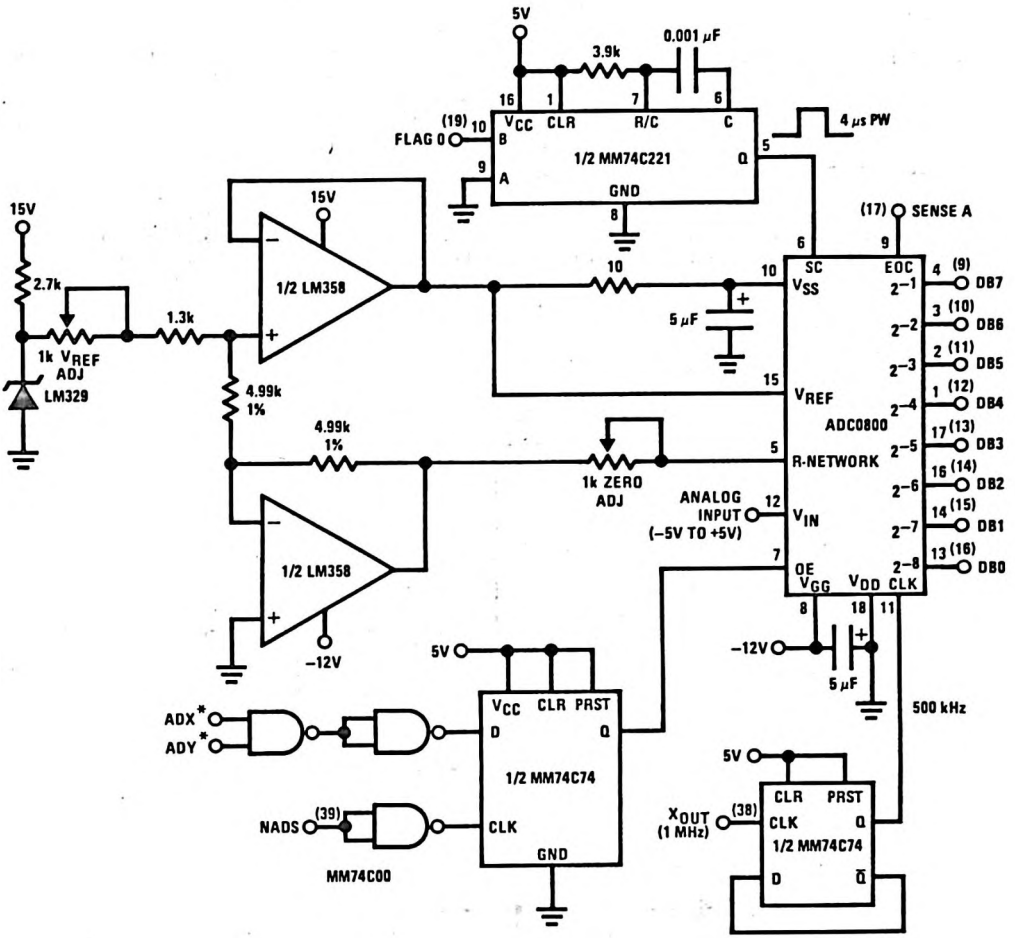
Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure 3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08      START:      NOP
0002  C4 01                LDIX'01
0004  35                  XPAH 1
0005  C4 00                LDIX'00
0007  31                  XPAL 1        ;P1 = 0100
0008  C4 02                LDIX'02
000A  36                  XPAH 2
0008  C4 00                LDIX'00
000D  C9 00                ST(P1)        ;Zero word count (P1)
000F  32                  XPAL 2        ;P2 = 0200
0010  C4 03                LDIX'03
0012  37                  XPAH 3
0013  08      INITIALIZE: NOP
0014  C4 00                LDIX'00
0016  33                  XPAL 3        ;P3 = 0300
0017  C4 01                LDIX'01
0019  07                  CAS           ;Starts converter via flag 0
001A  C1 00                LD (P1)
001C  F4 FF                XRIX'FF
001E  98 05                JZ DTA IN     ;Test to see if word count is FF,
                                          if so, jump to DTA IN
0020  05                  IEN           ;Enables INTERRUPT
0021  08      LOOP:       NOP
0022  90 FE                JMP LOOP      ;Loop until EOC
0024  08      DTA IN:     NOP
                          .
                          .
                          .             ;User program to process data
                          .
                          .
                          .
   :DATA ENTRY SUBROUTINE
0300  08      DATA IN SR: NOP
0301  A9 00                ILD (P1)      ;Increment word count
0303  C4 05                LDIX'05
0305  35                  XPAH 1        ;P1 will point to converter
0306  C1 00                LD (P1)       ;Converter data loaded into
                                          accumulator
0308  F4 7F                XRIX'7F       ;Put data in 2's complement form
030A  CE 01                ST @ 1(P2)    ;Store data
030C  C4 00                LDIX'00
030E  07                  CAS           ;Resets flag 0
030F  C4 01                LDIX'01
0311  35                  XPAH 1        ;Resets P1 to point at word count
0312  C4 13                LDIX'13
0314  33                  XPAL 3
0315  3F                  XPPC 3        ;Return to INITIALIZE to start a
                                          new conversion
```

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LED's to display the resulting digital output code as shown in *Figure 4*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

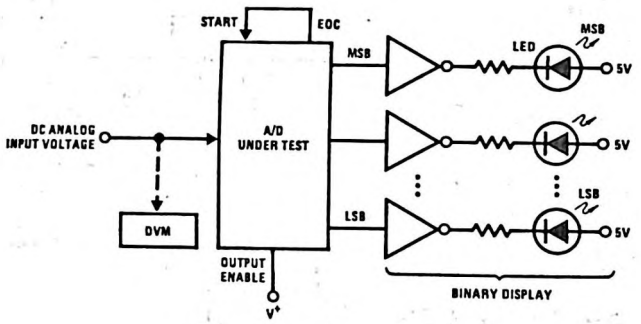


FIGURE 4. Basic A/D Tester

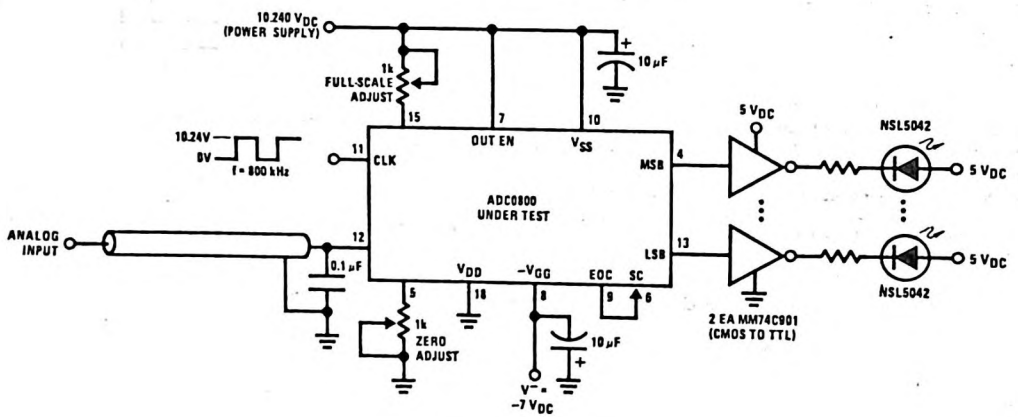


FIGURE 5. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 6* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

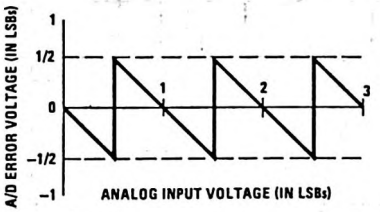


FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 7*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

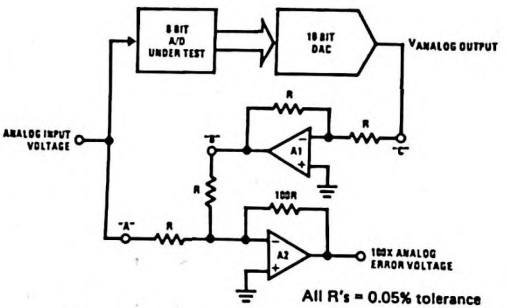


FIGURE 7. A/D Tester with Analog Error Output

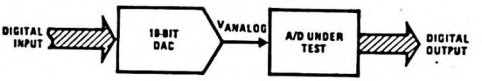
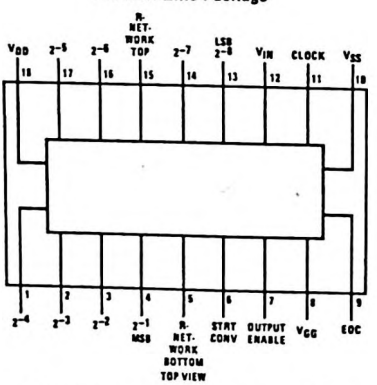


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

Order Number ADC0800PCN (0°C to +70°C)
See NS Package N18A

National Semiconductor

Analog-to-Digital Converters

ADC0808, ADC0809 Single Chip Data Acquisition System

General Description

The ADC0808, ADC0809 data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stablilzed comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any one of 8-single-ended analog signals.

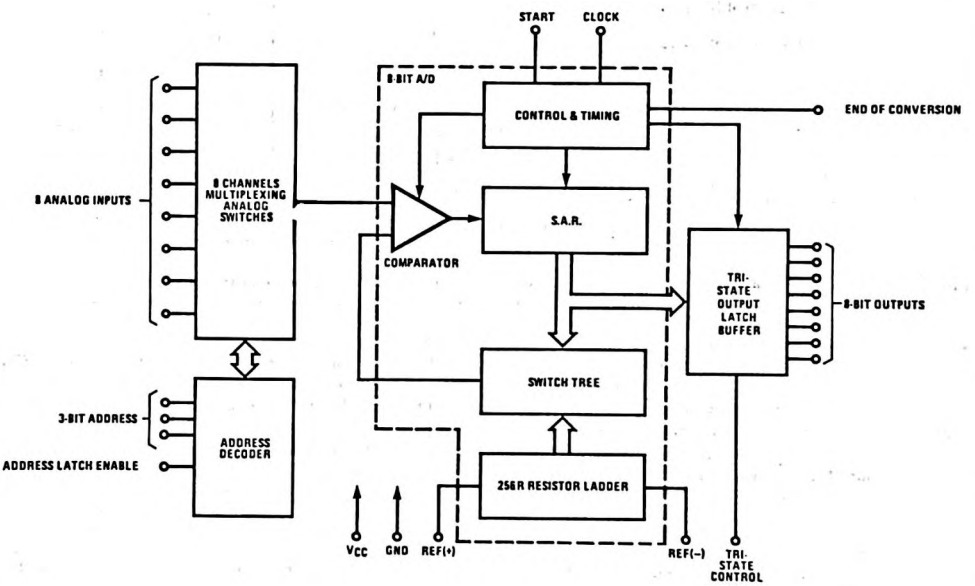
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy $\leq$ 1 LSB including quantizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

Features

- Total unadjusted error $<$ ±1/2 LSB
- Linearity error $<$ ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW
- Full −55°C to +125°C operation available

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Control Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Control Inputs (Start, TRI-STATE, Clock, ALE, ADD A, ADD B, ADD C)	−0.3V to + 15V
Operating Temperature Range	
ADC0808CCN, ADC0809CCN	−40°C to +85°C
ADC0808CD	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (at 25°C)	500 mW
Operating V_{CC} Range	4.5V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

ADC0808CCN, ADC0809CCN

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted, (Note 2)

ADC0808CD

$4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA @ T_A = 85°C I_O = −300 μA @ T_A = 125°C	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	Clock Frequency = 500 kHz				
		@ T_A = 85°C		300	1000	μA
		@ T_A = 125°C			3000	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V			3	μA
		V_O = 0	−3			μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic, *(Figure 2)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 2)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage, *(Figure 2)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors, *(Figure 3)*.

Note 7: Quantization error is the ±1/2 LSB uncertainty caused by the converter's finite resolution, *(Figure 3)*.

Note 8: Absolute Accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance, *(Figure 3)*.

Note 9: Supply rejection relates to the ability of an ADC to maintain accuracy as the supply voltage varies. The supply and $V_{REF(+)}$ are varied together and the change in accuracy is measured with respect to full-scale.

Note 10: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence, *(Figure 5)*.

DC Electrical Characteristics (Continued)

ANALOG MULTIPLEXER

ADC0808CCN, ADC0809CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted.
ADC0808CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel)				
		$T_A = 25°C$, $R_L = 10k$		1.5	3	kΩ
		$T_A = 85°C$			6	kΩ
		$T_A = 125°C$			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$,		10	200	nA
		$T_A = 25°C$			200	nA
		ADC0808CD @ $T_A = 125°C$			400	nA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$,	−200	−10		nA
		$T_A = 25°C$	−200			nA
		ADC0808CD @ $T_A = 125°C$	−400			nA

CONVERTER SECTION

$V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $f_c = 640$ kHz
ADC0808CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted.
ADC0808CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/4	±1/2	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	$T_A = 25°C$ (Note 6)		±1/4	±1/2	LSB
	ADC0808CD		±1/4	±1/2	LSB
	ADC0808CCN		±1/4	±3/4	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	$T_A = 25°C$ (Note 8)		±3/4	±1	LSB
	ADC0808CD		±3/4	±1	LSB
	ADC0808CCN		±3/4	±1 1/4	LSB

ADC0809CCN $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/2	±1	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	(Note 6)		±1/2	±1	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	(Note 8)		±1	±1 1/2	LSB

ADC0808CCN $-40°C \leq T_A \leq +85°C$, **ADC0809CCN** $T_A = 25°C$
ADC0808CD $-55°C \leq T_A \leq +125°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection	$4.75V \leq V_{CC} = V_{REF(+)} \leq 5.25V$, (Note 9)		0.05	0.15	%/V
Comparator Input Current	$f_c = 640$ kHz, (Note 10)	−2	±0.5	2	μA
Ladder Resistance	From Ref(+) to Ref(−)	1	4.5		kΩ

DC Electrical Characteristics (Continued)

DESIGN GUIDELINES

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Voltage Across Ladder	From Ref(+) to Ref(−)	0.512	5.12	5.25	V
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2}-0.1$	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}-0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V

AC Electrical Characteristics

$T_A = 25°C$, $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{WS}	Start Pulse Width	*(Figure 5)*	200	100		ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*	200	100		ns
t_S	Address Set-Up Time	*(Figure 5)*	50	25		ns
t_H	Address Hold Time	*(Figure 5)*	50	25		ns
t_D	Analog MUX Delay Time From ALE	$R_S + R_{ON} \leq 5\ k\Omega$, $C_L = 10\ pF$		1	2.5	μs
t_{H1}, t_{H0}	TRI-STATE Control to Q Logic State	$C_L = 50\ pF$		125	250	ns
t_{1H}, t_{0H}	TRI-STATE Control to Hi-Z	$C_L = 10\ pF$, $R_L = 10k$		125	250	ns
t_C	Conversion Time	$f_C = 640\ kHz$, *(Figure 5)* (Note 11)	90	100	114	μs
f_C	Clock Frequency		10	640	1200	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	1		8	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
		At MUX Inputs		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		5	7.5	pF

Note 11: The outputs of the data register are updated one clock cycle before the rising edge of EOC.
Note 12: Capacitance guaranteed by periodic testing.

Timing Diagram

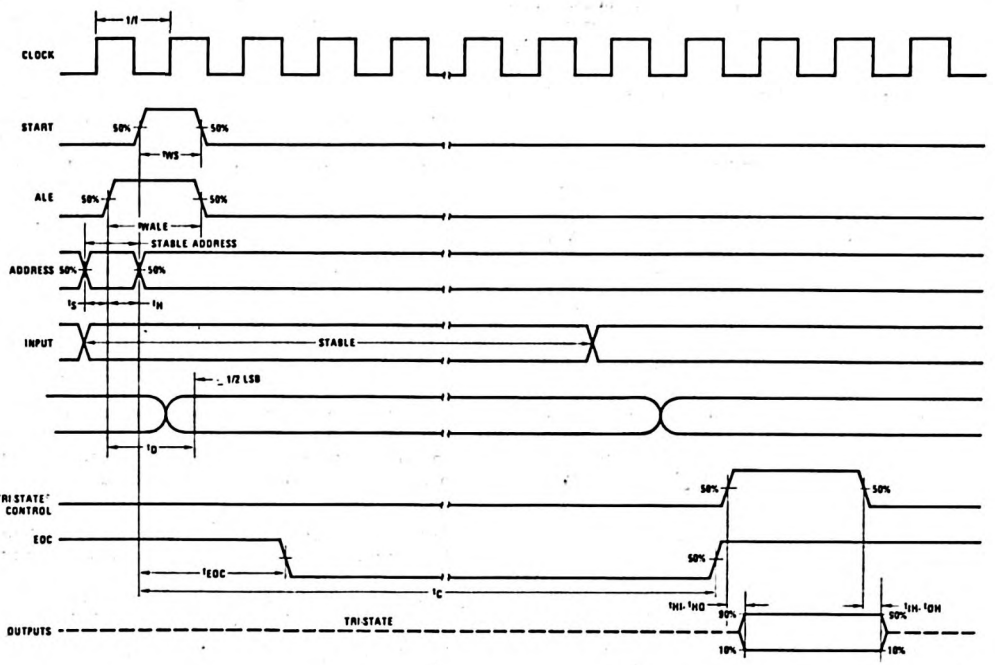


FIGURE 5

Typical Performance Characteristics

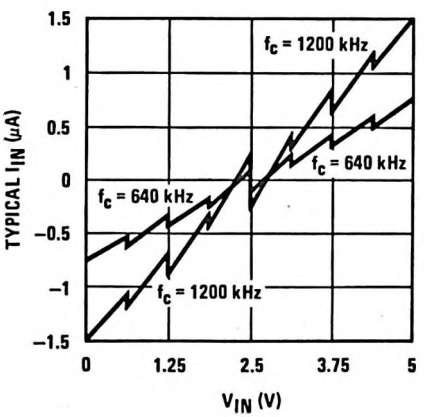


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

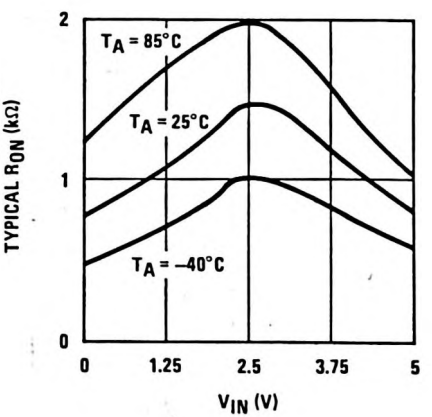


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

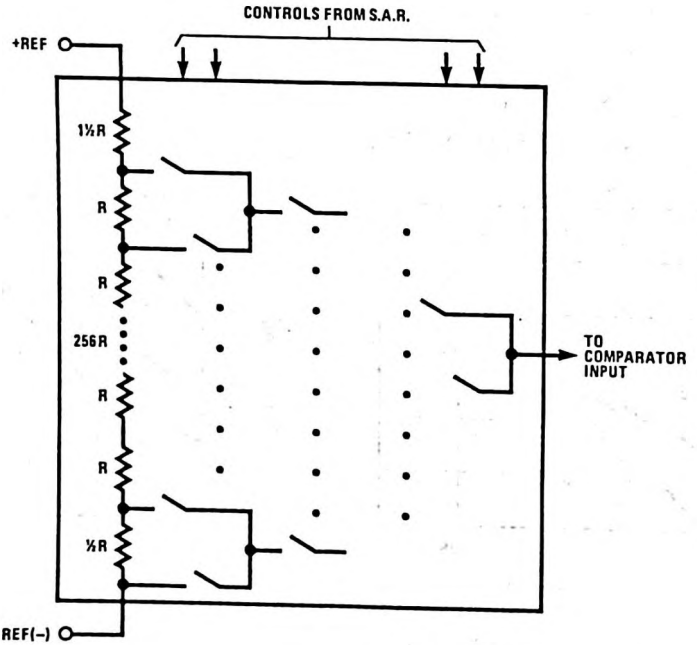


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 1 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179. The characteristic is generated with the analog input signal applied to the comparator input.

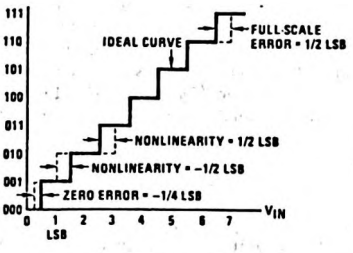


FIGURE 2. 3-Bit A/D Transfer Curve

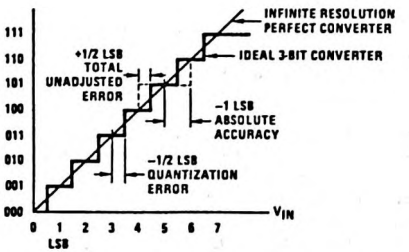


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

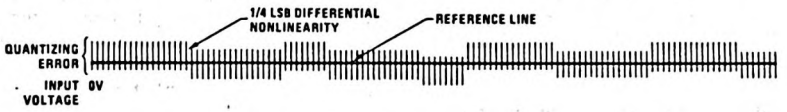
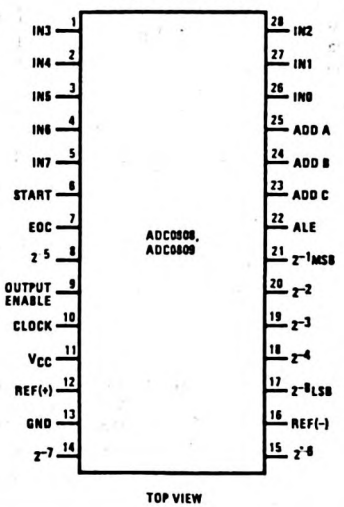


FIGURE 4. Typical Error Curve

Connection Diagrams

Dual-In-Line Package



TOP VIEW

Applications Information

OPERATION

Ratiometric Conversion

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{fs} = Full-scale voltage
V_z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 8)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder Ref(−) should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 9 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 10* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 11*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 12*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = V_{REF(+)} \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE} \quad (2)$$

The center of an output code N is given by:

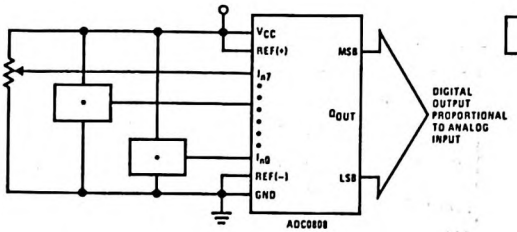
$$V_{IN} = V_{REF(+)} \left[\frac{N}{256}\right] \pm V_{TUE} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN}}{V_{REF(+)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = GND
V_{TUE} = Total unadjusted error voltage(typically $V_{REF(+)}/512$)

Applications Information (Continued)

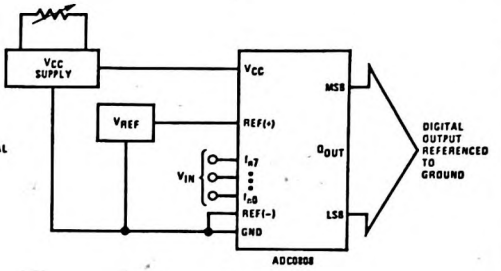


$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

*Ratiometric transducers

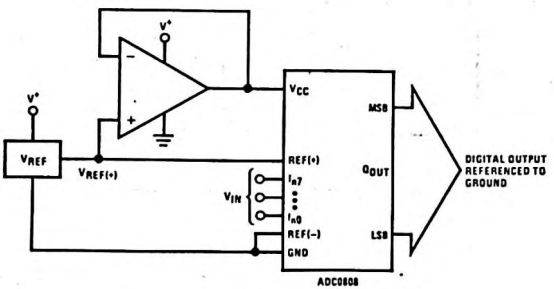
FIGURE 8. Ratiometric Conversion System



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 9. Ground Referenced Conversion System Using Trimmed Supply



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

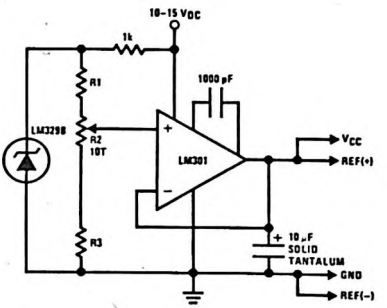
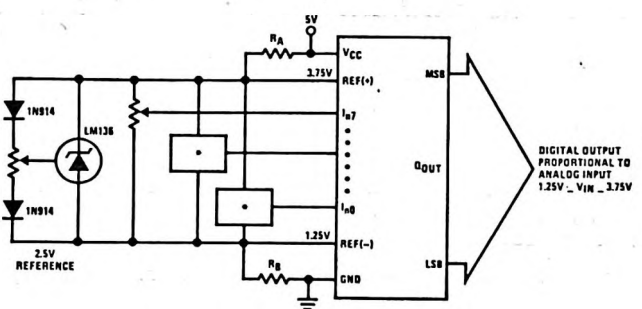


FIGURE 11. Typical Reference and Supply Circuit

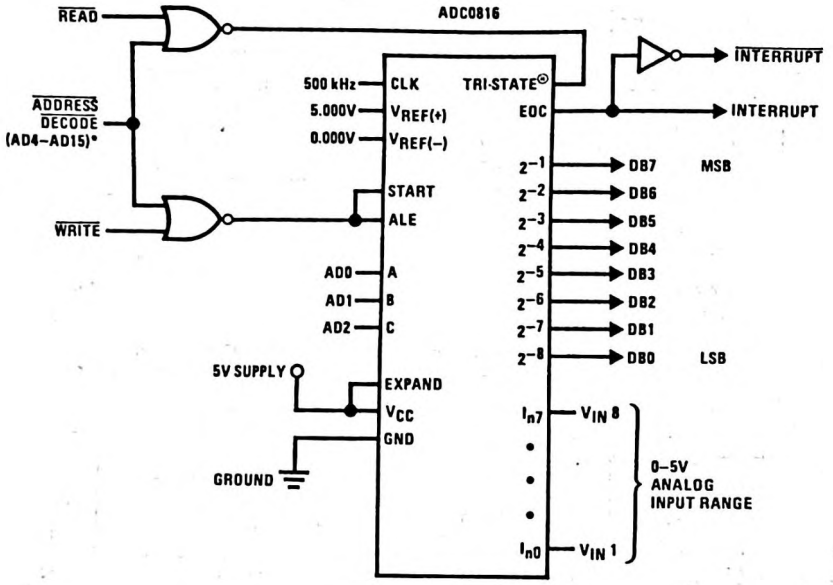


$R_A = R_B$

*Ratiometric transducers

FIGURE 12. Symmetrically Centered Reference

Typical Application



*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z–80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA · φ2 · R/W	VMA · φ2 · $\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

ORDER NUMBER	TEMPERATURE RANGE	25°C TOTAL UNADJUSTED ERROR	SEE NS PACKAGE NUMBER
ADC0808CD	−55°C to +125°C	±1/2 LSB	D28A
ADC0809CCN	−40°C to +85°C	±1/2 LSB	N28A
ADC0809CCN	−40°C to +85°C	±1 LSB	N28A

National Semiconductor

Analog-to-Digital Converters

ADC0816, ADC0817 Single Chip Data Acquisition System

General Description

The ADC0816, ADC0817 (MM74C948) data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, a 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16 single-ended analog signals and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the input of the 8-bit A/D converter.

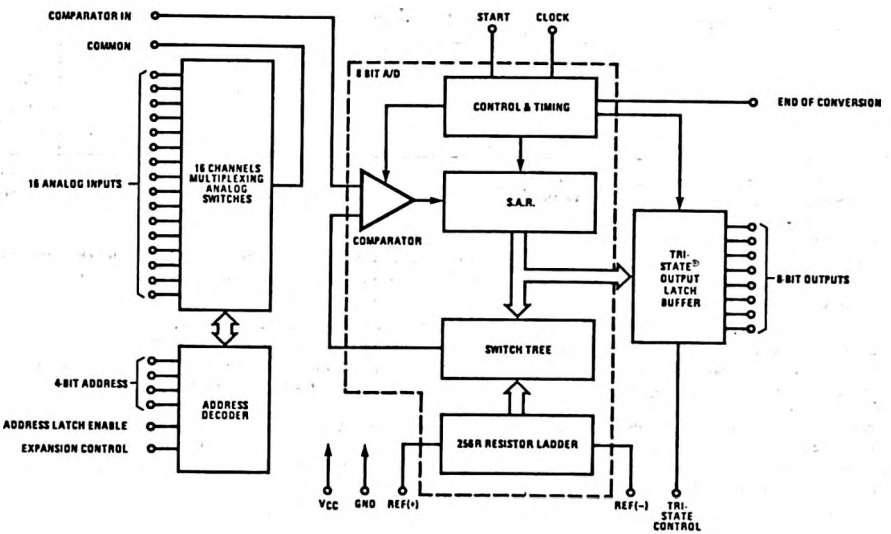
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy $\leq$ 1 LSB including quantizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control. For similar performance except 8-channel multiplexer in a 28-pin package, see ADC0808 data sheet.

Features

- Total unadjusted error $<$ ±1/2 LSB
- Linearity error $<$ ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW
- Full military temperature range available

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Control Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Control Inputs (Start, TRI-STATE, Clock, ALE, ADD A, ADD B, ADD C, ADD D, Expansion Control)	−0.3V to + 15V
Operating Temperature Range	
ADC0816CCN, ADC0817CCN	−40°C to +85°C
ADC0816CD	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (at 25°C)	500 mW
Operating V_{CC} Range	4.5V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

ADC0816CCN, ADC0817CCN

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted, (Note 2)

ADC0816CD

$4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA @ T_A = 85°C I_O = −300 μA @ T_A = 125°C	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	Clock Frequency = 500 kHz				
		@ T_A = 85°C		300	1000	μA
		@ T_A = 125°C			3000	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V			3	μA
		V_O = 0	−3			μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic, *(Figure 2)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 2)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage, *(Figure 2)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors, *(Figure 3)*.

Note 7: Quantization error is the ±1/2 LSB uncertainty caused by the converter's finite resolution, *(Figure 3)*.

Note 8: Absolute Accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance, *(Figure 3)*.

Note 9: Supply rejection relates to the ability of an ADC to maintain accuracy as the supply voltage varies. The supply and $V_{REF(+)}$ are varied together and the change in accuracy is measured with respect to full-scale.

Note 10: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence, *(Figure 5)*.

DC Electrical Characteristics (Continued)

ANALOG MULTIPLEXER

ADC0816CCN, ADC0817CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted
ADC0816CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel)				
		$T_A = 25°C$, $R_L = 10k$		1.5	3	kΩ
		$T_A = 85°C$			6	kΩ
		$T_A = 125°C$			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$,		10	200	nA
		$T_A = 25°C$			200	nA
		ADC0816CD @ $T_A = 125°C$			400	nA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$,	−200	−10		nA
		$T_A = 25°C$	−200			nA
		ADC0816CD @ $T_A = 125°C$	−400			nA

CONVERTER SECTION

$CC = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $f_c = 640$ kHz

ADC0816CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted
ADC0816CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/4	±1/2	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	$T_A = 25°C$ (Note 6)		±1/4	±1/2	LSB
	ADC0816CD		±1/4	±1/2	LSB
	ADC0816CCN		±1/4	±3/4	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	$T_A = 25°C$ (Note 8)		±3/4	±1	LSB
	ADC0816CD		±3/4	±1	LSB
	ADC0816CCN		±3/4	±1 1/4	LSB

ADC0817CCN $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/2	±1	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	(Note 6)		±1/2	±1	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	(Note 8)		±1	±1 1/2	LSB

ADC0816CCN $-40°C \leq T_A \leq +85°C$, **ADC0817CCN** $T_A = 25°C$
ADC0816CD $-55°C \leq T_A \leq +125°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection	$4.75V \leq V_{CC} = V_{REF(+)} \leq 5.25V$, (Note 9)		0.05	0.15	%/V
Comparator Input Current	$f_c = 640$ kHz, (Note 10)	−2	±0.5	2	μA
Ladder Resistance	From Ref(+) to Ref(−)	1	4.5		kΩ

DC Electrical Characteristics (Continued)

DESIGN GUIDELINES

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{LAD}	Voltage Across Ladder	From Ref(+) to Ref(−)	0.512	5.12	5.25	V
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2}-0.1$	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V

AC Electrical Characteristics

$T_A = 25°C$, $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{WS}	Start Pulse Width	*(Figure 5)*	200	100		ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*	200	100		ns
t_S	Address Set-Up Time	*(Figure 5)*	50	25		ns
t_H	Address Hold Time	*(Figure 5)*	50	25		ns
t_D	Analog MUX Delay Time From ALE	Common Tied to Comparator In $R_S + R_{ON} \leq 5\ k\Omega$, $C_L = 10\ pF$		1	2.5	μs
t_{H1}, t_{H0}	TRI-STATE Control to Q Logic State	$C_L = 50\ pF$		125	250	ns
t_{1H}, t_{0H}	TRI-STATE Control to Hi-Z	$C_L = 10\ pF$, $R_L = 10k$		125	250	ns
t_C	Conversion Time	$f_C = 640\ kHz$, *(Figure 5)* (Note 11)	90	100	114	μs
f_C	Clock Frequency		10	640	1200	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	1		8	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs At MUX Inputs		10 5	15 7.5	pF pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		5	7.5	pF

Note 11: The outputs of the data register are updated one clock cycle before the rising edge of EOC.
Note 12: Capacitance guaranteed by periodic testing.

Timing Diagram

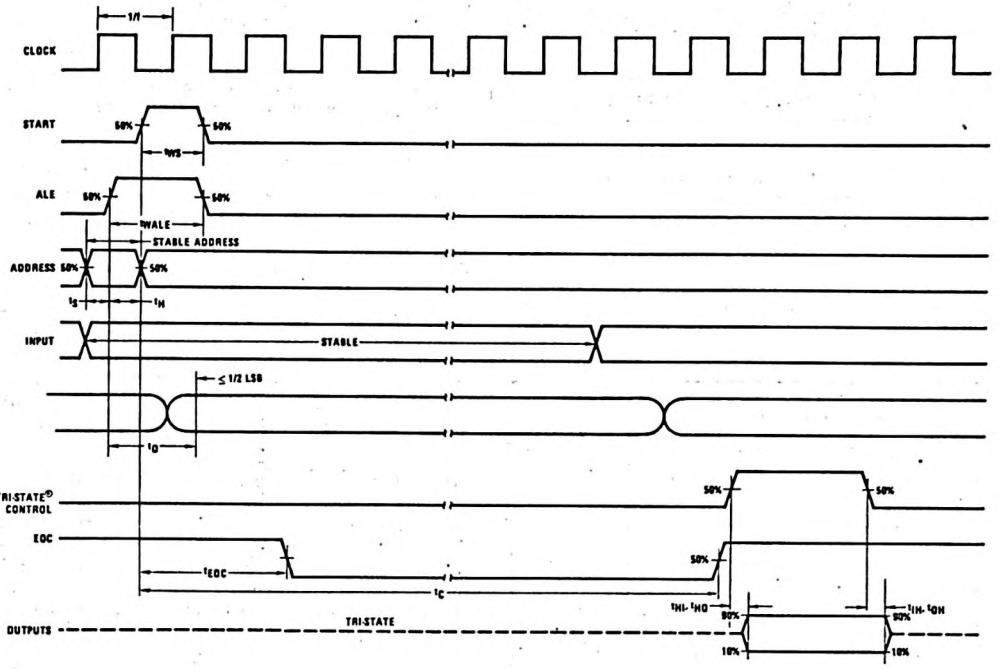


FIGURE 5

Typical Performance Characteristics

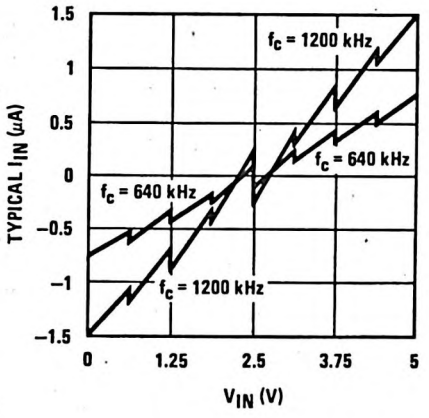


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC} = V_{REF} = 5V)

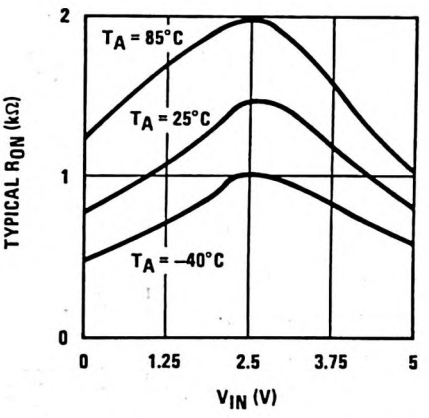


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC} = V_{REF} = 5V)

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

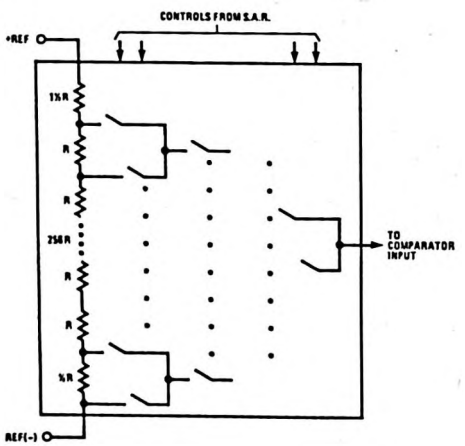


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 1 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179. The characteristic is generated with the analog input signal applied to the comparator input.

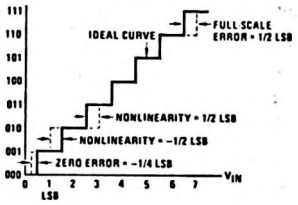


FIGURE 2. 3-Bit A/D Transfer Curve

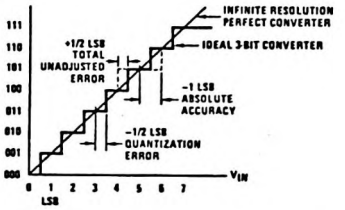


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

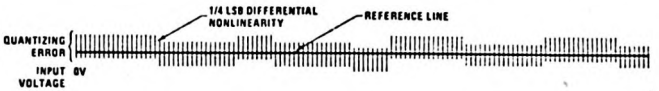
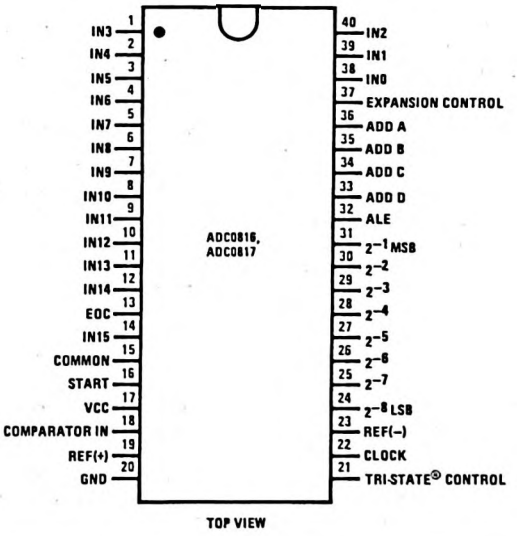


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Applications Information

OPERATION

Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 8)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder Ref(−) should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 9 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 10* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 11*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 12*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = V_{REF(+)} \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE} \quad (2)$$

The center of an output code N is given by:

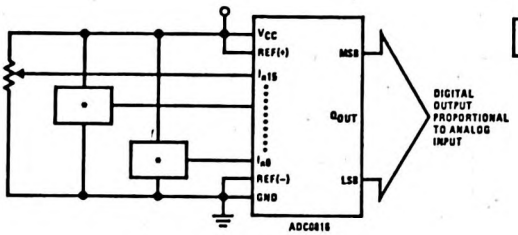
$$V_{IN} = V_{REF(+)} \left[\frac{N}{256}\right] \pm V_{TUE} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN}}{V_{REF(+)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = GND
V_{TUE} = Total unadjusted error voltage(typically $V_{REF(+)}/512$)

Applications Information (Continued)

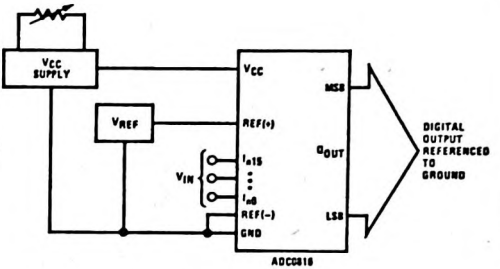


$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

*Ratiometric transducers

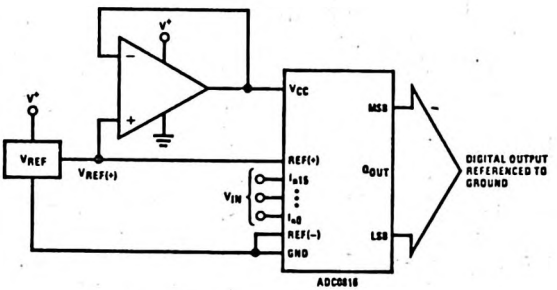
FIGURE 8. Ratiometric Conversion System



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 9. Ground Referenced Conversion System Using Trimmed Supply



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 10. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

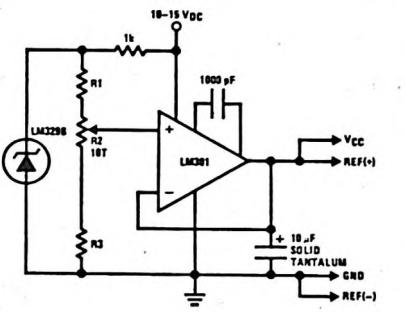
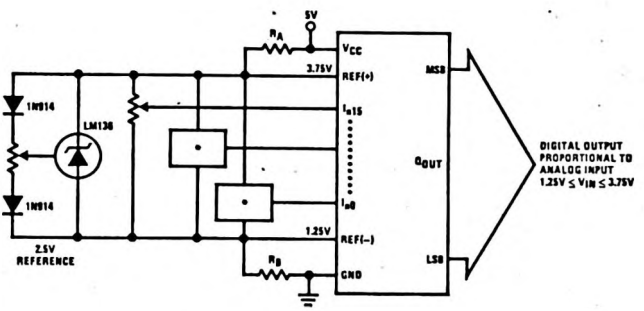


FIGURE 11. Typical Reference and Supply Circuit

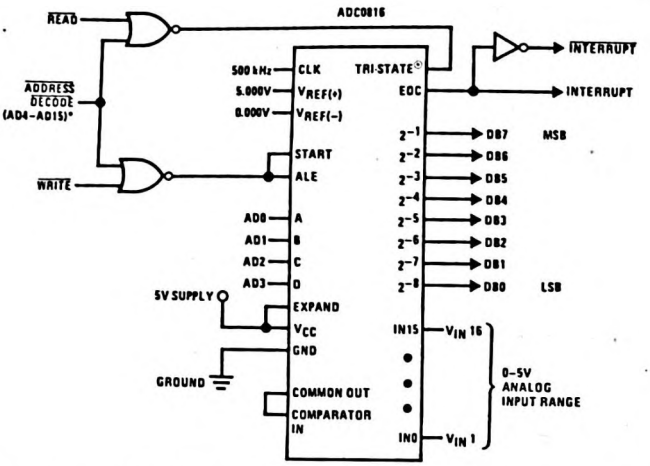


$R_A = R_B$

*Ratiometric transducers

FIGURE 12. Symmetrically Centered Reference

Typical Application



*Address latches needed for 8085 and SC/MP interfacing the ADC0816 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z–80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA · Φ2 · R/W	VMA · Φ2 · R/W	IRQA or IRQB (Thru PIA)

Ordering Information

ORDER NUMBER	TEMPERATURE RANGE	25°C TOTAL UNADJUSTED ERROR	SEE NS PACKAGE NUMBER
ADC0816CD	−55°C to +125°C	±1/2 LSB	D40D
ADC0816CCN	−40°C to +85°C	±1/2 LSB	N40A
ADC0817CD	−55°C to +125°C	±1 LSB	D40D
ADC0817CCN	−40°C to +85°C	±1 LSB	N40A

National Semiconductor

Analog-to-Digital Converters

ADC1210, ADC1211 12-Bit CMOS A/D Converters

general description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

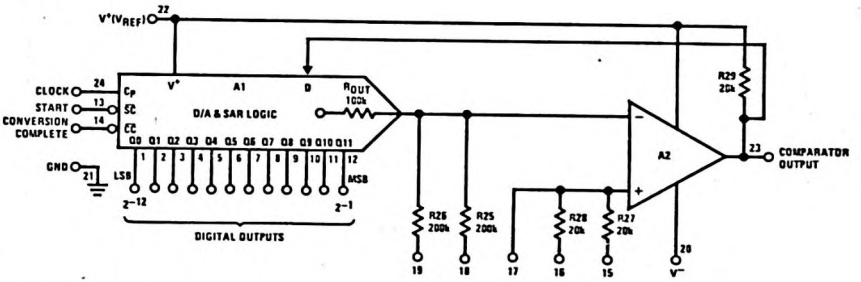
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

features

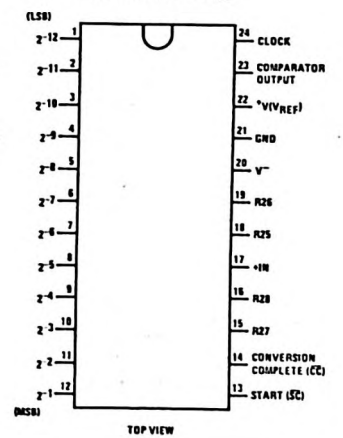
- 12-bit resolution
- ±1/2 LSB linearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance
- Low cost

block diagram



connection diagram

Dual-In-Line Package



absolute maximum ratings

Maximum Reference Supply Voltage (V^+)	16V
Maximum Negative Supply Voltage (V^-)	−20V
Voltage At Any Logic Pin	$V^+ + 0.3V$
Analog Input Voltage	±15V
Maximum Digital Output Current	±10 mA
Maximum Comparator Output Current	50 mA
Comparator Output Short-Circuit Duration	5 Seconds

Power Dissipation	See Curves
Operating Temperature Range	
ADC1210HD, ADC1211HD	−55°C to +125°C
ADC1210HCD, ADC1211HCD	−25°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	ADC1210			ADC1211			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error	(Note 3)							
	f_{CLK} = 65 kHz, T_A = 25°C			±0.0122			±0.0488	% FS
	f_{CLK} = 65 kHz			±0.0244				% FS
Full Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Zero Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.1			0.1	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	V_{IN} = 10.24V			1			1	μA
Logic "0" Input Current	V_{IN} = 0V			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT} \leq -1$ μA	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT} \leq 1$ μA			0.5			0.5	V
Positive Supply Current	V^+ = 15V, f_{CLK} = 65 kHz, T_A = 25°C		5	8		5	8	mA
Negative Supply Current	V^- = −15V, T_A = 25°C		4	6		4	6	mA

ac electrical characteristics T_A = 25°C, (Notes 1 and 2)

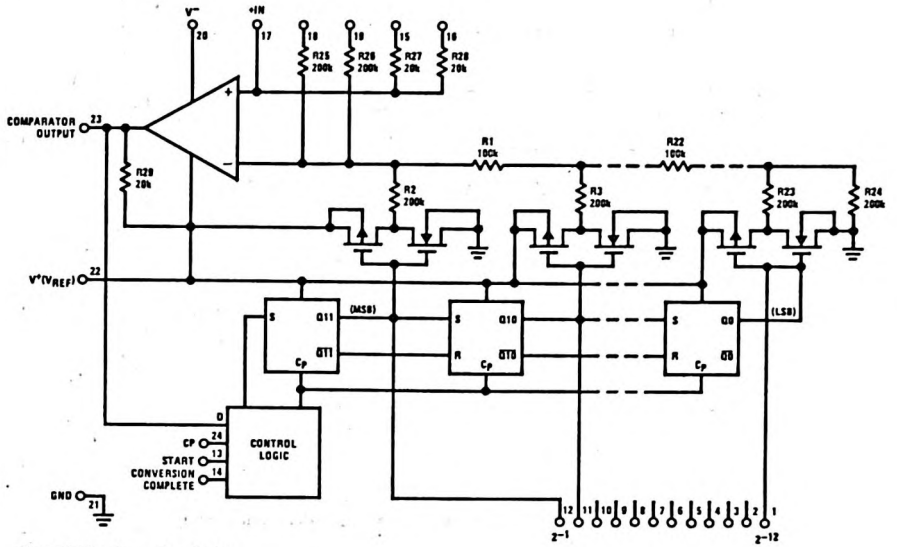
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Maximum Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output (Q0 to Q11)	$t_r \leq t_f \leq 10$ ns		60	150	ns
Propagation Delay From Clock to Conversion Complete	$t_r \leq t_f \leq 10$ ns		60	150	ns
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

Note 1: Unless otherwise noted, these specifications apply for V^+ = 10.240V, V^- = −15V, over the temperature range −55°C to +125°C for the ADC1210HD, ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.

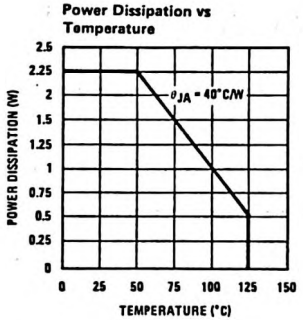
Note 2: All typical values are for T_A = 25°C.

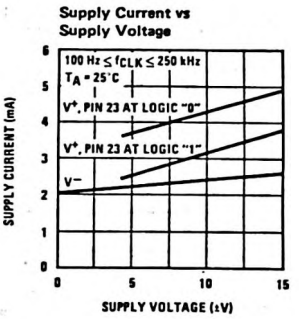
Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a*.

schematic diagram



Note: 3 bits shown for clarity




Supply Current vs Supply Voltage
100 Hz ≤ fCLK ≤ 250 kHz
TA = 25°C
V⁺, PIN 23 AT LOGIC "0"
V⁺, PIN 23 AT LOGIC "1"
V⁻
SUPPLY CURRENT (mA)
SUPPLY VOLTAGE (±V)

applications information

THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit, Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V^+ = 10.240V, V^- = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

applications information (Continued)

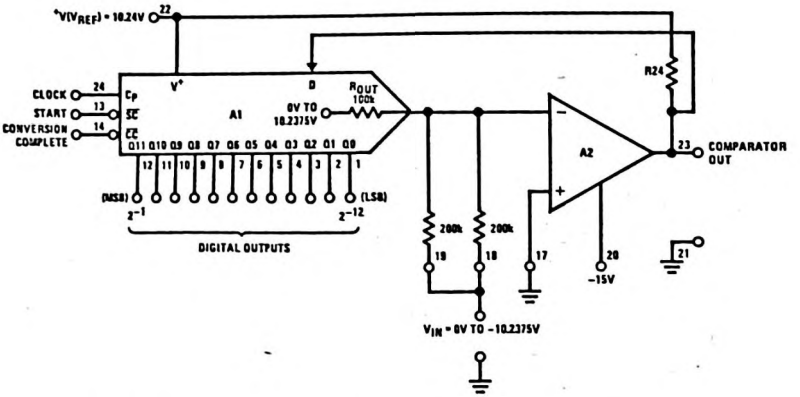


FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)

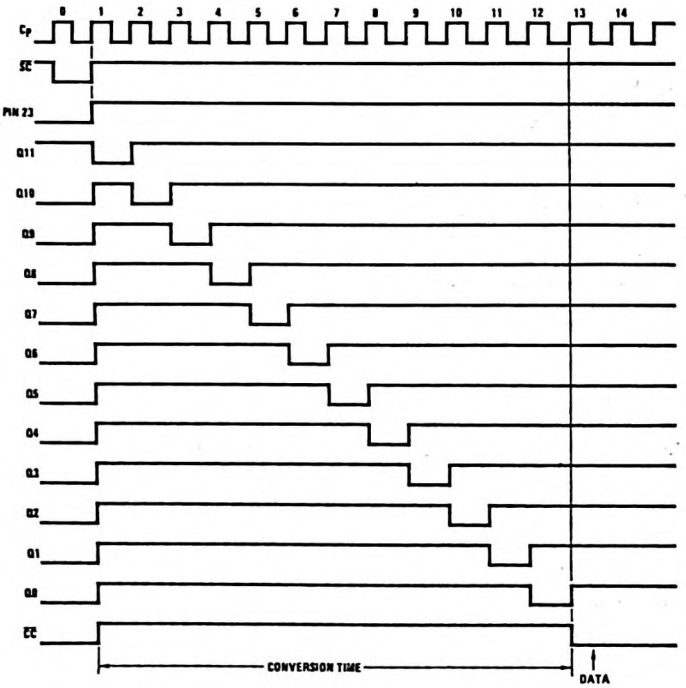


FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

applications information (Continued)

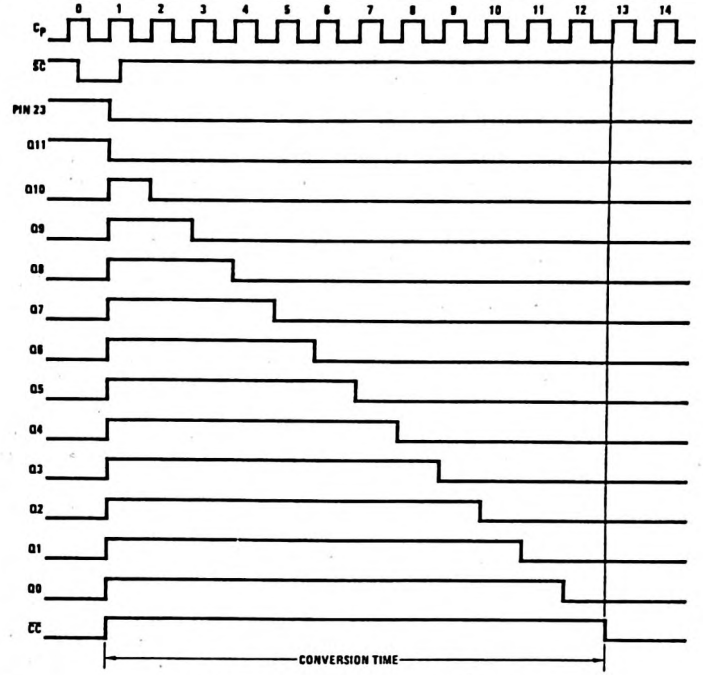


FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

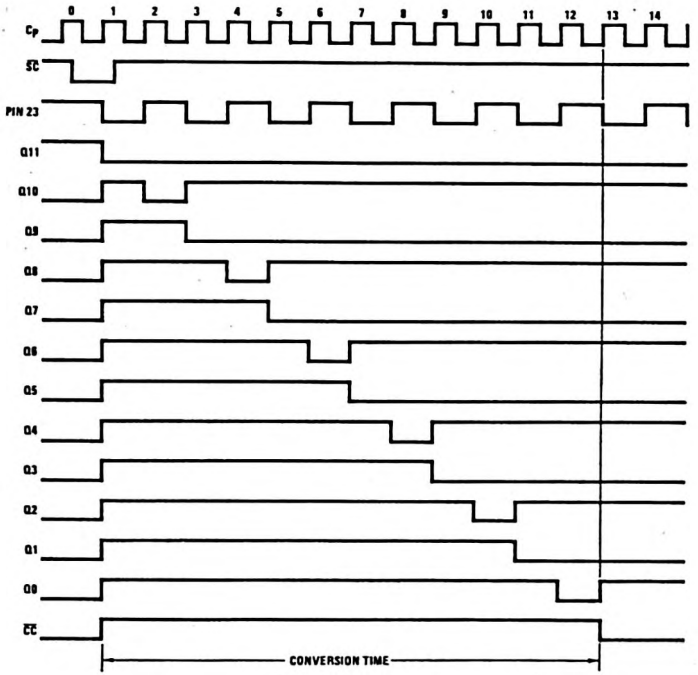


FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

applications information (Continued)

TABLE I. Pin Assignments and Explanations

PIN NUMBER	MNEMONIC	FUNCTION
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V^+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V^+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V^+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V^-	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	$V^+(V_{REF})$	V^+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	C_P	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V^+.

POWER SUPPLY CONSIDERATIONS AND DECOUPLING

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V^+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V^+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V^+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V^- supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

SHORT CYCLE FOR IMPROVED CONVERSION TIME (FIGURE 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

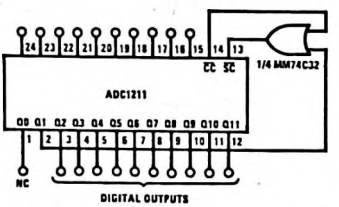


FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

LOGIC COMPATIBILITY

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4.*

OPERATING CONFIGURATIONS

Several recommended operating configurations are shown in *Figure 5.*

applications information (Continued)

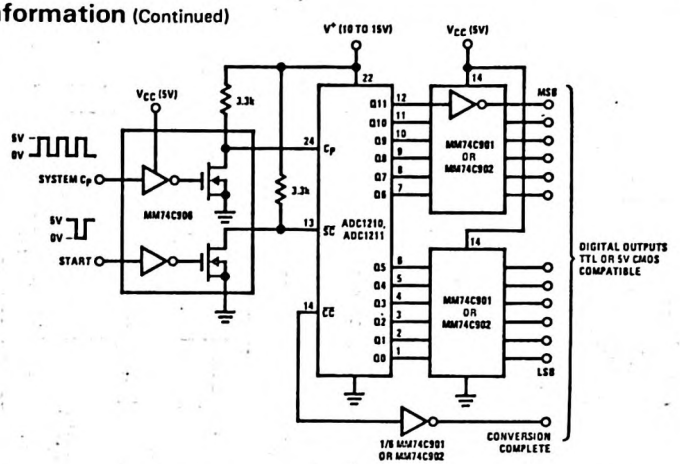


FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$

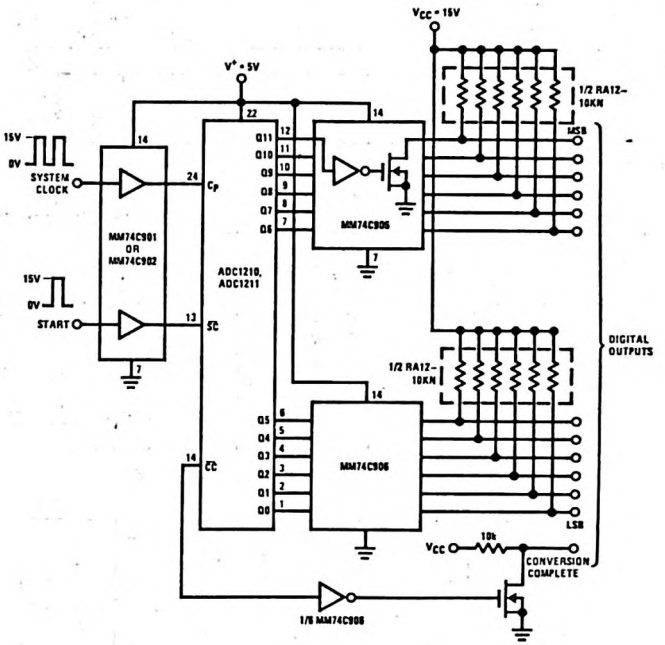


FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

OFFSET AND FULL SCALE ADJUST

A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp (e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to 1/2 LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19.

applications information (Continued)

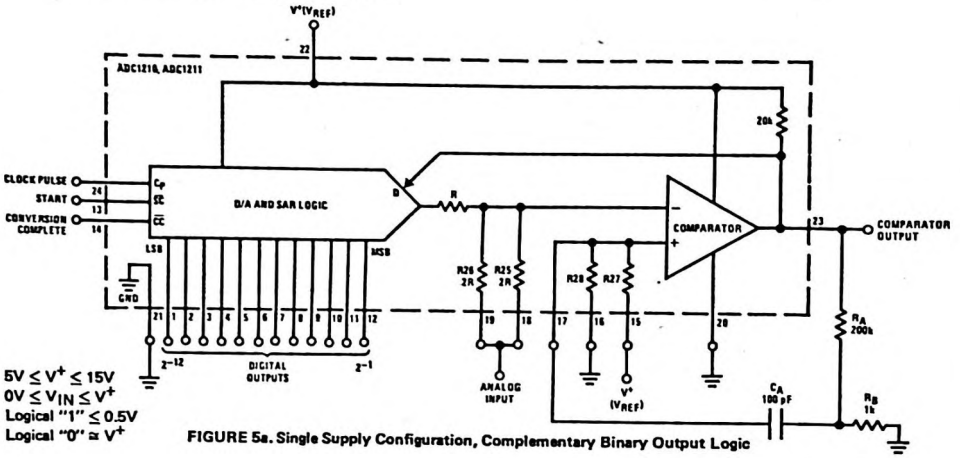


FIGURE 5a. Single Supply Configuration, Complementary Binary Output Logic

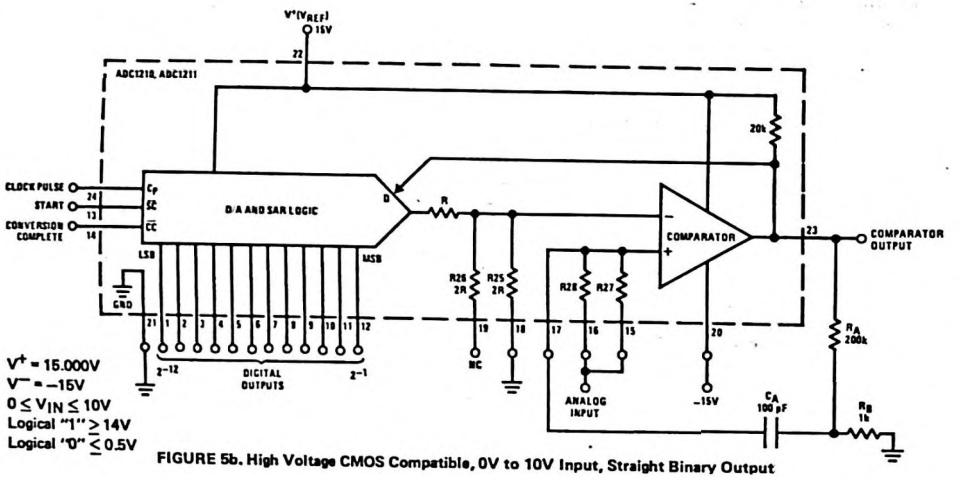


FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input, Straight Binary Output

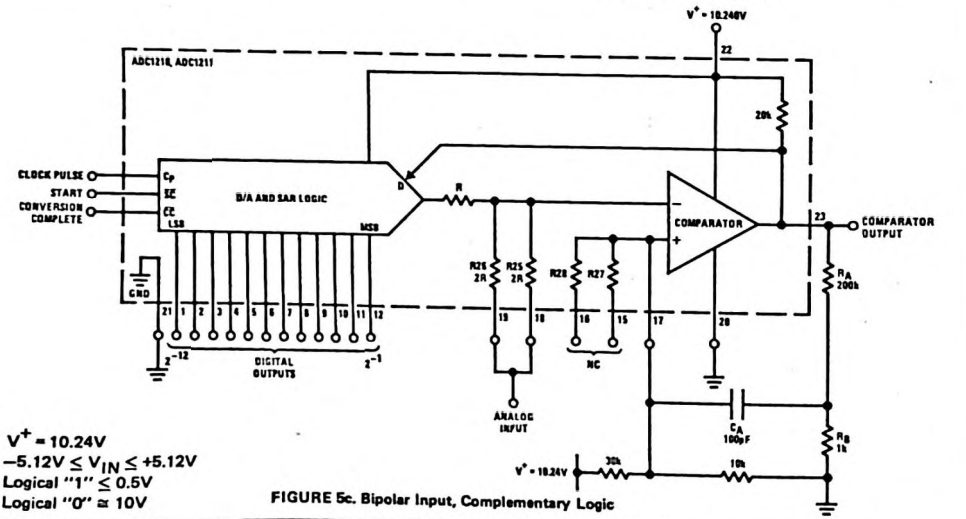


FIGURE 5c. Bipolar Input, Complementary Logic

applications information (Continued)

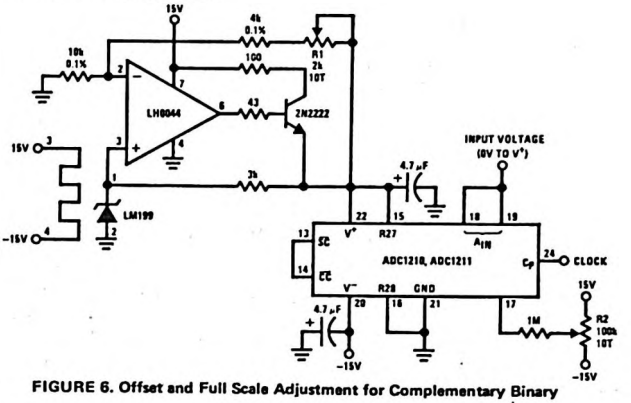


FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".

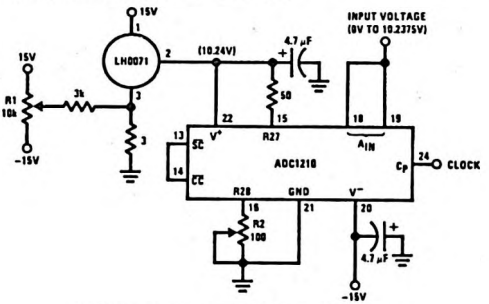


FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 8*.

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to

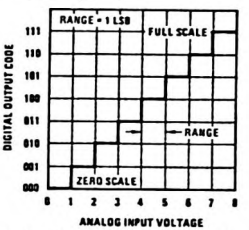


FIGURE 8. Quantization Uncertainty of a Perfect 3-Bit A/D

offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB as shown in *Figure 9*. Rather than +1, −0 bit shown in *Figure 8*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

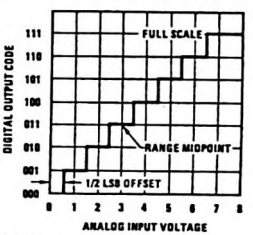


FIGURE 9. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. The Linearity Error of the ADC1210 is guaranteed to be less than ±1/2 LSB or ±0.0122% of FS and ±0.0488% of FS for the AD1211. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (or Offset): Zero Scale Error is a measure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 10*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition

applications information (Continued)

takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 10*, the offset is 2 LSB's or 0.286% of FS.

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 11*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 11*, Full Scale Error is 1 1/2 LSB's, or 0.214% of FS.

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in the Applications section.

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than ±1/2 LSB. This places a maximum slew rate of 12.5 μV/μs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. See AN-154 for additional information.

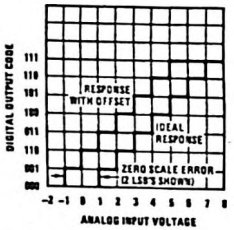


FIGURE 10. A/D Transfer Characteristic with Offset

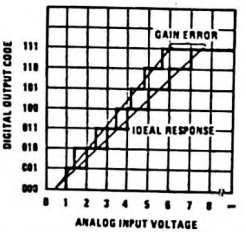


FIGURE 11. Full Scale (Gain Error)

ordering information

PART NUMBER	OPERATING TEMPERATURE RANGE	25°C LINEARITY
ADC1210HD, ADC1210HN	−55°C to +125°C	0.01%
ADC1210HCD, ADC1210HCN	−25°C to +85°C	0.01%
ADC1211HD, ADC1211HN	−55°C to +125°C	0.05%
ADC1211HCD, ADC1211HCN	−25°C to +85°C	0.05%

See NS Package D24A or N24A

National Semiconductor

Analog-to-Digital Converters

ADC3511 3½-Digit Microprocessor Compatible A/D Converter
ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937-1, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

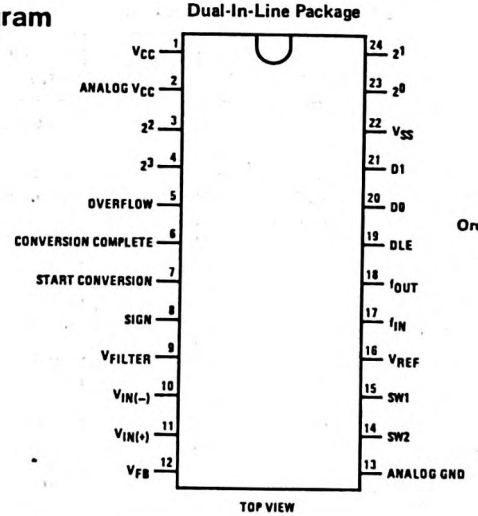
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number ADC3511CCN
or ADC3711CCN
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics ADC3511CC, ADC3711CC

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		V_{CC}−0.6			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except $2^0, 2^1, 2^2, 2^3$)	I_O = 360μA	V_{CC}−0.4			V
$V_{OUT(1)}$	Logical "1" Output Voltage ($2^0, 2^1, 2^2, 2^3$)	I_O = 360μA	V_{CC}−1.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	V_{IN} = V_{CC}		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

V_{CC} = 5V; T_A = 25°C; C_L = 50 pF; t_r = t_f = 20 ns; unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC		f_{IN}/64,512		conversions/sec
		ADC3711CC		f_{IN}/129,024		conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to $2^0, 2^1, 2^2, 2^3$	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to $2^0, 2^1, 2^2, 2^3$			2.0	5.0	μs
t_{SET-UP}	Set-Up Time D0, D1, to DLE	t_{HOLD} = 0 ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

Converter Characteristics ADC3511CC, ADC3711CC $4.75V \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A \leq +85°C$, f_C = 5 conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	V_{IN} = 0–2V Full Scale V_{IN} = 0–200 mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	V_{IN} = 0V	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	−5	±1	+5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

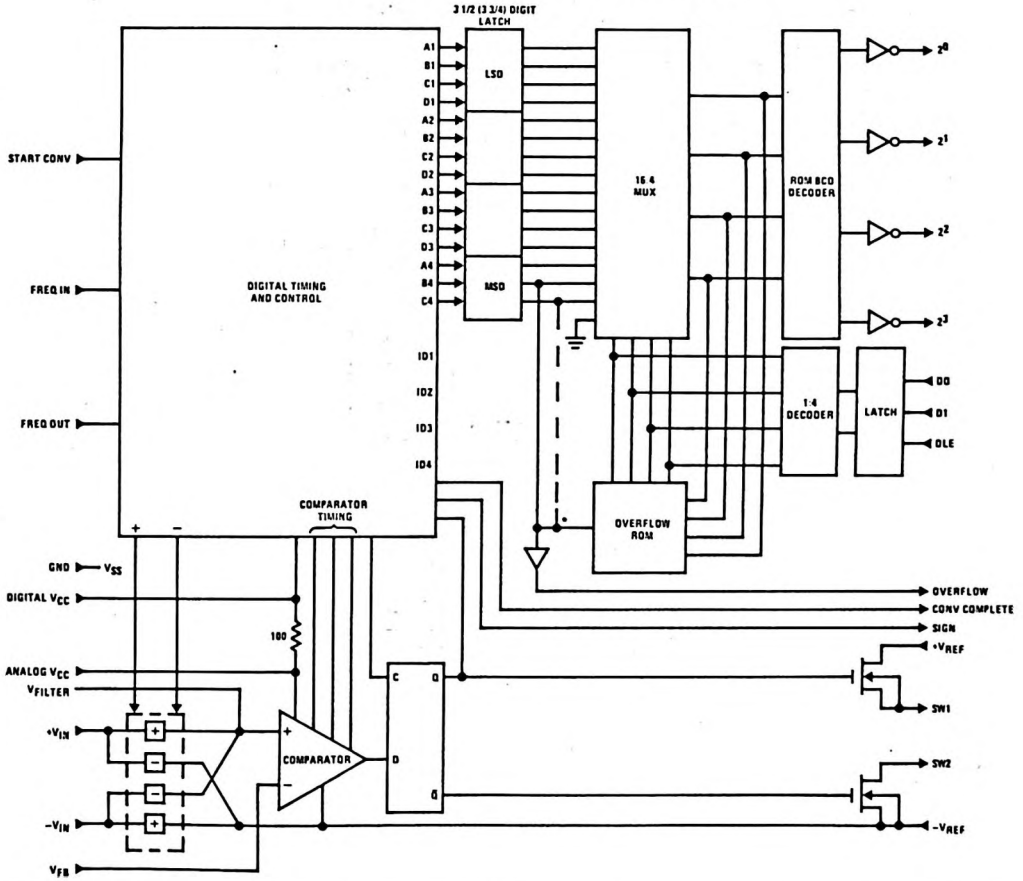
Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = 1/2 count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Block Diagram

ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D)



Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level V_{OUT} = 0V. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

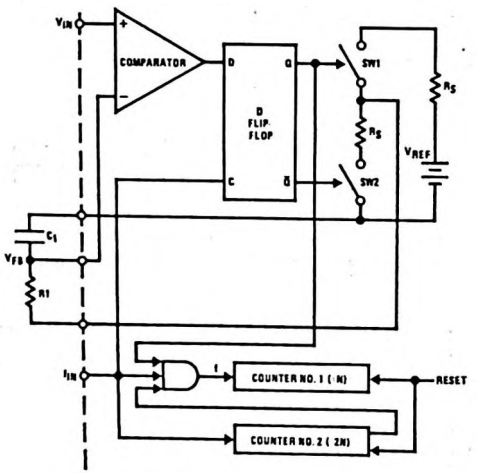
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in counter no. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 x $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$ on the ADC3511, or 128 x $1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ (129,024 x $1/f_{IN}$ for the ADC3711) and the minimum time is 256 x $1/f_{IN}$ (512 x $1/f_{IN}$ for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

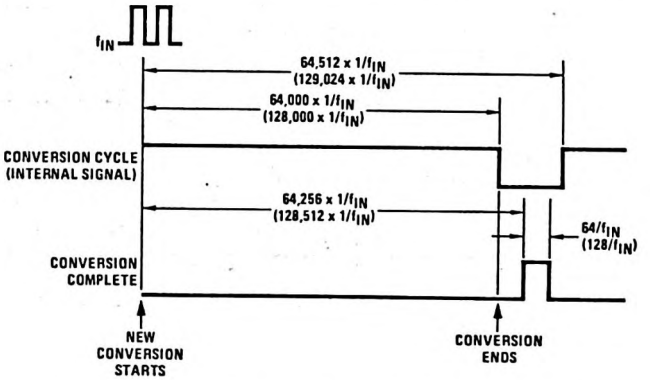


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

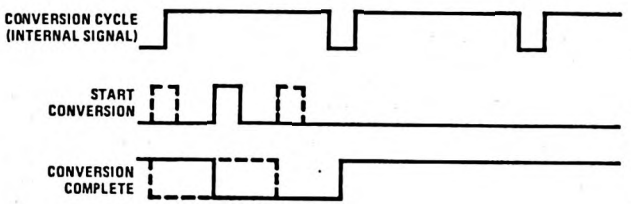


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = Low logic level
H = High logic level
X = Irrelevant logic level

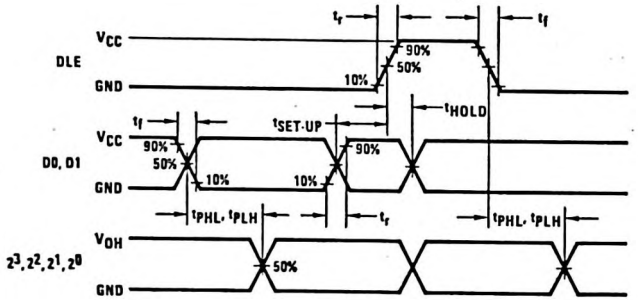
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



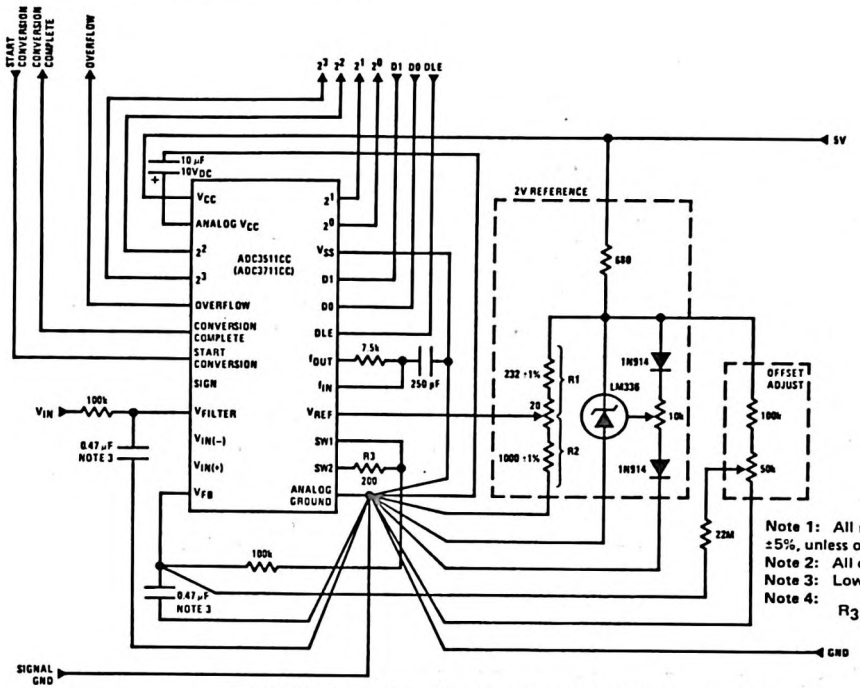
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6.*

Figures 5 and 6 show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

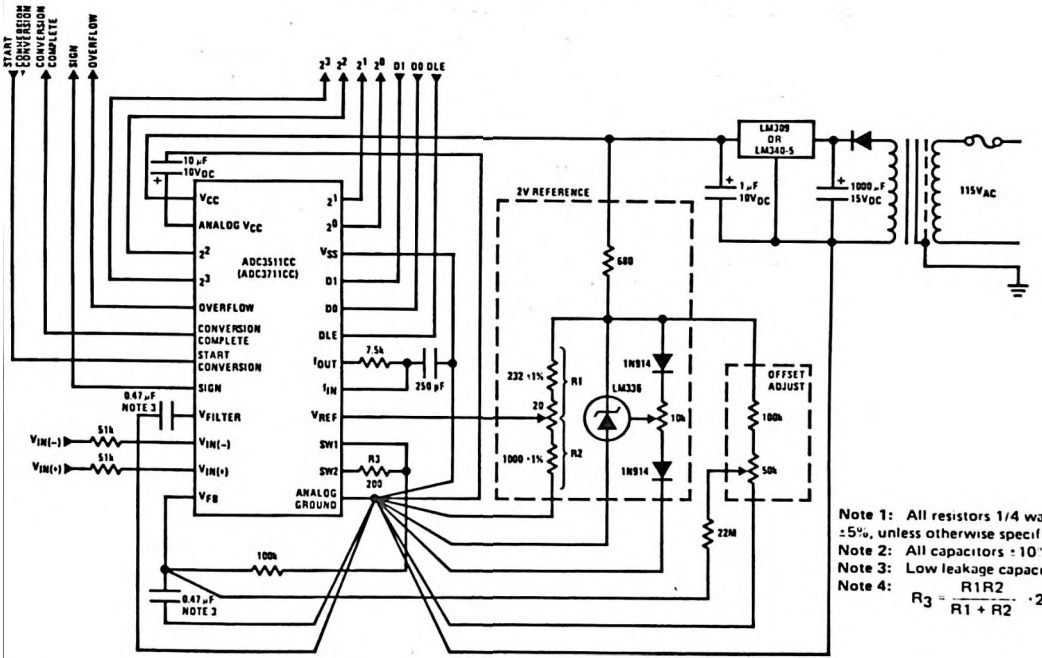
The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error (1.0×10^{-9} A x 100 kΩ = 0.1 mV). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications (Continued)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$

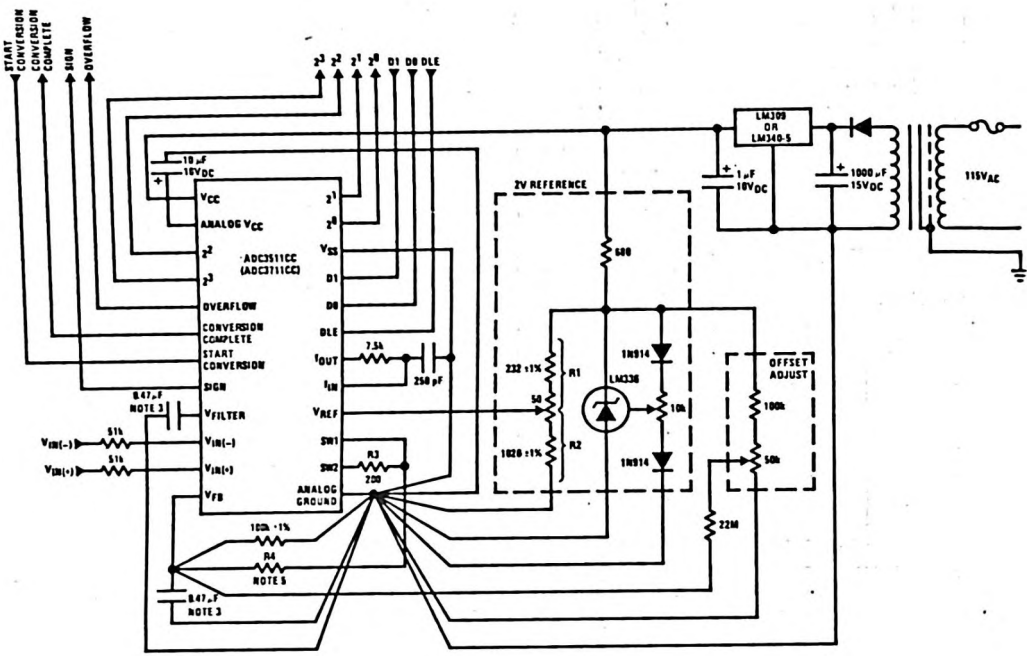
FIGURE 4. 3 1/2-Digit A/D; +1999 Counts, +2.000 Volts Full Scale (3 3/4-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$

FIGURE 5. 3 1/2-Digit A/D; ±1999 Counts, ±2.000 Volts Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±2.000 Volts Full Scale)

Typical Applications (Continued)

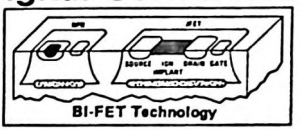


Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$.
Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.
R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

FIGURE 6. 3 1/2-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor

Analog-to-Digital Converters



LF13300 Integrating A/D Analog Building Block

General Description

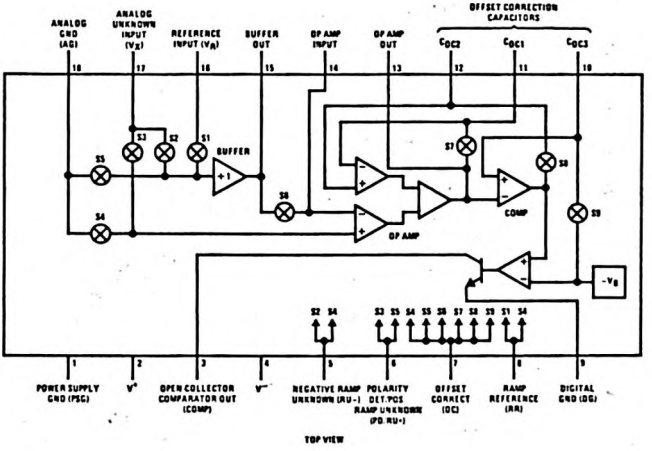
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with either the ADB4511 DPM digital building block or the ADB1200 (MM5863)* 12-bit binary building block.

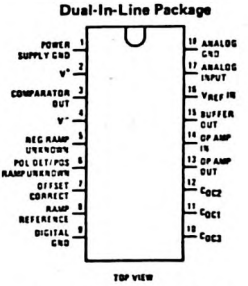
*See ADB1200 (MM5863) data sheet for more information.

Features

- Rugged JFETs allow blow-out free handling
- High input impedance 10,000 MΩ typ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams





Order Number LF13300D
See NS Package D18A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation, (Note 1)	570 mW
Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

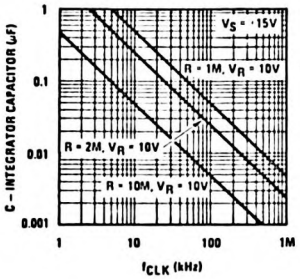
Electrical Characteristics (V_S = ±15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	TEST CIRCUIT	LF13300 MIN	LF13300 TYP	LF13300 MAX	UNITS
Analog Input Current, I_{IN}	V_X = 0	1, 2		80	500	pA
	$T_{MIN} \leq T_A \leq T_{MAX}$				5	nA
	V_X = ±11V				10	nA
Analog Input Voltage Range		1, 2			±11	V
Analog Input Resistance	V_X = 0	1, 2		10,000		MΩ
Reference Input Currents, I_R	V_R = 10V			0.1	100	nA
	$T_{MIN} \leq T_A \leq T_{MAX}$	3			10	μA
	V_R = 11V				10	μA
Reference Input Voltage Range		3	0		11	V
Reference Input Resistance	V_R = 10V	3		1000		MΩ
Offset Correction Voltage, $-V_B$		4		−12		V
Offset Correction		5		20	2000	pA
Input Current, I_{OC}	$T_{MIN} \leq T_A \leq T_{MAX}$	5			20	nA
Op Amp Slew Rate		6		10		V/μs
Op Amp Bandwidth		7		3		MHz
Buffer Slew Rate		9		25		V/μs
Comparator Response Time	200 μV Input Stop, 100 μV Overdrive	11		2.5		μs
Comparator Output Saturation Voltage	V_{CC} = 5V, R_L = 2k, $T_{MIN} \leq T_A \leq T_{MAX}$	11		0.25	0.4	V
Logic "1" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		2.0		5.0	V
Logic "0" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		−2.0		0.8	V
Logic Input Current	All Switching Input Pins 5, 6, 7, 8, $0 \leq V_L \leq 5V$, $T_{MIN} \leq T_A \leq T_{MAX}$			15	50	μA
Power Supply Voltage Range ±V_S	$V_R \leq V^+ - 3V$, V_{IN} = 0V		±4.75		±18	V
Power Supply Current				3.0		mA
				−5.5		mA
	$T_{MIN} \leq T_A \leq T_{MAX}$				±11	mA

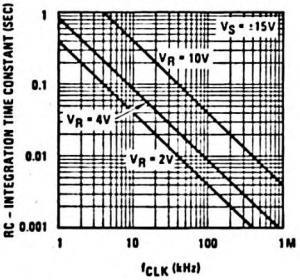
Note 1: For operating at elevated temperatures, the LF13300 in the dual-in-line package must be derated based on the thermal resistance of 100°C/W junction to ambient.

Typical Performance Characteristics

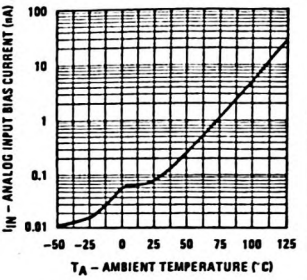
Integrator Capacitance, C vs f_{CLK} for Different Integrator Resistances, R



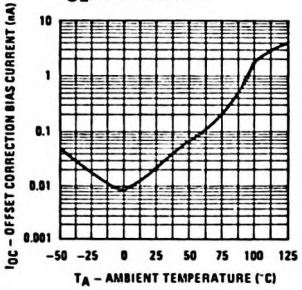
Integration Time Constant (RC) vs f_{CLK} for Different Reference Voltages, V_R



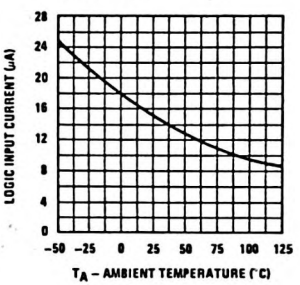
Analog Input Bias Current, I_{IN}, V_X = 0V, vs Temperature



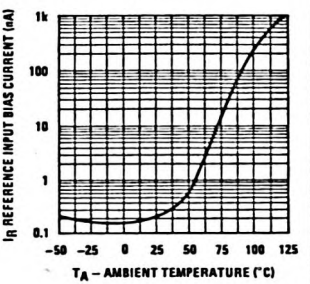
Offset Correction Bias Current, I_{OL}, vs Temperature



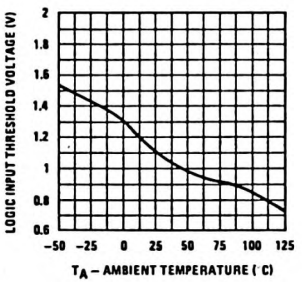
Logic Input Current vs Temperature



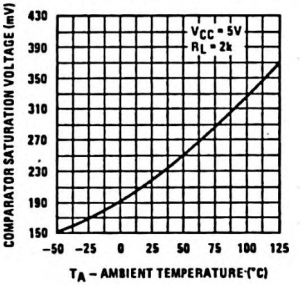
Reference Input Bias Current, I_R, vs Temperature



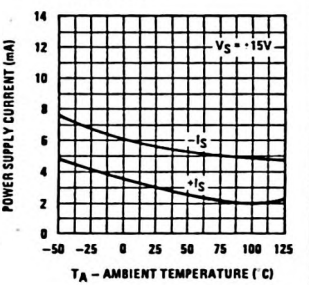
Logic Input Threshold Voltage vs Temperature



Comparator Saturation Voltage vs Temperature



Power Supply Current vs Temperature



Functional Description

The LF13300 goes through the following 5 states during normal cycle: 1) Offset Correction; 2) Polarity Determination; 3) Initialization; 4) Ramp Unknown; 5) Ramp Reference

Offset Correction Description *(Figure 1)*

The Offset Correction scheme will drive the input of the comparator to its switching threshold when the analog input is zero and the timing components, RC, are bypassed.

The Offset Correction input (OC) is driven high, closing switches S4–S9.

The offset voltages are assigned as follows: V_{OS1} – the input offset voltage of the buffer; V_{OS2} – the input offset voltage of A1; V_{OS3} – the input offset voltage of A2; V_{OS4} – the input offset voltage of the comparator.

S5 grounds the input of the buffer so that its output voltage is simply V_{OS1}. S6 bypasses R to keep the integration time constant, RC, from affecting the circuit operation. S4 makes the total equivalent input voltage to A1 be $-V_{OS1} - V_{OS2}$. S7 puts the op amp in a unity gain configuration with respect to the input of A2. S8 keeps the output voltage of the op amp at $-V_B + V_{OS4} = -V_B'$ (the Offset Correction potential) since the comparator is placed inside the loop. C3 samples the output of the $-V_B$ generator. The voltage at the non-inverting input of A2 is $-V_B - V_{OS1} -$

Functional Description (Continued)

$V_{OS2} - V_{OS3} + V_{OS4} = V1$. Thus, the sum of the offsets is stored on C1, and the differential voltage across the comparator is zero.

Polarity Determination *(Figure 2)*

The simplified diagram of the LF13300 in the Polarity Determination state is shown in *Figure 2*. S5 and S3 are closed during this period. S5 grounds the buffer input and V_X (the unknown voltage) is applied through S3 to the non-inverting input of A1. The equation that describes the op amp output voltage is given in *Figure 2*. When V_X is applied to A1 at t_1, the output of the op amp slews to V_X and is integrated until t_2, when S3 opens and S4 closes. At t_2, V_{OUT} slews down by $-V_X$

leaving $\frac{1}{RC}\int_{t_2}^{t_2} V_X dt - V_B'$ at the op amp output.

Just before t_2, the comparator senses the op amp output with respect to $-V_B$; the comparator output goes high if $V_X > 0$ and remains low if $V_X \leq 0$.

Initialization *(Figure 1)*

During initialization, the configuration is the same way as it is in the Offset Correction state and the op amp output is brought back to the Offset Correction potential $-V_B'$.

Ramp Unknown *(Figures 2 and 3)*

In the Ramp Unknown state, if $V_X \geq 0$, S3 and S5 are closed, as shown in *Figure 2*, and V_X is applied to the + input of the integrator. If $V_X < 0$, the device is connected as in *Figure 3* with S2 and S4 closed. V_X is now applied through the buffer to the − input of the integrator. In either Ramp Unknown case, the op amp output ramps in the positive direction and V_X is applied to a high impedance JFET input.

Ramp Reference *(Figure 4)*

In this state, the LF13300 is configured with switches S1 and S4 closed. The reference voltage, V_R, a positive voltage, is applied to the buffer input and the op amp output ramps down until $V_{OUT} = -V_B'$ where the comparator will trip.

If V_X and V_R are assumed to be constant over their respective integration periods, the integrals of *Figure 4* are reduced to,

$$\frac{V_X(t_4 - t_3)}{RC} = \frac{V_R(t_5 - t_4)}{RC}$$

or

$$\frac{V_X}{V_R} = \frac{t_5 - t_4}{t_4 - t_3}$$

Since $t_4 - t_3 = 4096$ clock periods and $t_5 - t_4$ can be measured in clock periods, $V_X/V_R = X/2^{12}$, where X is a digital binary output representing an analog input V_X with respect to V_R.

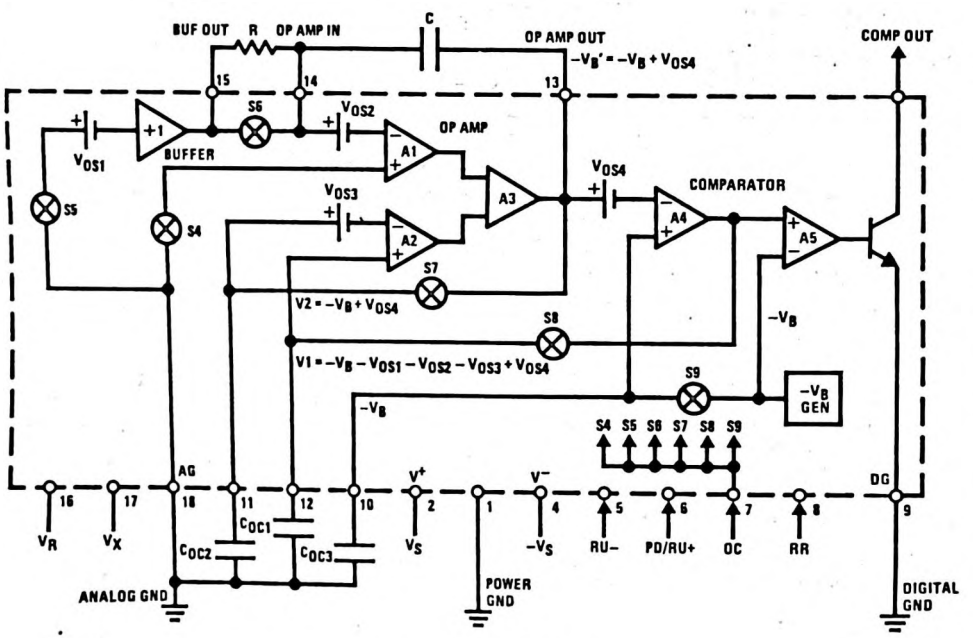


FIGURE 1. Offset Correction Circuit

Functional Description (Continued)

$$V_{OUT} = \begin{cases} -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X \geq 0 \\ -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_1}^{t_2} V_X\,dt: \text{Polarity Determination} \end{cases}$$

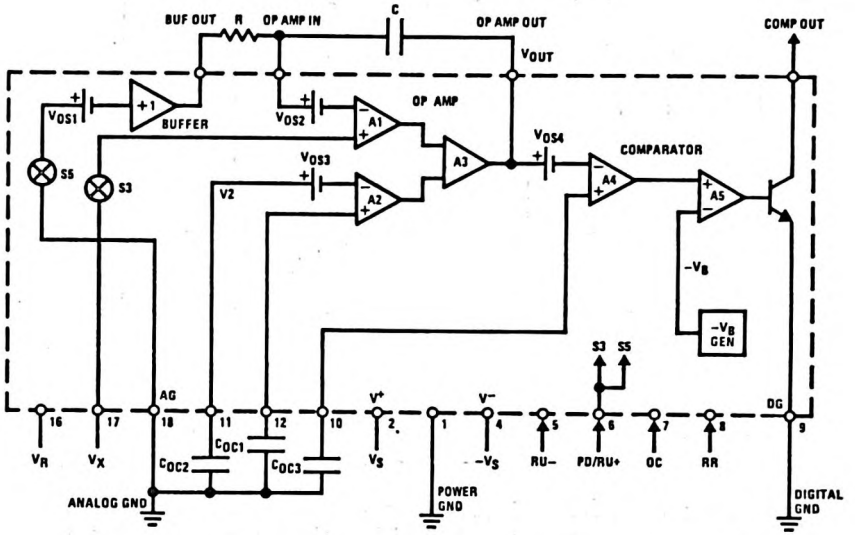


FIGURE 2. Polarity Determination Circuit or Ramp Unknown Circuit for $V_X \geq 0$

$$V_{OUT} = -V_B' + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X < 0$$

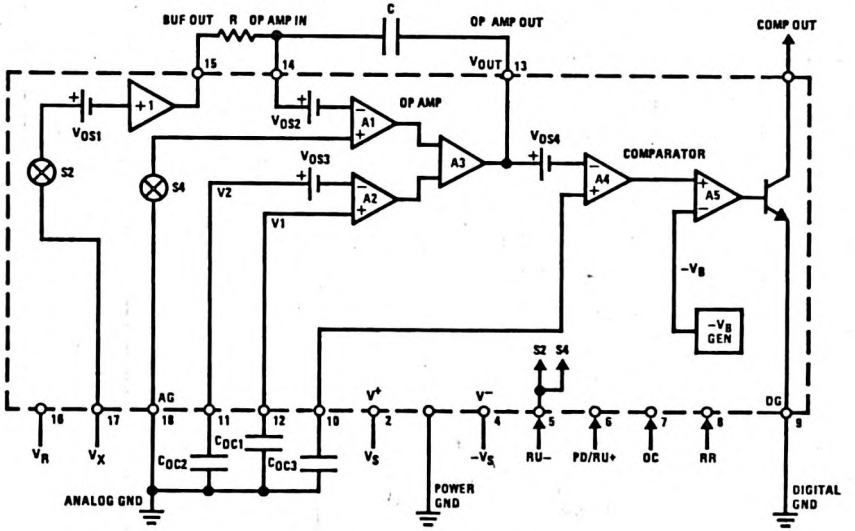
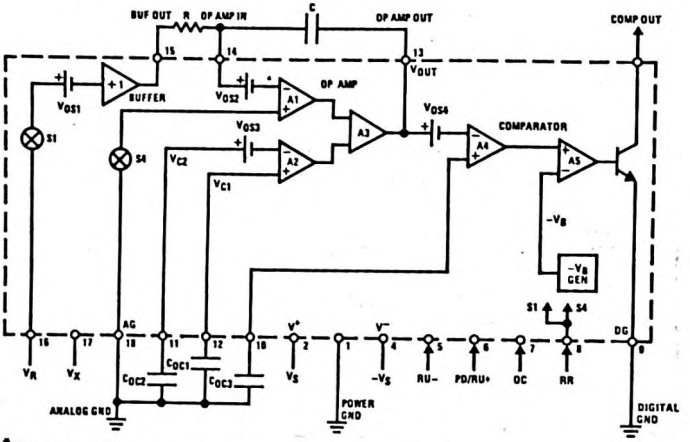


FIGURE 3. Ramp Unknown for $V_X < 0$

Functional Description (Continued)

$$V_{OUT}^{*} = -V_B' + \frac{1}{RC}\left(\int_{t_3}^{t_4} V_X\,dt - \int_{t_4}^{t_5} V_R\,dt\right)$$



*More accurately

$$V_{OUT} = -V_B' + \frac{1}{RC}\left(\int_{t_4}^{t_5+\Delta} V_R\,dt + \int_{t_3}^{t_4} V_X\,dt\right) + \delta$$

Where δ is the incremental voltage overdrive needed to fully switch the comparator and Δ is the sum of the additional time required to develop δ and the comparator propagation delay.

FIGURE 4. Ramp Reference Circuit

12-Bit A/D Converter Electrical Characteristics

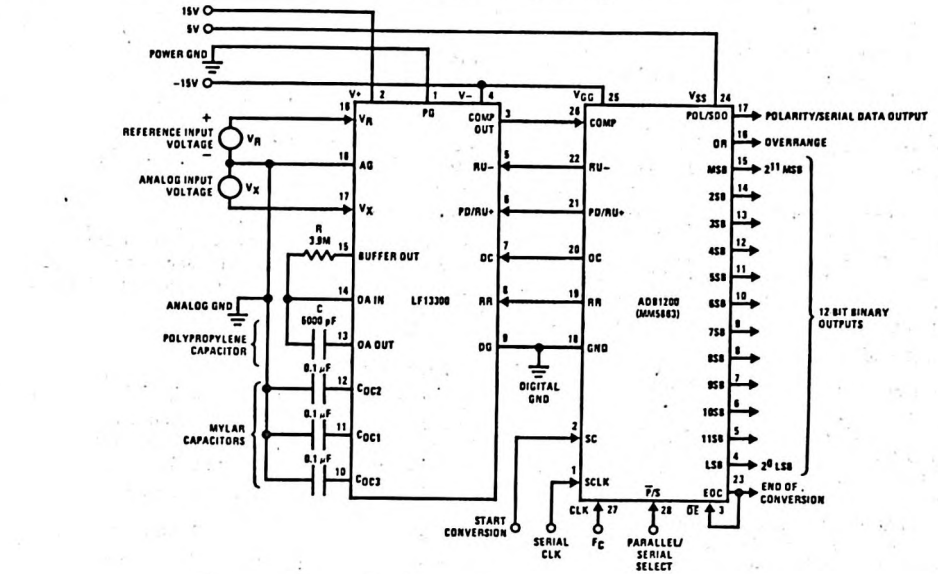
12-bit plus sign. (LF13300 with ADB1200 (MM5863)). (V_R = 10.000V, F_C = 250 kHz, 0°C ≤ T_A ≤ +70°C unless otherwise noted.)

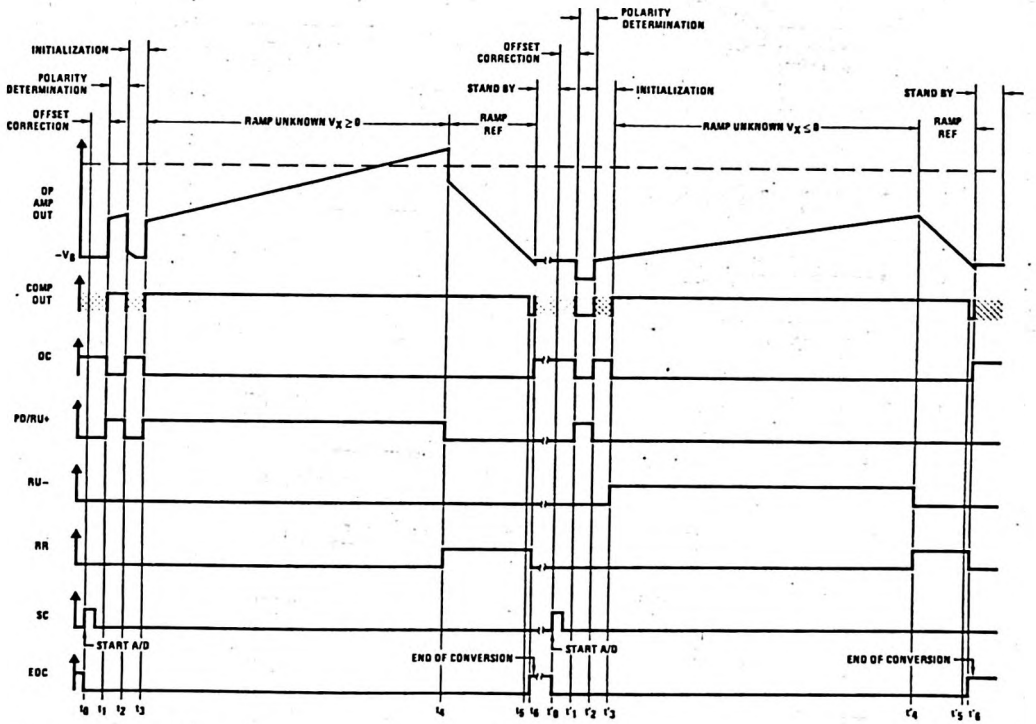
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (Note 3)	V_R = 5.000V, −10V ≤ V_X ≤ +10V	13			Bits
	F_C = 125 kHz, T_A = 25°C	14			Bits
Non-Linearity			±1/8	±1/2	LSB
Ratiometric Gain Error (Def.)	V_X = ±10.000V, T_A = 25°C, (Note 2)		±1/2	±2	LSB
Gain Error Drift	V_X = 10.000V		±1		ppm/°C
Zero Reading Drift	V_X = 0V		±0.5		ppm/°C
Analog Input Voltage Range		±11	±12		V
Analog Input Leakage Current	V_X = 0V, T_A = 25°C		80	500	pA
Analog Input Resistance	V_X = 0V, T_A = 25°C	100	1000		MΩ
Reference Input Voltage Range	V_R Varied, T_A = 25°C	4		12	V
Reference Input Leakage Current	V_R = 10.000V, T_A = 25°C		0.1	100	nA
Reference Input Resistance	V_R = 10.000V, T_A = 25°C	100	1000		MΩ
Start Conversion Pulse Width	V_{SC} = 2.4V	2.4			μs
Conversion Time	V_{IN} = 10.000V t_c = 8960/F_C			36	ms
15V Supply Currents	LF13300, V^+ Current			11	mA
−15V Supply Currents	LF13300, V^- Current, ADB1200 (MM5863), V_{GG} Current		27	45	mA
5V Supply Currents	V_{IN} = 0V, ADB1200 (MM5863), V_{SS} Current		23	39	mA

Note 2: The A/D converter system must have been operational for a minimum of 30 seconds before this measurement is made. This is to relax the dielectric absorption effects of the integration capacitor, C.

Note 3: Polarity and Overrange outputs are considered as additional output bits.

12-Bit A/D Converter Circuit and Timing Diagrams





*Note. All TTL signal level.

FIGURE 5.

Application Hints

Increasing the Input Impedance of the LF13300, MM5863 12-Bit A/D Converter

The input impedance of the LF13300, ADB1200 (MM5863) A/D converter can be increased 1 to 2 orders of magnitude over the typical 1000 MΩ cited in the 12-bit A/D specifications by insuring that the signals that switch the LF13300 do not overlap. A circuit that eliminates switching overlap by introducing a Delay (t_d) ≈ 3.3k x 100 pF ≈ 300 ns to the rising edge of the signals from the ADB1200 (MM5863) is shown in *Figure 6. Figure 7* shows the operation of this circuit. The total delay time t_r' of the output will be equal to the inherent gate rise time, t_r, plus the RC delay, t_d. The fall time, t_f will be the basic gate delay.

Nulling the Residual Offset

The residual offset is < 200 μV which is negligible for most applications. This can be reduced to < 40 μV by lowering the clock frequency from 250 kHz to about 75 kHz. If a lower residual offset is required, we may trim out the remainder as shown in *Figure 8*. This circuit applies a negative step to the offset correction capacitor, C_{OC2}, by means of a variable capacitor which is adjusted until charge injection imbalance of the offset correction switches are cancelled.

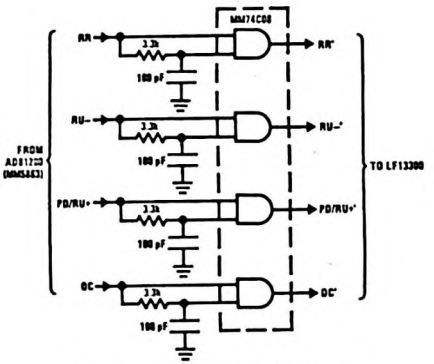


FIGURE 6. Overlap Elimination Circuit

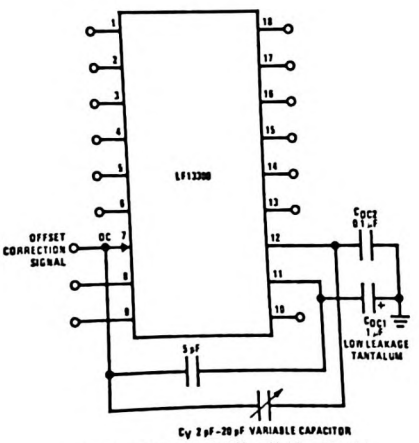


FIGURE 8. Residual Offset Nulling Circuit

Eliminating Errors Due to Power Supply Noise

For many applications, power supply noise (f ≥ 10 Hz) causes errors which reduces the accuracy of the system. In most applications, noise can be adequately eliminated by putting a series resistor (100Ω) in the power supply line with a 10 μF tantalum capacitor connected at the power supply pins *(Figure 9)*. The 10 μF capacitor is, in addition to the normal 0.1 μF ceramic disc capacitors, used as supply bypass capacitors.

Errors caused by noise on the negative supply, $-V_S$, can be further reduced by replacing, C_{OC3} with a 10 μF low leakage tantalum capacitor. Since $-V_B$ is 3V above $-V_S$, any noise appearing at $-V_S$ appears at $-V_B$; the 10 μF capacitor eliminates this noise.

Continuous Conversion Mode

For using the MM5863 in the continuous conversion mode, connect the end of conversion output, EOC (pin 23), to the output enable input, OE (pin 3), and connect the start conversion input, SC (pin 2) to 5V.

Miscellaneous

Since none of the output pins employ short-circuit protection, extreme care should be taken when breadboarding or troubleshooting with the power ON.

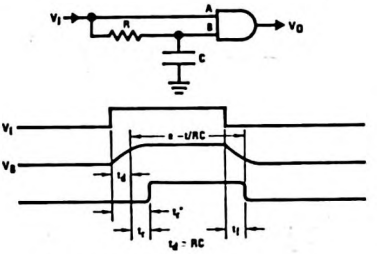


FIGURE 7. Rise Time Delay Circuit

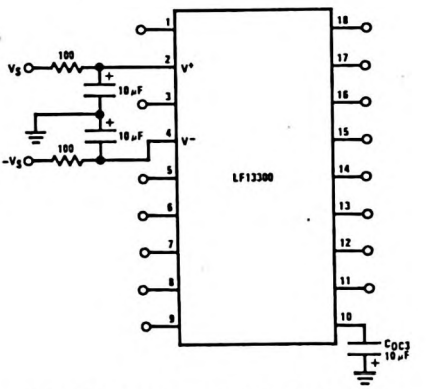
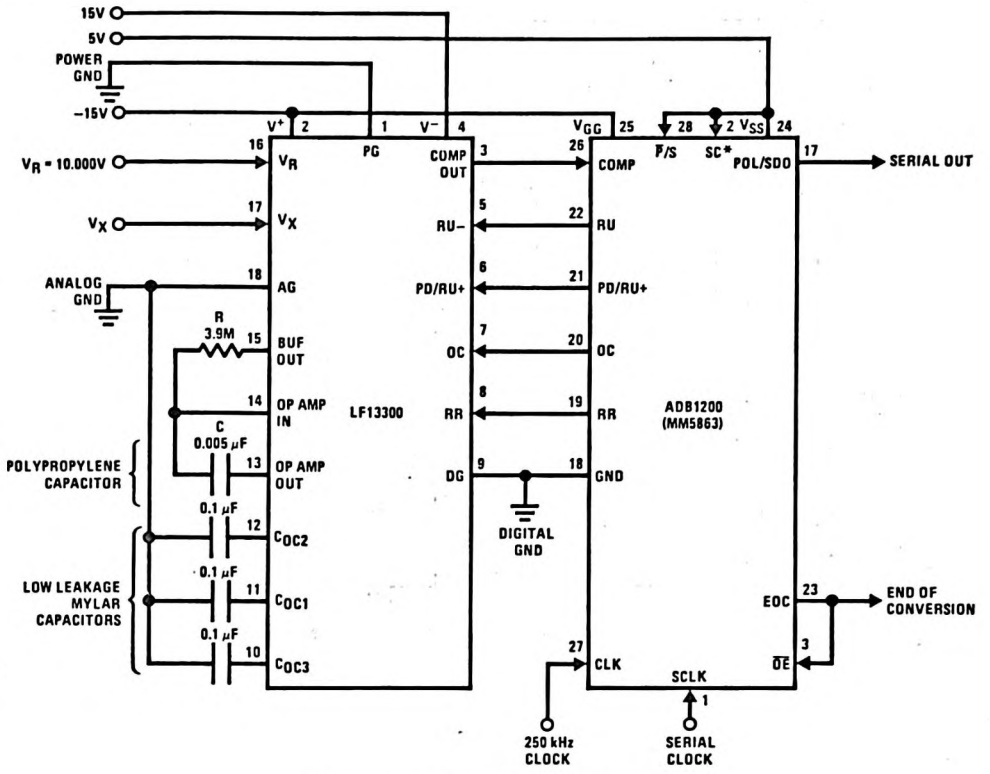


FIGURE 9. Power Supply Noise Reduction Circuit

Typical Applications



*SC at logic "1" for continuous conversion mode

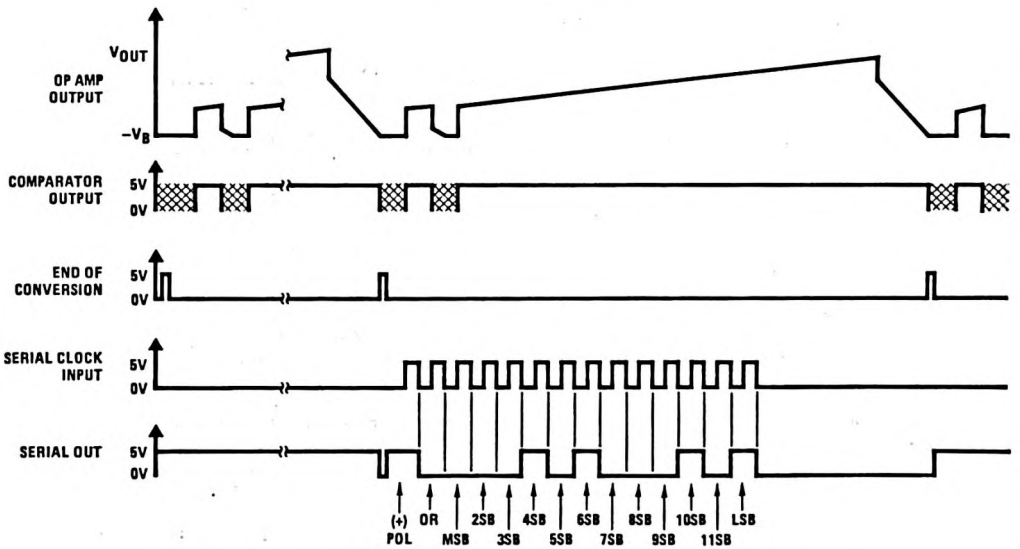
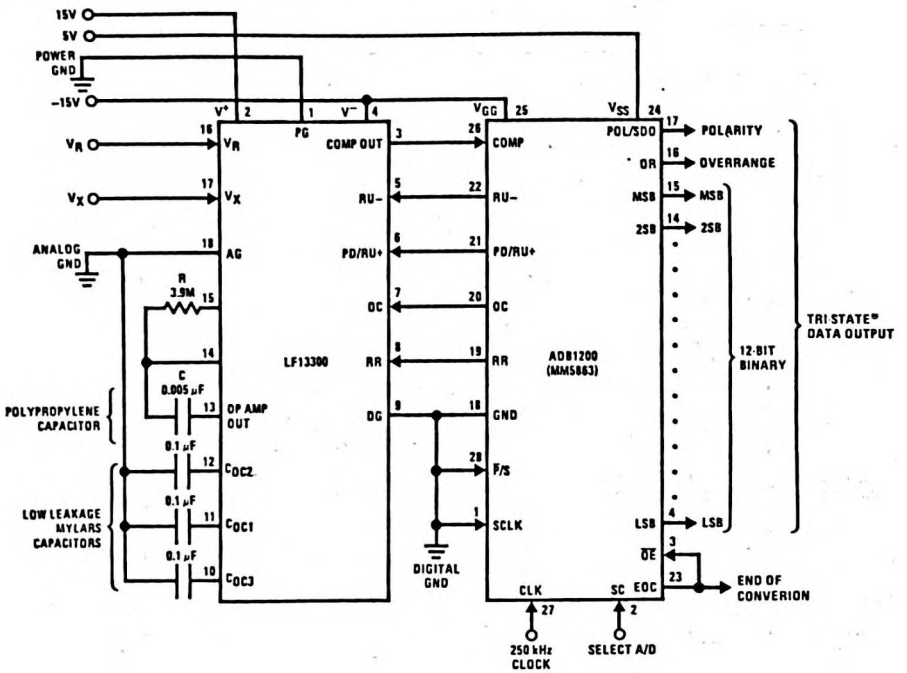
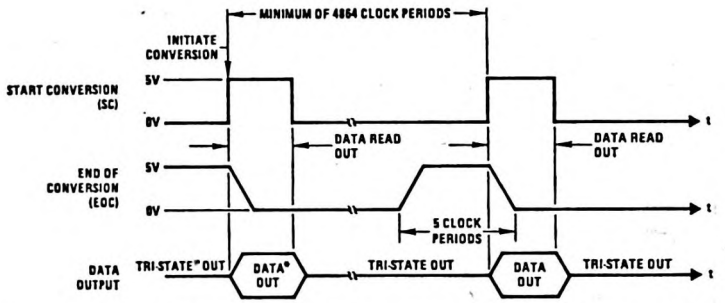


FIGURE 10. Continuous Conversion 12-Bit Plus Sign Serial Output A/D Using the LF13300 and the MM5863

Typical Applications (Continued)





® Note. Prior to the first conversion cycle, the data outputs will all be in a "1" state when the outputs are enabled ($\overline{OE}$ in "0" state).

FIGURE 11. 12-Bit Plus Sign A/D in Command Conversion Mode

4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

Figure 12 shows a low speed, high accuracy, data acquisition unit where the analog input signal is acquired differentially and preconditioned through an LF352 monolithic instrumentation amplifier. To eliminate amplifier offset errors, autozeroing circuitry is added around the LF352 and is timed through the ADB1200 and flip-flop C. Flip-flops A and B form a 2-bit up counter for channel select.

The instrumentation amplifier is zeroed at power-up and after each conversion as shown in the timing diagram; during autozero the multiplexer is disabled. When the system does polarity detection and A/D conversion, the LF352 is active and the multiplexer is enabled. The zeroing cycle for the LF13300 and the LF352 lasts for 256 clock periods, so the maximum clock frequency will depend upon the required accuracy and the minimum zeroing time of the instrumentation amplifier. Notice here that the system accuracy will be less than 12 bits since it will be affected by the gain linearity of the instrumentation amplifier.

For more details concerning data acquisition, see AN-156 and LF11508/LF11509 data sheet. For details on the instrumentation amplifier, see the LF352 data sheet.

Typical Applications (Continued)

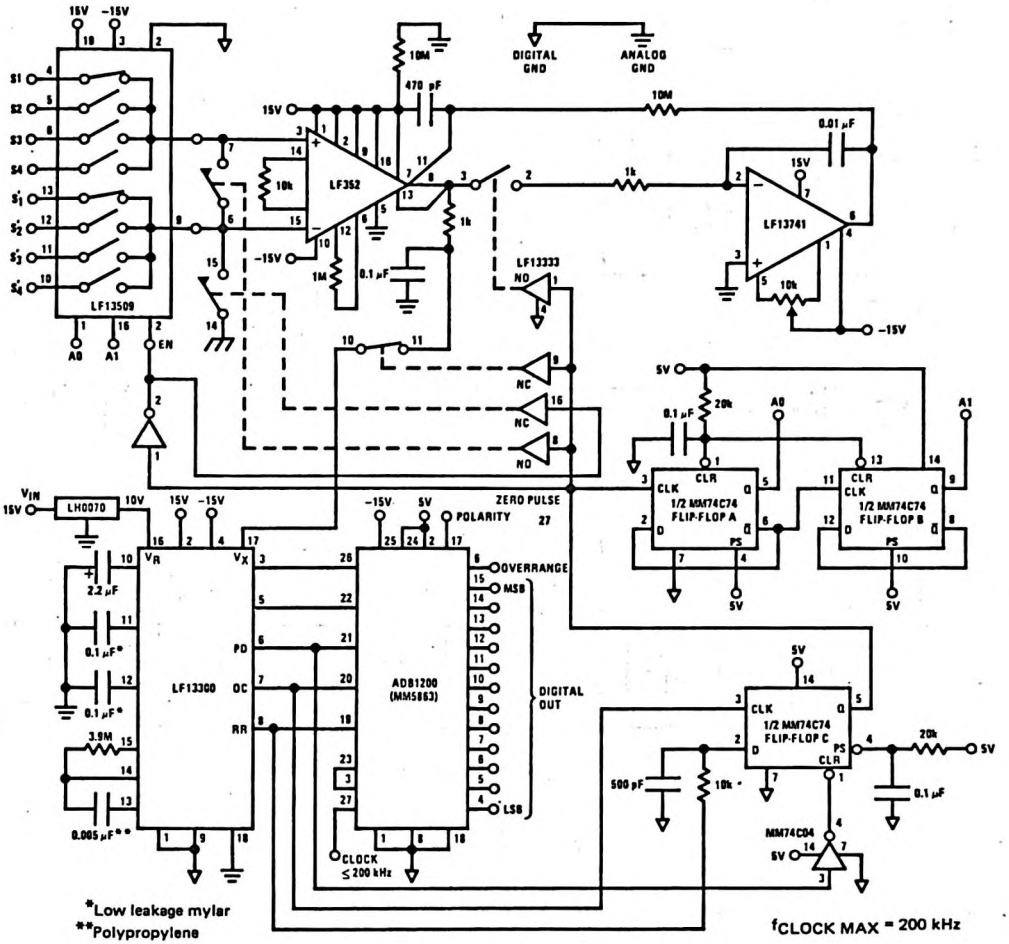


FIGURE 12. 4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

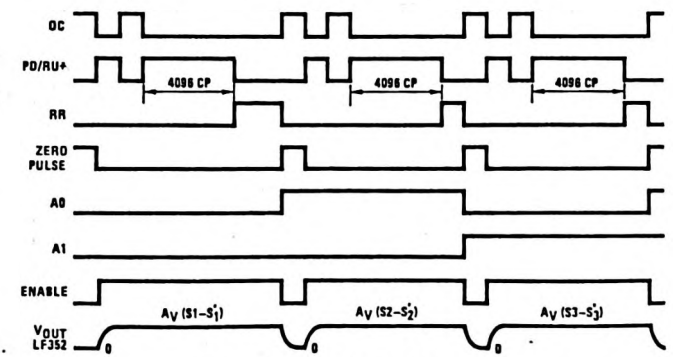


FIGURE 13. Timing Diagram for *Figure 12*

Typical Applications (Continued)

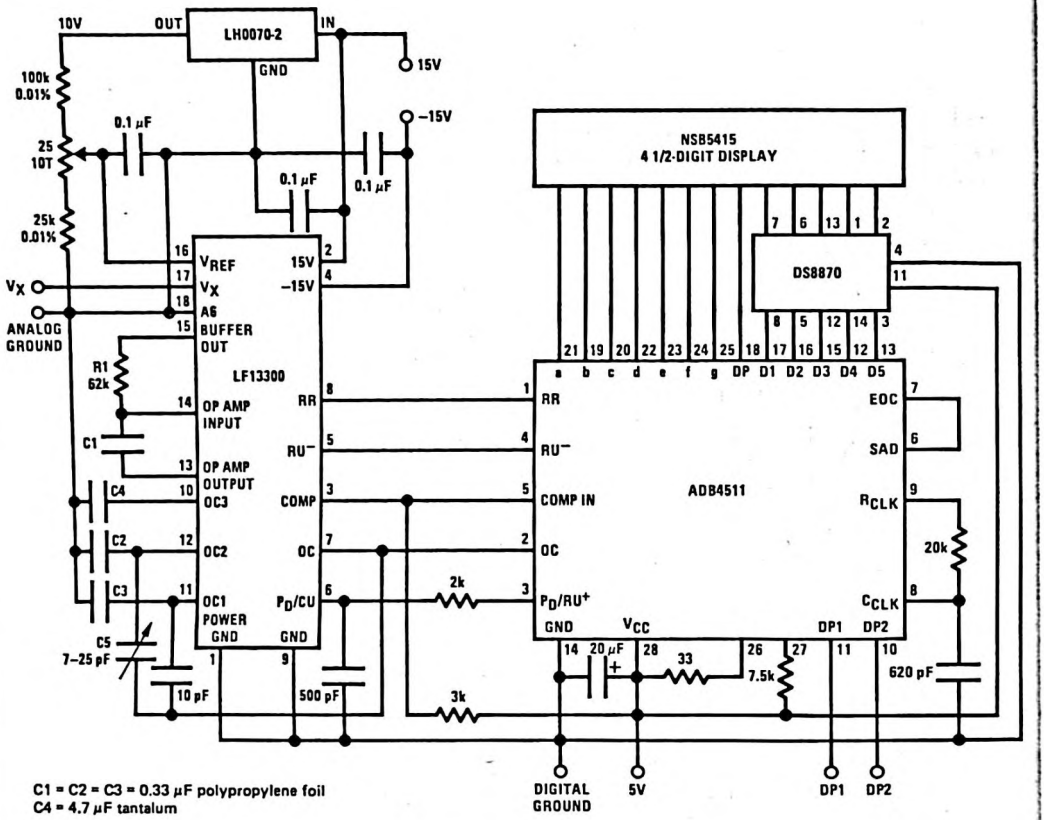


FIGURE 14. 4 1/2 Digit DPM

4½-Digit DPM Electrical Characteristics

4 1/2-digit + sign (±19,999 counts) DPM system circuit as shown in *Figure 14*, V_S = ±15V, V_{REF} = 2V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-2V \leq V_X \leq 2V$	20,000			Counts
Non-Linearity	V_X = ±1.9999V		±1/2	±1	Counts
Ratiometric Gain Error	$V_X = V_{REF}$		±1/2	±1	Counts
Gain Error Drift	$V_X = V_{REF}$, $0°C \leq T_A \leq +70°C$		±1/2		ppm/°C
Zero Reading Drift	V_X = 0, $0°C \leq T_A \leq +70°C$		±1/4		ppm/°C
Analog Input Voltage Range				±2	V
Reference Input Voltage Range	Reference Varied	0		12	V
Analog Input Leakage Current	V_X = 0			500	pA
Reference Input Leakage Current	V_X = 2V			100	nA
Analog Input Resistance	V_X = 0		1000		MΩ
Conversion Time	$V_X = V_{REF}$, f_{CLK} = 95 kHz			0.505	Sec

Typical Applications (Continued)

4 1/2-Digit DPM (20,000 Count System, > 14 Bits)

The circuit in *Figure 14* shows a complete 4 1/2-digit DPM using the LF13300 and ADB4511. The ADB4511 provides the control logic to run the LF13300. It also provides the interface and drive to a 4 1/2-digit multiplexed LED display.

Features include extremely high input impedance, > 1000 MΩ and auto-zeroing of all offset voltages in the LF13300's integrator, comparator and buffer amplifiers.

The timing waveforms for this system are the same as those shown in *Figure 5*.

The time for each phase of integration is listed below:

PHASE	NO. OF CLOCK PULSES
OC	2,000
P_D/RU^+	2,010
RU^-	20,000
RR	≤20,000

Construction and Calibration Hints

Extreme care must be taken in the following areas:

Grounds: No digital currents should flow in the analog ground; that is, the analog and digital grounds must be single point connected right at the power supply ground terminal.

Reference: The reference must be accurate and stable to within 100 μV. It must also be well bypassed for noise. Notice that with a 2V reference the resolution is 100 μV.

Clock: The R_{CLK} and C_{CLK} pins of the ADB4510 are very high impedance nodes, so the clock components must be mounted as close as possible to these pins.

Calibration Procedure

Calibration in this system is a 2 step procedure: reference, and full-scale adjust.

Step 1: Adjust the reference voltage for exactly 2.0000V. This voltage adjustment must be accurate to within ±50 μV.

Step 2: With V_X (input voltage) equal to near full-scale, ≈ ±1.9990V, adjust C5 to obtain correct reading.

Decimal Point Programming

The decimal point is programmed in the following manner:

Display	1	. 9	. 9	. 9	9
Decimal Points		1	2	3	4

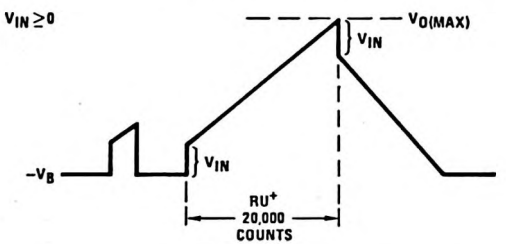
Decimal Point	1	2	3	4
DP1, Pin 11	1	0	1	0
DP2, Pin 10	1	1	0	0

(0 = Gnd, 1 = 5V)

Calculating the Integration Components

R_i, C_i

Proper selection of the integration components, R_i, C_i, is mandatory. R_i must be small enough to minimize a slight error due to the integrators bias current, but at the same time $R_i \times C_i$ must be large enough to keep the integrator within its output swing range. The ($R_i \times C_i$) min, (fastest integration), can be calculated as follows:



- $V_{O(MAX)}$ is ≈ 3 V_{BE} + 1 V_{SAT} below V_S^+ ≈ (V_S^+–2.6V)
- $-V_B$ is typically 3V above V_S^-. Assume 3.5V to be maximum
- ∴min V_O swing = [(V_S^+–2.6V) + (V_S^- + 3.5V)]
- $V_{O(RU+)\ SWING} = V_{IN} + \frac{1}{RC}\int_0^t V_{IN}dt\ t = \frac{1}{f_{CLK}} \cdot 20{,}000$
  V_{IN} = 2V max
- Equating min V_O (SWING) and $V_{O(RU+)}$ SWING R_iC_i min can be solved for:

  $(R_i \times C_i)\ \text{min} = \frac{1826}{f_{CLK}}$; V_S = ±15V

Typical Applications (Continued)

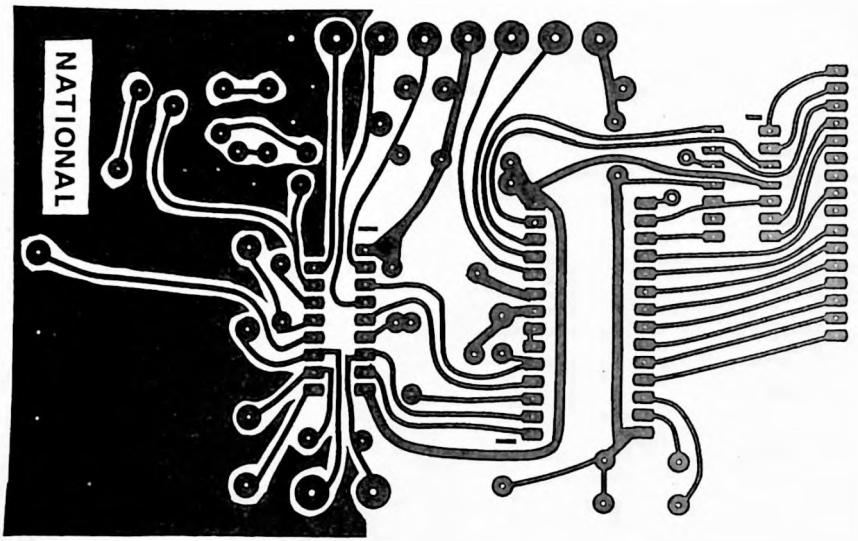


FIGURE 15. PC Board for 4 1/2-Digit DPM (Foil Side)

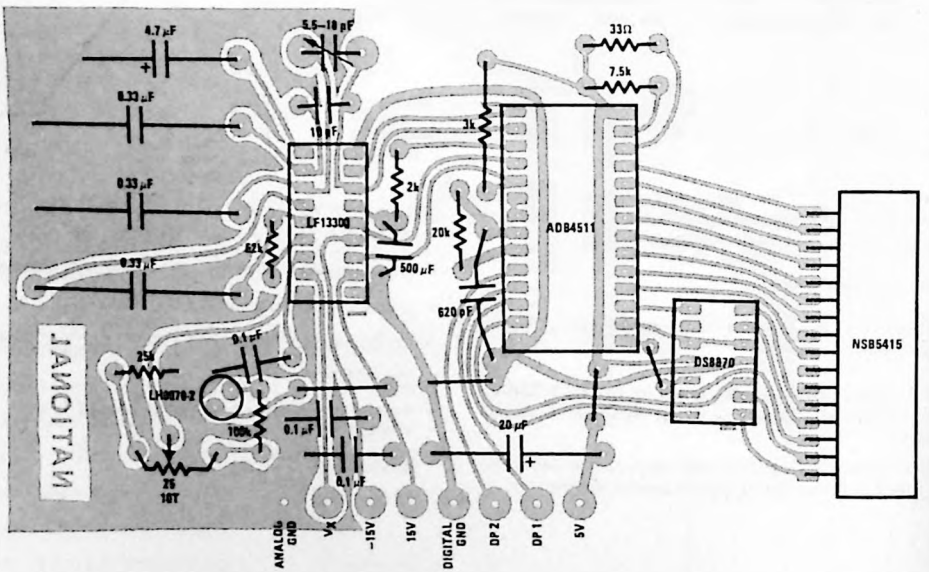


FIGURE 16. Stuffing Diagram for 4 1/2-Digit DPM (Component Side)

Typical Applications (Continued)

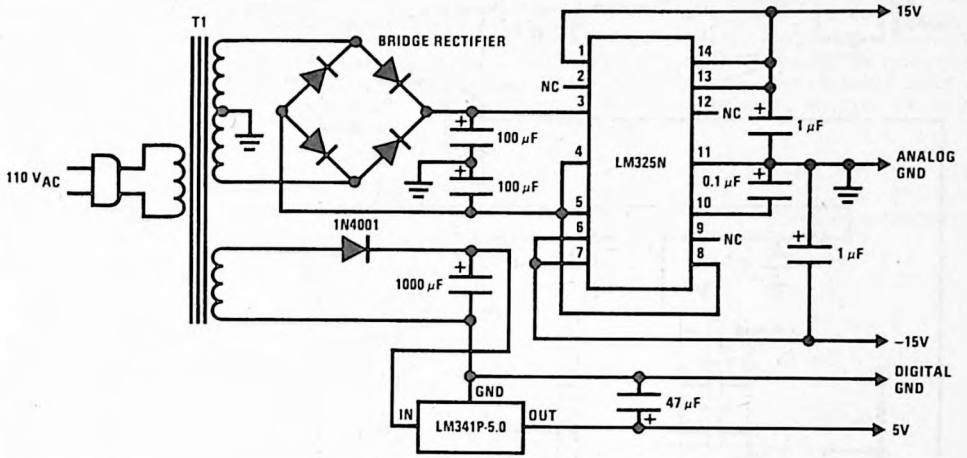
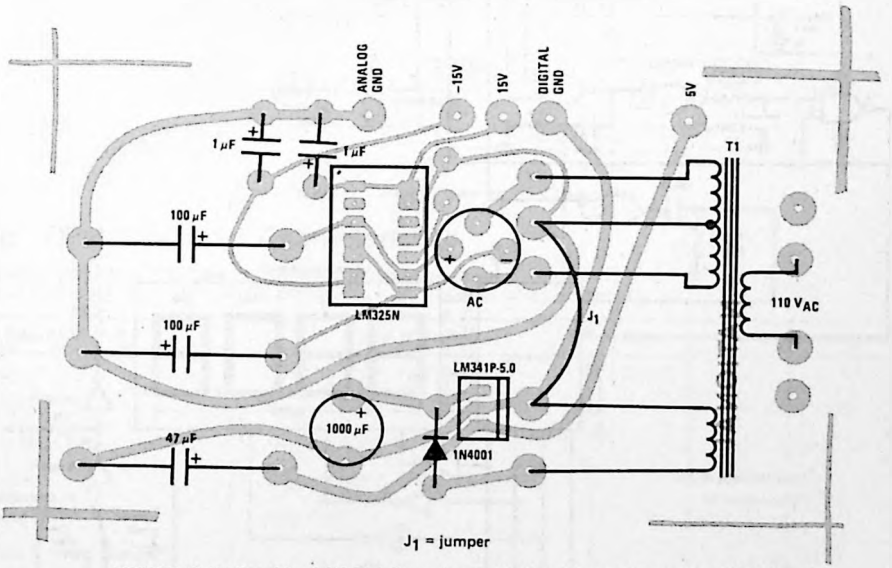


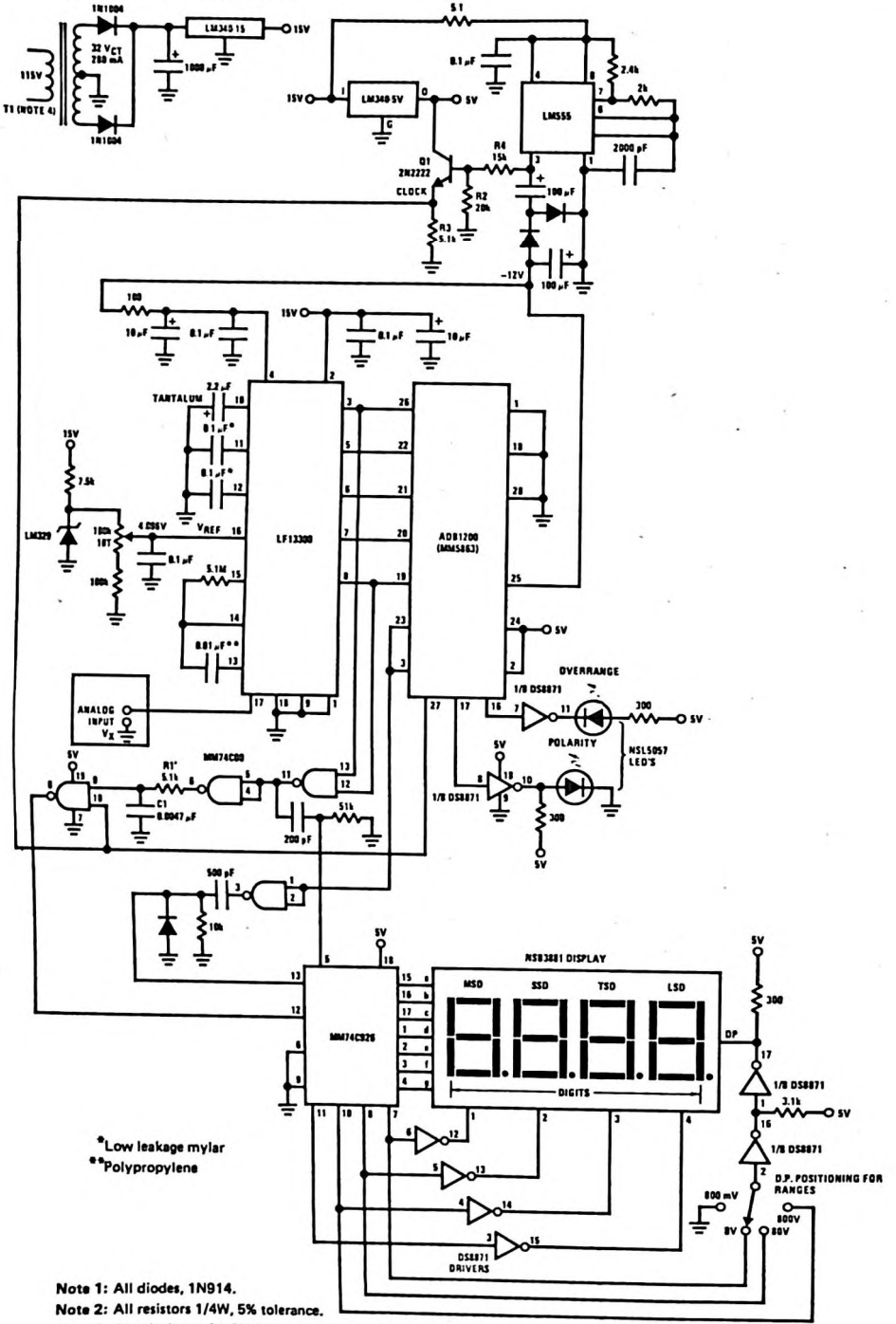
FIGURE 17. Power Supply for 4 1/2-Digit DPM



J_1 = jumper

FIGURE 18. PC Board for 4 1/2-Digit Power Supply Stuffing Diagram (Component Side Shown)

Typical Applications (Continued)



*Low leakage mylar
**Polypropylene

Note 1: All diodes, 1N914.
Note 2: All resistors 1/4W, 5% tolerance.
Note 3: Circuit drawn for 8V full scale operation input scaling not shown.
Note 4: Inductive components U4X003 or Microtran PC6714.

FIGURE 19. 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM Schematic Diagram

Typical Applications (Continued)

3 3/4 Plus Digit (±8191 Counts)/3 1/2-Digit (±1999 Counts) DPM

In this circuit of *Figure 19*, the LF13300 and ADB1200 interact as previously described. The CMOS counter (MM74C926, MM74C928) is connected to count clock pulses during the ramp reference cycle. The counts are latched into the display when the comparator output trips, (goes low), as shown in the timing diagram *Figure 20*.

The RC network consisting of R1 and C1 is a low pass filter that prohibits the fast transients that occur on the comparator output during Offset Correction from loading any erroneous counts into the counter.

The DPM is able to operate from a single 15V power supply with the aid of a dc-dc converter. The LM555 generates the negative voltages required in the circuit and also doubles as the clock. The combination of Q1, R2, R3 and R4 forms a level shift to convert the output swing of the LM555 to a 0V–5V swing that is compatible with the logic. The LM340–5 drops the incoming 15V to 5V for use by the logic circuits and the LED display.

This circuit can be a 3 3/4 plus digit DPM if the MM74C926 is used or a 3 1/2-digit DPM if the MM74C928 is used. These counters are pin compatible and physically interchangeable.

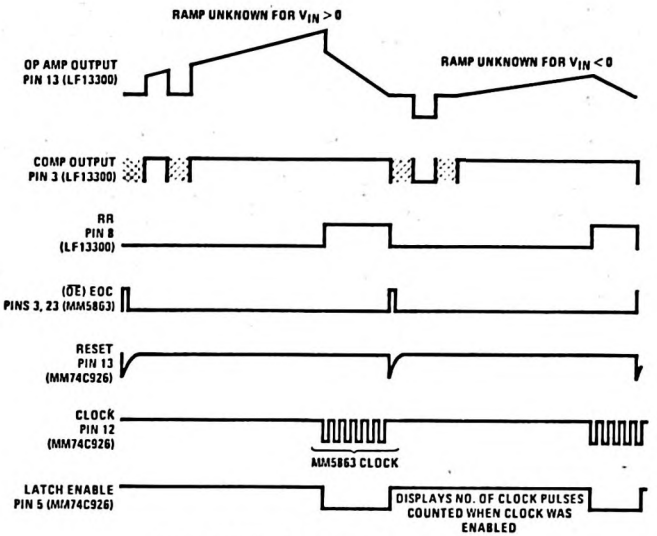

RAMP UNKNOWN FOR $V_{IN} > 0$
OP AMP OUTPUT PIN 13 (LF13300)
RAMP UNKNOWN FOR $V_{IN} < 0$
COMP OUTPUT PIN 3 (LF13300)
RR PIN 8 (LF13300)
($\overline{OE}$) EOC PINS 3, 23 (MM5863)
RESET PIN 13 (MM74C926)
CLOCK PIN 12 (MM74C926)
MM5863 CLOCK
LATCH ENABLE PIN 5 (MM74C926)
DISPLAYS NO. OF CLOCK PULSES COUNTED WHEN CLOCK WAS ENABLED

FIGURE 20. Timing Diagram for 3 3/4-Digit DVM

3¾-Digit DPM Electrical Characteristics

3 3/4 plus digits plus sign (±8191 counts) DPM system characteristics.
(Circuit as in *Figure 18*, $V_S = \pm 15V$, $V_R = 4.096V$, $T_A = 25°C$, unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-8.2V \leq V_X \leq +8.2V$	16,382			Counts
Nonlinearity	$V_{IN} = 4.000V$		±1/8	±1/2	Counts
Ratiometric Gain Error	$V_{IN} = 4.000V$		±1/2	±2	Counts
Gain Error Drift	$V_{IN} = 4.000V$, $0°C \leq T_A \leq +70°C$		±1		ppm/°C
Zero Reading Drift	$V_{IN} = 0V$		±1		ppm/°C
Analog Input Voltage Range				±11	V
Reference Input Voltage Range	Reference Varied	0		+12	V
Analog Input Leakage Current	$V_{IN} = 0V$		80	500	pA
Reference Input Leakage Current			0.1	100	nA
Analog Input Resistance	$V_{IN} = 0V$		1000		MΩ
Conversion Time	$V_{IN} = 4.000V$, $f_C = 125$ kHz			74	ms

Typical Applications (Continued)

Component Side Foil

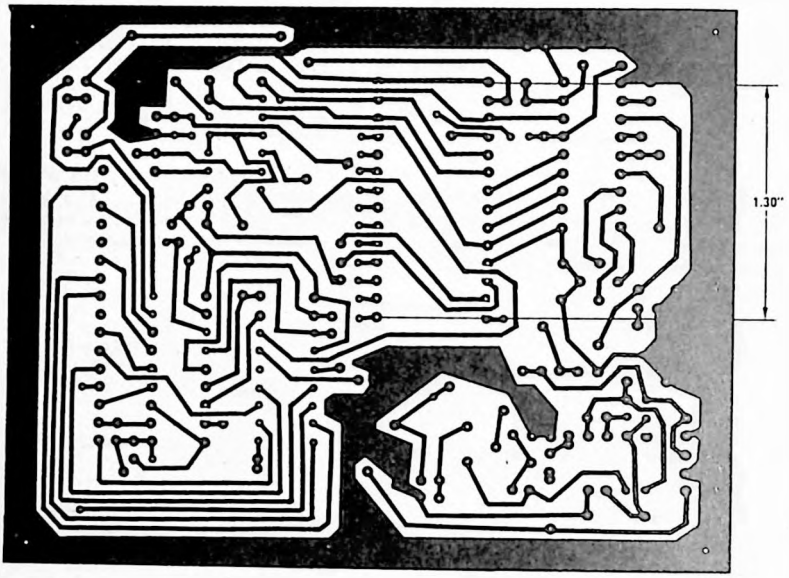


FIGURE 21. PC Board for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

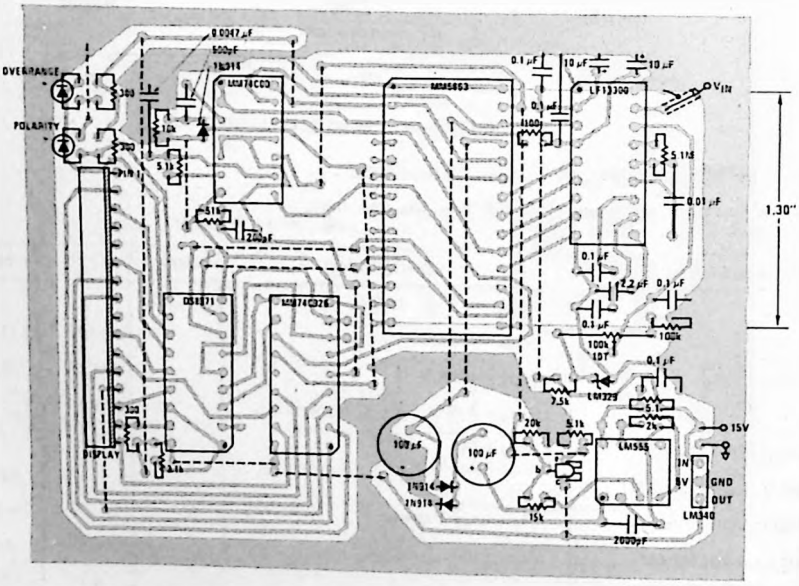
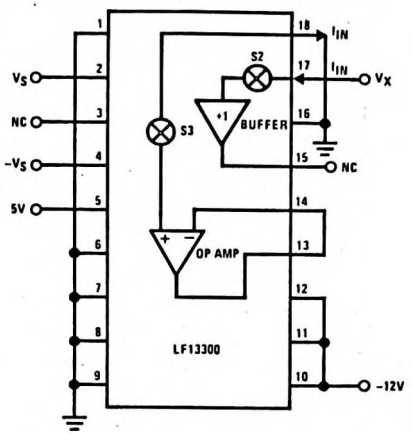


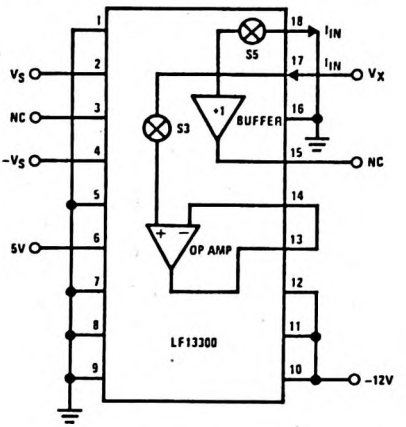
FIGURE 22. Stuffing Diagram for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

AC Test Circuits

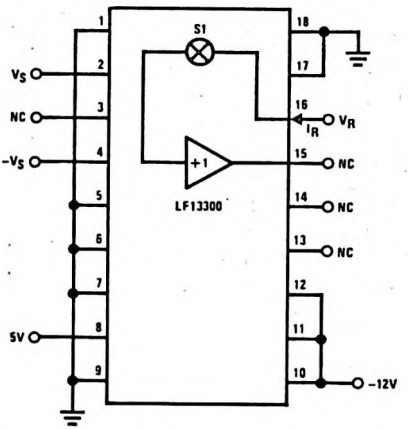
Test Circuit 1
Analog Input Characteristics Test with RU — High



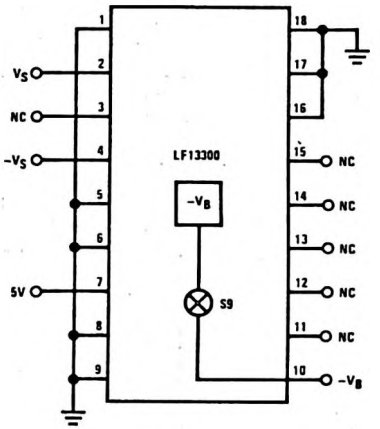
Test Circuit 2
Analog Input Characteristics Test with PD/RU+ High



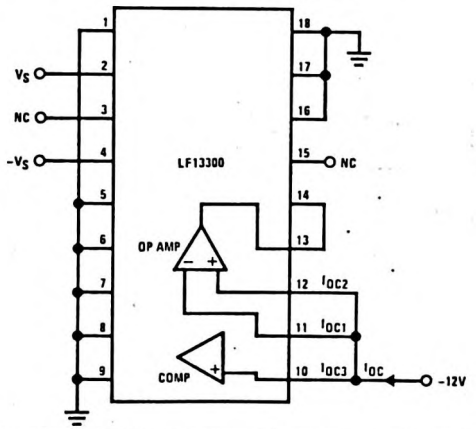
Test Circuit 3
Reference Input Characteristic Test with RR High



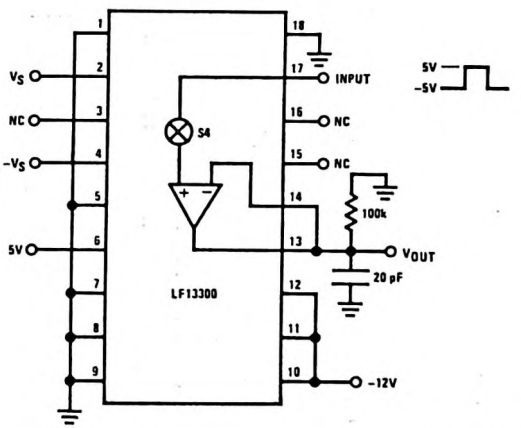
Test Circuit 4
–VB Voltage Measurement Test



Test Circuit 5
Offset Correction Input Current, I_{OC} Test

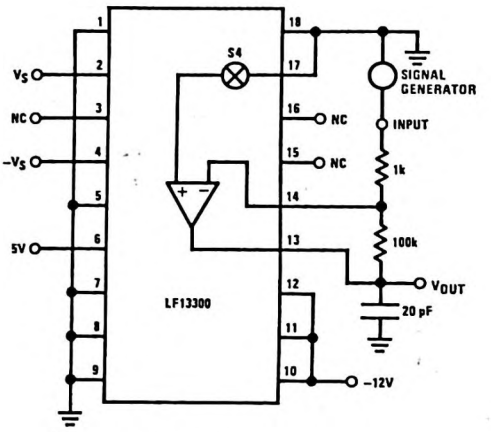


Test Circuit 6
Op Amp Slew Rate Test

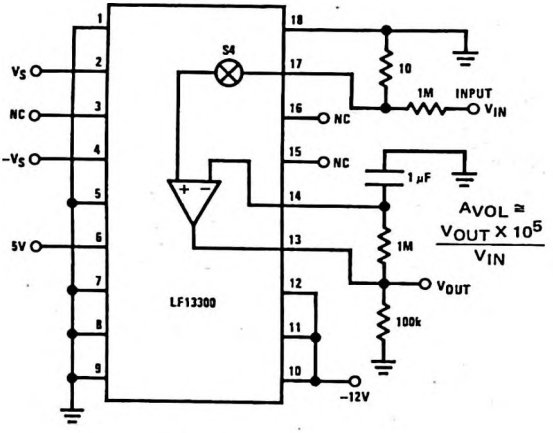


AC Test Circuits (Continued)

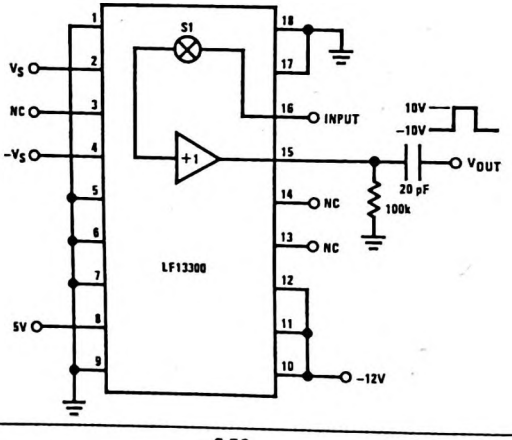
Test Circuit 7
Frequency Response Test



Test Circuit 8
Open Loop Gain Test

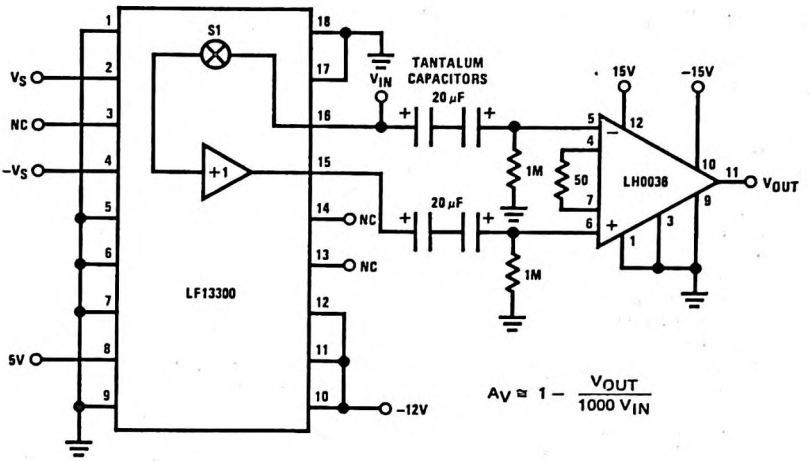


Test Circuit 9
Buffer Slew Rate Test



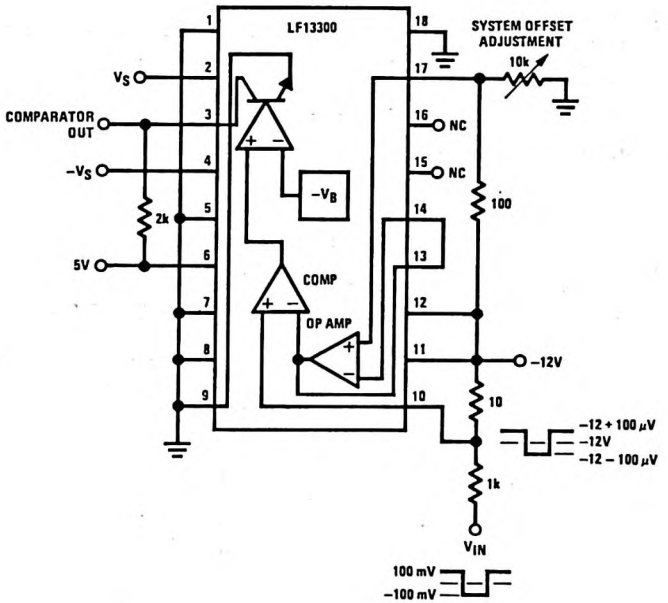
AC Test Circuits (Continued)

Test Circuit 10
Buffer Voltage Gain Test



$$A_V \cong 1 - \frac{V_{OUT}}{1000\, V_{IN}}$$

Test Circuit 11
Comparator Response Time Test



National Semiconductor

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

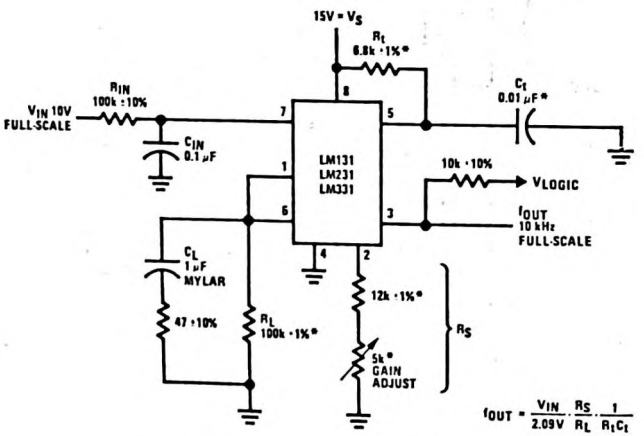
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See applications notes.

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Absolute Maximum Ratings

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to +V_S	−0.2V to +V_S	−0.2V to +V_S
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W
(N Package) P_D		500 mW	500 mW
θ_{jA}		155°C/W	155°C/W

Electrical Characteristics T_A = 25°C unless otherwise specified. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VFC Non-Linearity (Note 2)	4.5V ≤ V_S ≤ 20V		±0.003	±0.01	% Full-Scale
	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.006	±0.02	% Full-Scale
In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	% Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	T_{MIN} ≤ T_A ≤ T_{MAX}, 4.5V ≤ V_S ≤ 20V				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	4.5V ≤ V_S ≤ 10V		0.01	0.1	%/V
	10V ≤ V_S ≤ 40V		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	T_{MIN} ≤ T_A ≤ T_{MAX}		±4	±14	mV
LM131A/LM231A/LM331A	T_{MIN} ≤ T_A ≤ T_{MAX}		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	T_{MIN} ≤ T_A ≤ T_{MAX}	−0.2		V_{CC}−2.0	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	x V_S
Input Bias Current, Pin 5	V_S = 15V				
All Devices	0V ≤ $V_{PIN\ 5}$ ≤ 9.9V		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V

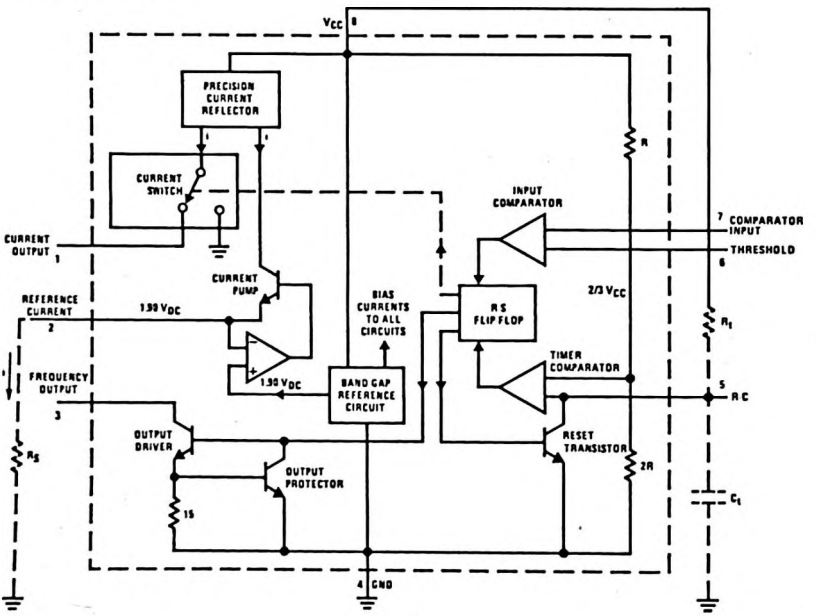
Electrical Characteristics (Continued) $T_A = 25°C$ unless otherwise specified (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \leq V_{PIN\ 1} \leq 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	$I = 5\ mA$		0.15	0.50	V
	$I = 3.2\ mA$ (2 TTL Loads), $T_{MIN} \leq T_A \leq T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231, LM231A	$V_S = 5V$	2.0	3.0	4.0	mA
	$V_S = 40V$	2.5	4.0	6.0	mA
LM331, LM331A	$V_S = 5V$	1.5	3.0	6.0	mA
	$V_S = 40V$	2.0	4.0	8.0	mA

Note 1: All specifications apply in the circuit of *Figure 3*, with $4.0V \leq V_S \leq 40V$, unless otherwise noted.

Note 2: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz/-10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon*, or polystyrene.

Functional Block Diagram



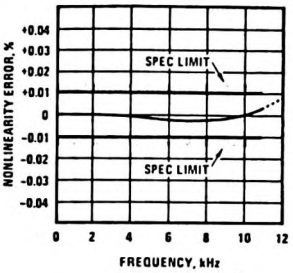
*Registered trademark of DuPont

FIGURE 1a

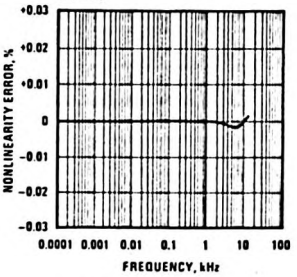
Typical Performance Characteristics

(All electrical characteristics apply for the circuit of *Figure 3*, unless otherwise noted.)

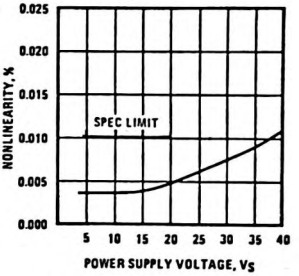
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter *(Figure 3)*



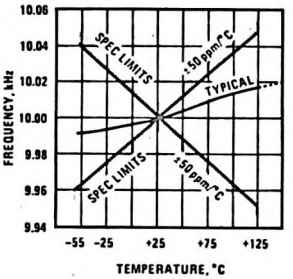
Nonlinearity Error, LM131 Family



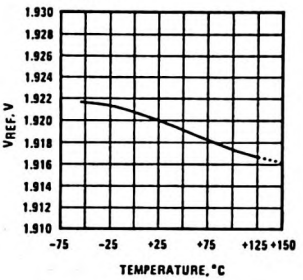
Nonlinearity vs Power Supply Voltage



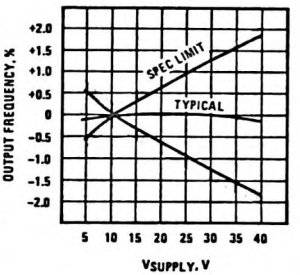
Frequency vs Temperature, LM131A



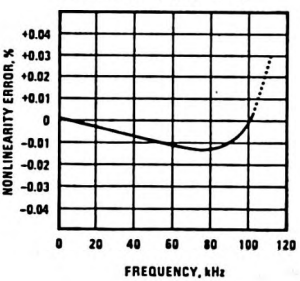
VREF vs Temperature, LM131A



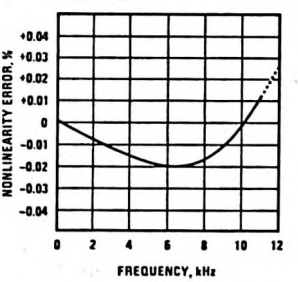
Output Frequency vs VSUPPLY



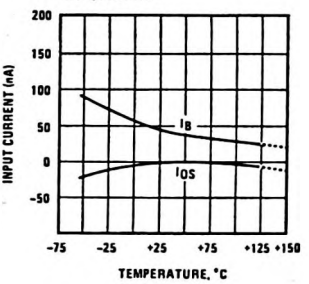
100kHz Nonlinearity Error, LM131 Family *(Figure 4)*



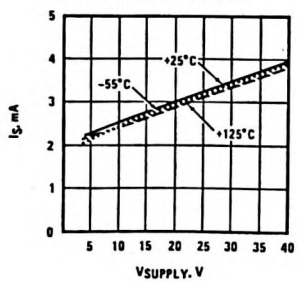
Nonlinearity Error, LM131 *(Figure 1)*



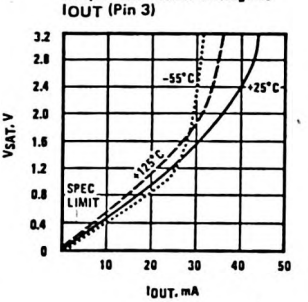
Input Current (Pins 6, 7) vs Temperature



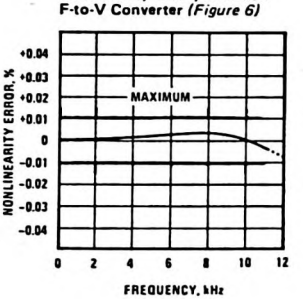
Power Drain vs VSUPPLY



Output Saturation Voltage vs IOUT (Pin 3)



Nonlinearity Error, Precision F-to-V Converter *(Figure 6)*



Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_X, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_X up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_X falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_X/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.

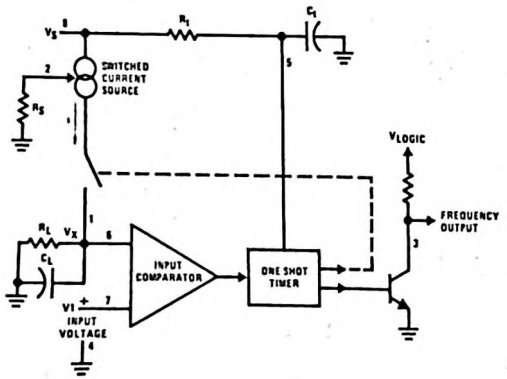


FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM *(FIGURE 1a)*

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than 1/2% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_S$ to flow. For $R_S = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the RS flip-flop.

The timing function consists of an RS flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the RS flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to 2/3 V_{CC}, the timer comparator causes the RS flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses 2/3 V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER *(FIGURE 1)*

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_S at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t. For best results, all the components

Typical Applications (Continued)

should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon* or polypropylene are best suited.

A capacitor is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily.

A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

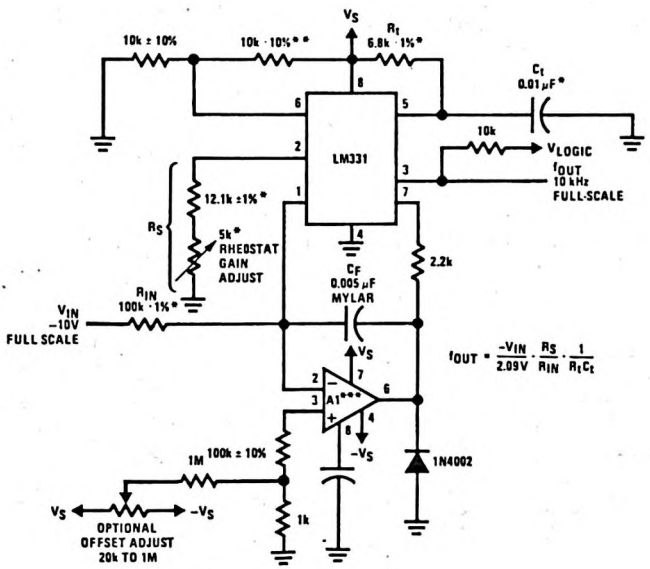
DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER *(FIGURE 3)*

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated. The average current fed into the op amp's summing point (pin 2) is i x (1.1 R_tC_t) x f which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter, nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.

*Registered trademark of DuPont



*Use stable components with low temperature coefficients. See applications notes.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF351B

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

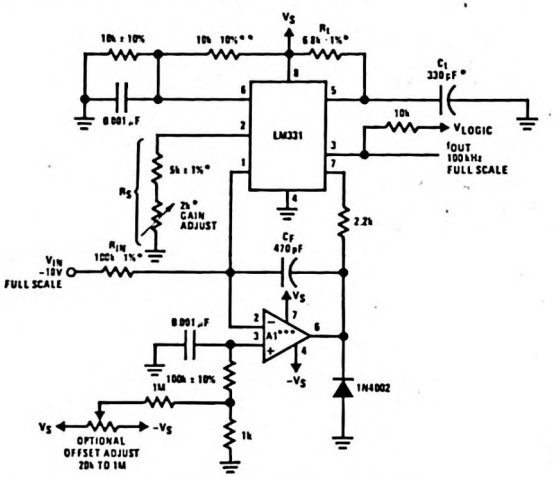
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS *(FIGURES 5 AND 6)*

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *Figure 5*, this current is filtered in the network R_L = 100 kΩ and 1 μF. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.

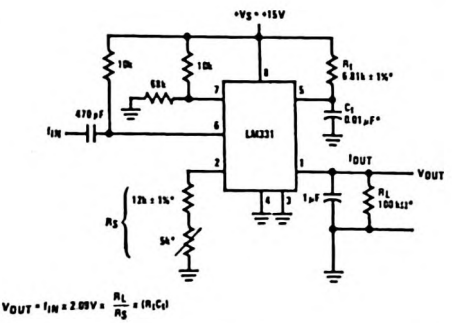


*Use stable components with low temperature coefficients. See applications notes.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

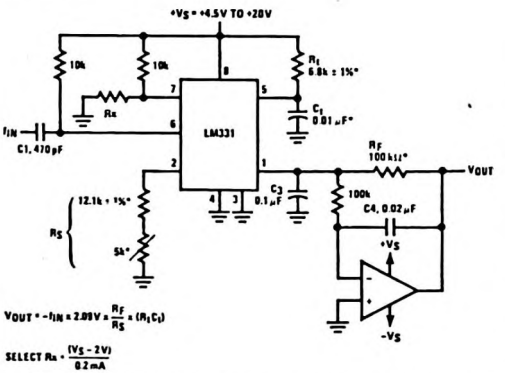
***Use low offset voltage and low offset current op amps for A1: recommended types LF351B or LF356.

FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity



*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity

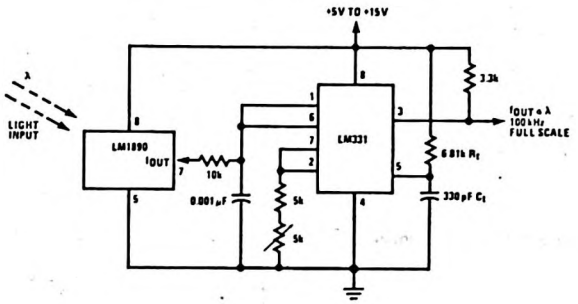


*Use stable components with low temperature coefficients.

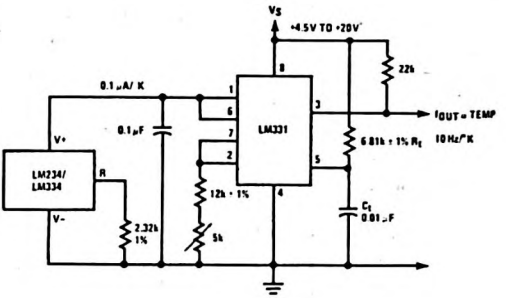
FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Typical Applications (Continued)

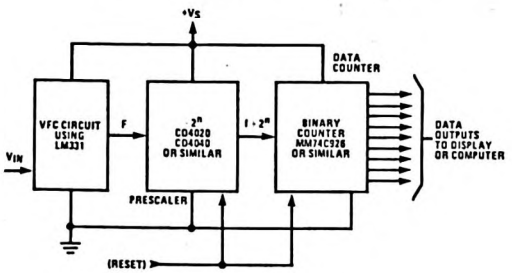
Light Intensity to Frequency Converter



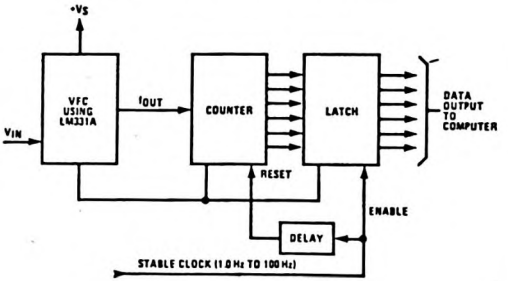
Temperature to Frequency Converter



Long-Term Digital Integrator Using VFC

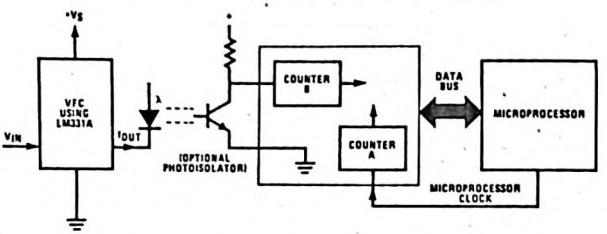


Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter

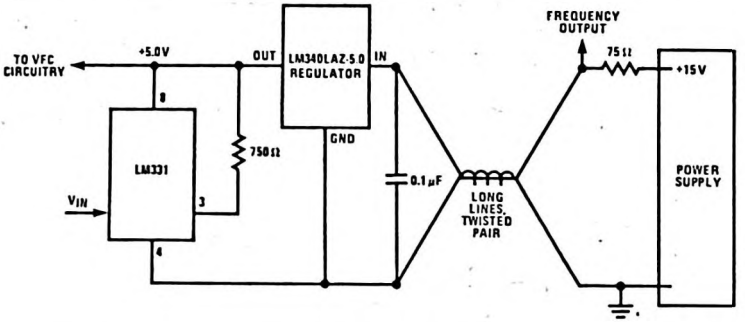


Typical Applications (Continued)

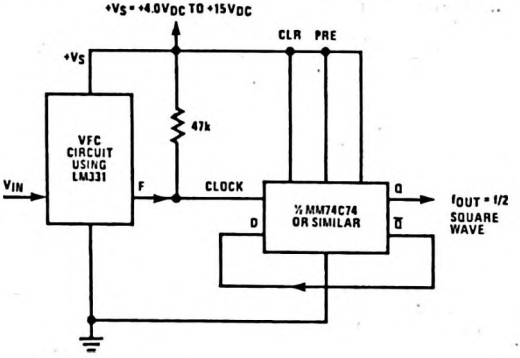
Analog-to-Digital Converter with Microprocessor



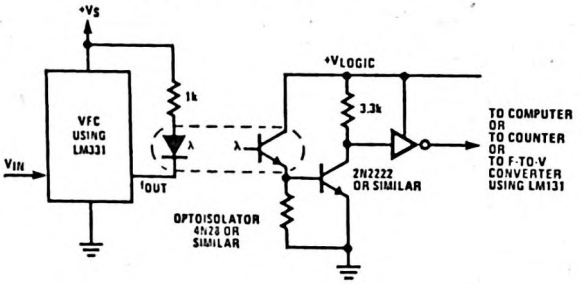
Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



Voltage-to-Frequency Converter with Square-Wave Output Using ÷2 Flip-Flop

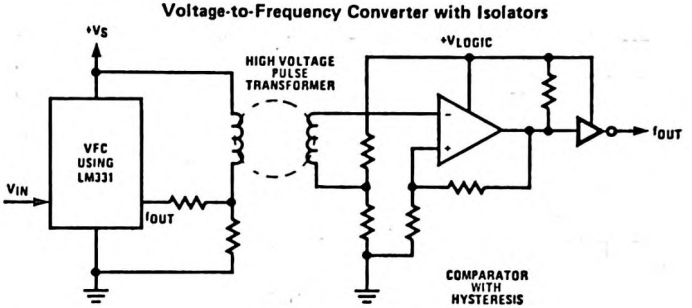


Voltage-to-Frequency Converter with Isolators

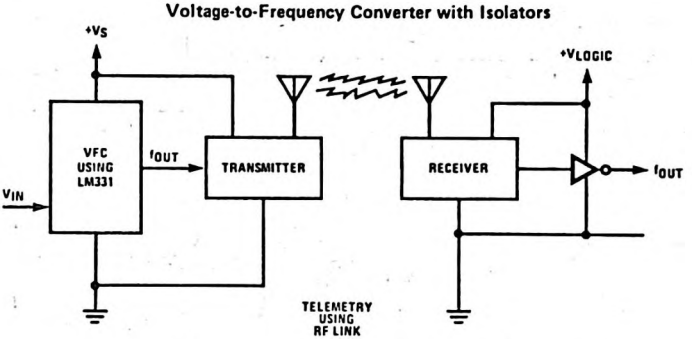


Typical Applications (Continued)

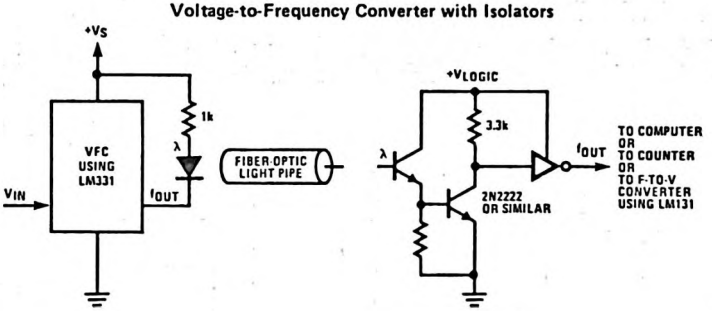
Voltage-to-Frequency Converter with Isolators



Voltage-to-Frequency Converter with Isolators

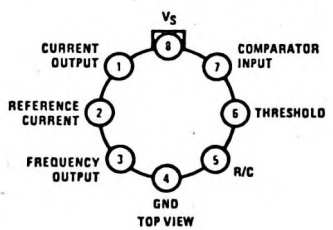


Voltage-to-Frequency Converter with Isolators



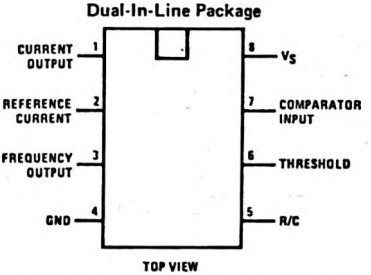
Connection Diagrams

Metal Can Package



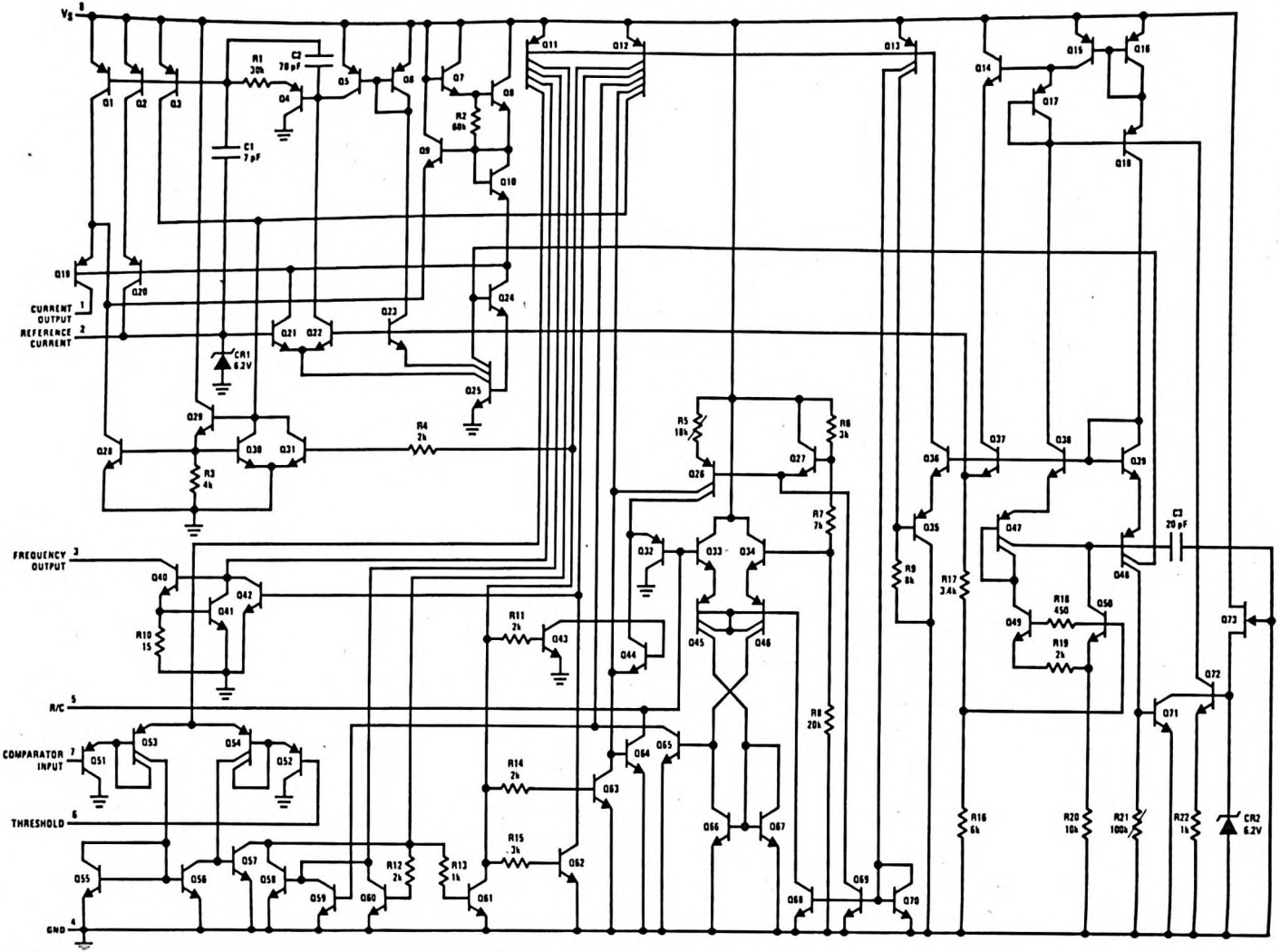
Order Number LM131AH, LM131H, LM231AH, LM231H, LM331AH or LM331H
See NS Package H08B

Dual-In-Line Package



Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package N08A

Schematic Diagram



National Semiconductor

Analog-to-Digital Converters

TP3000 CODEC System (TP3001 μ-Law, TP3002 A-Law)

General Description

The TP3001 and TP3002 are Pulse Code Modulation (PCM) systems for the digital coding and decoding of analog signals in the voice frequency band. The TP3001 system utilizes μ-law coding of the analog signals while the TP3002 is an A-law system. Each system consists of 2 IC packages. The TP3001 system uses linear part LF3700 and CMOS part MM58100. The TP3002 system uses the same linear part and a different CMOS part (MM58150). Each system samples a filtered (300 Hz $\leq$ f $\leq$ 3.4 kHz) analog signal at an 8 kHz rate, converts this sampled voltage to an 8-bit companded digital code (μ-law or A-law) and loads this code into a high speed serial output buffer. This output buffer will operate at any speed between 64 and 2100 kilobits per second. Either system will also accept an incoming 8-bit PCM word (again, at any speed between 64 and 2100 kilobits per second) and will automatically interrupt the encode cycle to decode the PCM word and update the CODEC output sample and hold. After decoding, the systems will automatically return to the encoding cycle. This interrupt capability allows either CODEC system to send and receive PCM data asynchronously. These systems were specifically designed for low cost "per line" or per channel CODEC applications.

These IC's contain all the necessary elements required for a complete CODEC system—both the input and output sample and hold, comparator, stable voltage reference, non-linear D/A converter, successive approximation logic, control logic and digital input and output PCM buffers. The user must provide an input aliasing filter (300 Hz $\leq$ f $\leq$ 3.4 kHz) such as the AF133 or similar filter. The AF134, or similar filter, is available for use as the output filter (300 Hz $\leq$ f $\leq$ 3.4 kHz) which is needed to reject sidebands around 8 kHz and provide correction for the sinx/x frequency distortion introduced by the output sample and hold.

A special auto-zero circuit insures an extremely low idle channel noise and low crosstalk enhancement. During the decode cycle, the non-linear D/A converter is shifted 1/2 LSB, thereby achieving a typical signal to total distortion performance of at least 3 dB better than the D3 channel bank specifications.

The TP3001 system also includes 4 pins for the insertion and extraction of the signaling bits required for D3 channel bank operation.

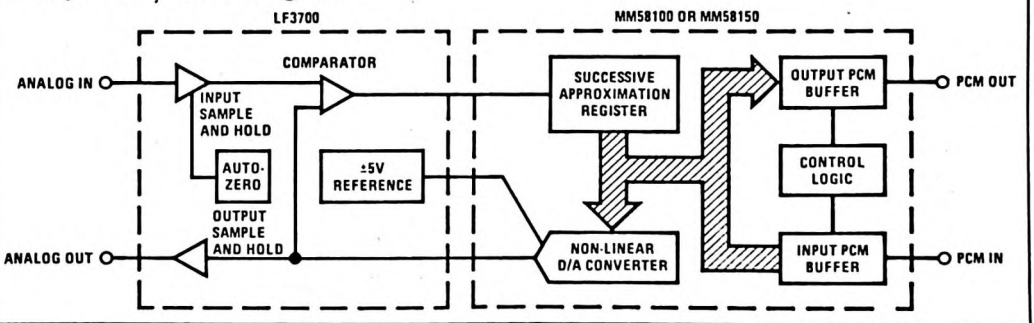
Features

- TP3001 uses the standard μ-255 code
- TP3002 uses the standard A-law code
- Each 2-chip system includes:
  - Non-linear D/A converter
  - Voltage reference with excellent long term stability
  - Comparator
  - Successive approximation logic
  - Input digital buffer
  - Output digital buffer
  - Input sample and hold
  - Output sample and hold
  - Auto-zero circuit
  - Control logic
- TP3001 system meets or exceeds all relevant D3 channel bank specifications
- Both systems meet or exceed all relevant CCITT specifications
- Analog input range of ±5V
- Analog output range of ±5V
- Input and output PCM words can be clocked at 64 to 2100 kilobits per second
- Incoming PCM word may be asynchronous
- Provision for the insertion and extraction of signaling bits in the TP3001 system
- Open drain PCM out for TRI-STATE® capability

Applications

- Use with digital switching systems in telephone central office or private branch exchange
- Replace 24 or 32-channel shared CODEC in telephone channel bank
- Use to digitize voice and similar analog signals for low noise transmission and reception

Simplified Block Diagram



Absolute Maximum Ratings

V^+ to Gnd	15V
V^- to Gnd	−15V
Voltage at Any Pin Except Digital Inputs or Digital Outputs	V^+ to V^-
Voltage at Any Digital Input or Output	−0.3 to +5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V^+ = 12V$, $V^- = -12V$, $V_{EE} = -12V$ (Note 4) over operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Distortion	Method 1:				
TP3001 or TP3002 Either Encoding or Decoding	A Suitable Noise Signal Applied to the Coder Input Between −55 dBm0 and −3 dBm0 (Refer to CCITT Rec. G712, Paragraph 9, Method 1), *(Figure 4)*		2		dB Above the CCITT Limits Shown in *Figure 1.*
	Method 2: Measured with C Message Weighting Filter, 1020 Hz Input Signal				
	0 dBm0 to −30 dBm0	36			dB
	−40 dBm0	30			dB
	−45 dBm0 *(Figure 5)*	25			dB
Gain Tracking Error	Method 1:				
TP3001 or TP3002 Either Encoding or Decoding	Deviation From Gain at −10 dBm0 A Suitable Noise Signal Applied to the Coder Input Between −60 dBm0 and −10 dBm0 (Refer to CCITT Rec. G712, Paragraph 11, Method 1, *(Figure 4)*				Within Limits Shown in *Figure 2* (Note that *Figure 2* is 1/2 of the Limits Set By CCITT.)
	Method 2: Deviation From Gain at 0 dBm0 1020 Hz Input Signal				
	3 dBm0 to −37 dBm0	−0.25		+0.25	dB
	−37 dBm0 to −50 dBm0 *(Figure 6)*	−0.50		+0.50	dB
Idle Channel Noise	Input Terminated with 600Ω				
TP3001	*(Figure 7)*		12		dBrnc0
TP3002			−72		dBm0p
Single Frequency Distortion	1020 Hz Input Signal at 0 dBm0, *(Figure 8)*			−40	dBm0
Reference Voltage	(Note 1)	5.25	5.50	5.75	V
Temperature Coefficient of Reference Voltage			±1.5		mV/°C
Decoder 0 dBm0 Output Level	(Note 1)	2.58	2.70	2.82	Vrms
Intrachannel Crosstalk					
Go-to-Return Crosstalk	Level at Decoder Output Due to a 0 dBm0 Signal Being Encoded *(Figure 9)*		−62		dBm0
Return-to-Go Crosstalk	Level at Encoder Output (Measured Via Independent Decoder) Due to a 0 dBm0 Signal Being Decoded *(Figure 10)*		−70		dBm0

Electrical Characteristics (Continued)

$V^+ = 12V$, $V^- = -12V$, $V_{EE} = -12V$ (Note 4) over operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Interchannel Crosstalk (TP3001 Only)	Level at Decoder Output When a −80 dBm0 Signal is Applied to Encoder Input *(Figure 11)*		−83		dBm0
Analog Output Frequency Response	$300 \leq f \leq 3.4$ kHz		±0.05		dB Deviation From Theoretical sinx/x Response *(Figure 3)*
Logical "1" Input Voltage	(Note 5)	4.0			V
Logical "1" Input Current	Digital $V_{IN} = 5V$			1	μA
Logical "0" Input Voltage				0.8	V
Logical "0" Input Current	Digital $V_{IN} = 0V$			−1	μA
Master Clock Frequency, F_C	For Proper Operation: Duty Cycle = 50% ±10%		128		kHz
Input and Output PCM Buffer Clocks (F_{bo} and F_{bi})	F_o and F_i = 8 kHz F_{bo}, F_{bi} Duty Cycle = 40–60%	64		2100	kHz
Propagation Delay F_{bo} to Valid PCM Out		50	150	250	ns
PCM Out Pin Capacitance			4		pF
PCM Out Fall Time	1 kΩ Resistor to V_{DD} 100 pF Capacitor to V_{SS}		50	150	ns
System Power Dissipation	F_{bo}, F_{bi} = 1.544 MHz		250	300	mW
Shutdown Mode (LF3701 Only)	Pin 3 at Logic High		10	20	mW

Note 1: The relationship between the digital coding and the relative audio signal level is fixed as follows: a sine wave of 1 kHz and a nominal level of 0 dBm0 should be present at the audio output of the decoder when the appropriate character sequence shown below is applied to the decoder input.

TP3001 SYSTEM μ-LAW							
MSB	2	3	4	5	6	7	LSB
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

TP3002 SYSTEM A-LAW							
MSB	2	3	4	5	6	7	LSB
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

The resulting theoretical load capacity (T_{MAX}) is 3.17 dBm0 for the TP3001 system (μ-law) and 3.14 dBm0 for the TP3002 system (A-law).

Note 2: The PCM transmit filter must be AC coupled to the CODEC and a resistor of 24 kΩ or lower must be tied between analog in and analog ground. CODEC input impedance will then appear as 24 kΩ.

Note 3: PCM OUT and S_i are open drain outputs and will require external pull-up resistors to +6V maximum. 1 kΩ for PCM OUT and 10 kΩ for S_i are recommended when $F_{bo} = F_{bi} = 2.1$ MHz.

Note 4: Special care must be taken to assure that the substrate to ground pn junction is never forward biased. In cases where the negative power must be open circuited, it is recommended that a high current diode (1 amp Schottky) be placed between V^- and ground. It is further recommended that the power supply turn-on sequence be as follows: V^- or ground first, followed by V^+. Power supply turn-off should reverse the procedure.

Note 5: For TTL or LS compatibility, external pull-up resistors are required between the digital inputs and the TTL or LS logic power supply.

System Description (Refer to block diagrams)

The master clock for the system is F_C and must be run at 128 kHz which divides the 125 μs (1/8 kHz) time-frame into 16 time slots. The rising edge of the Output Sync (F_O) initiates the encoding cycle. The Input Sample and Hold Control (IN S/H CNTL) will go high for 19 μs thereby causing the input sample and hold to acquire a new input analog voltage. This acquired analog voltage is presented to a UNITY GAIN BUFFER located on the CMOS chip and then forwarded to the positive comparator input on the linear chip. The successive approximation will then begin. The SUCCESSIVE APPROXIMATION REGISTER will first load a zero code into the NON-LINEAR D/A CONVERTER. The output of the D/A converter goes to a second unity gain buffer and then to the negative input of the comparator on the linear chip. The comparator will then decide if the sampled analog voltage is positive or negative. If the analog input voltage is positive, the CONTROL LOGIC will pull the polarity control line high, which in turn will cause the voltage reference on the linear chip to deliver a positive reference voltage to the NON-LINEAR D/A CONVERTER. Conversely, if the analog input voltage is negative, a negative reference voltage will be applied to the NON-LINEAR D/A. The successive approximation will turn ON the second bit to the NON-LINEAR D/A CONVERTER and a decision is made to either leave that bit ON, or turn it OFF. The logic will then turn ON the third bit and make a decision to leave that bit ON or turn it OFF. In this way, the analog input voltage can be converted into the standard 8-bit μ-law or A-law code in 8 clock cycles.

At the end of the encode cycle the 8-bit code is loaded into the OUTPUT PCM BUFFER. The word is read out serially (MSB first) on PCM OUT by the Output Clock (F_{bo}) and the Output Sync (F_O).

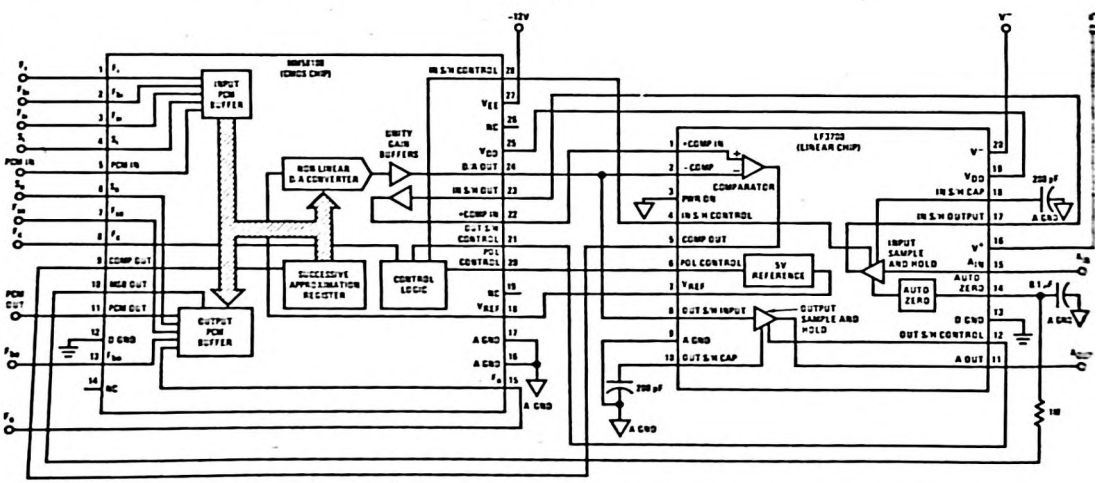
The incoming PCM word is read in serially (MSB first) on the PCM IN line by the Input Clock (F_{bi}) and the Input Sync (F_i). When the input word has been read in and F_i goes low, the system will immediately switch over to the decode mode. The current status of the successive approximation is temporarily stored while the decode word is delivered to the NON-LINEAR D/A CONVERTER. During decode, the ladder is shifted the required 1/2 LSB to minimize distortion. The CONTROL LOGIC will then raise the Output S/H Control line so that the Output Sample and Hold will acquire this new output voltage. After 4 clock cycles the circuit will return to the encode mode. The analog output of the system will therefore be a staircase type output with the associated sinx/x frequency distortion, *(Figure 3)*.

The system incorporates an AUTO-ZERO circuit to ensure a low DC offset for the encoding process, and very low idle channel noise. The encoded MSB (the sign bit) is latched on the MSB OUT pin. This signal then is fed to a simple external low pass RC filter (with a time constant of about 100 ms to 1 sec) and then to the AUTO-ZERO pin on the LF3700. The DC voltage on this pin will adjust the offset of the input sample and hold to correct for any offset voltage in the encoding path. This will also correct for up to ±20 mV DC offset voltage present in the analog input signal. This scheme simply forces equal numbers of positive and negative voltages over the long term.

There are 4 pins available in the TP3001 system for the insertion and extraction of signaling bits. The operation of these pins is covered in the timing diagrams.

System Block Diagrams

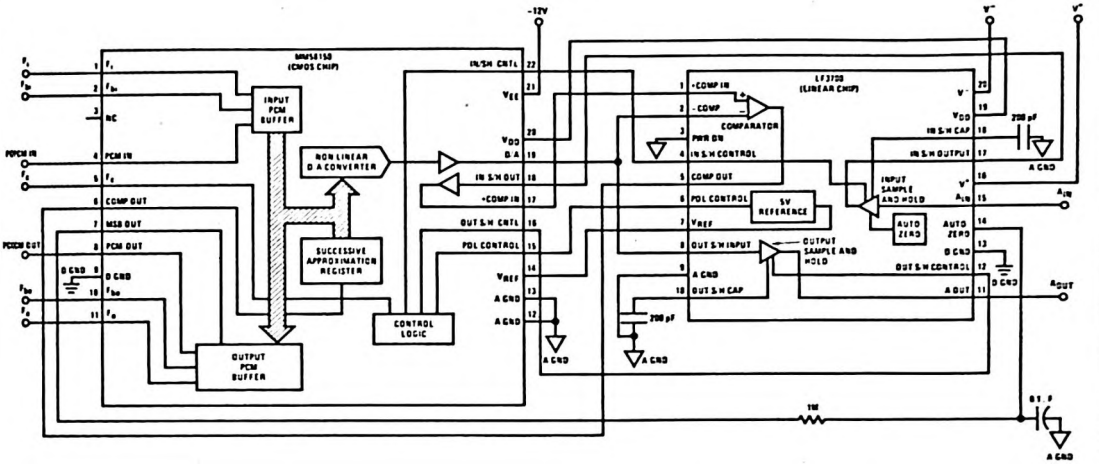
TP3001 System



Note. Pin 3 of the LF3700 should be connected to analog ground. Pin 3 of the LF3701 is a power down control; logic high (5V) is the power down standby mode for the TP3000 systems.

System Block Diagrams (Continued)

TP3002 System



Note. Pin 3 of the LF3700 should be connected to analog ground. Pin 3 of the LF3701 is a power down control; logic high (5V) is the power down standby mode for the TP3000 systems.

Ordering Information

SYSTEM	ORDER LINEAR PART:	AND CMOS PART:
TP3001 (μ-law)	LF3700D (D20A)	MM58100D (D28D)
TP3002 (A-law)	LF3700D (D20A)	MM58150D (D22B)

Description of Pin Functions

CMOS PIN FUNCTIONS:

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
1	1	F_i (INPUT SYNC)	When this line goes high, the data on the PCM IN line is shifted into the INPUT PCM BUFFER by F_{bi} (INPUT CLOCK). This line must be high for 8 clock pulses of F_{bi}. When F_i goes low, the incoming PCM word is loaded into the NON-LINEAR D/A CONVERTER and the OUTPUT SAMPLE AND HOLD is placed in the acquire mode. During decode, the D/A converter is shifted 1/2 LSB. After the decode is complete, the successive approximation will resume.
2	2	F_{bi} (INPUT PCM CLOCK)	The leading edges of this clock will serially shift the data on the PCM IN line into the INPUT PCM BUFFER when the F_i (INPUT SYNC) line is high.
3	–	F_{si} (MM58100 INPUT SIGNALING ENABLE)	When this line is high, the falling edge of F_i (INPUT SYNC) will transfer the LSB on the incoming PCM word to S_i (INPUT SIGNALING BIT). The PCM word is then decoded as a 7-bit code.
4	–	S_i (MM58100 INPUT SIGNALING BIT)	When F_{si} (INPUT SIGNALING ENABLE) is high, the LSB of the incoming PCM word is transferred to this line and latched by the falling edge of F_i (INPUT SYNC). An external pull-up resistor of 10k to the digital positive supply is required.

CMOS PIN FUNCTIONS: (Continued)

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
5	4	PCM IN	The incoming PCM word is received on this line.
6	–	S_o (MM58100 OUTPUT SIGNALING BIT)	When the F_{so} (OUTPUT SIGNALING ENABLE) line is high the LSB of the PCM word in the OUTPUT BUFFER is replaced by the logic state on this line.
7	–	F_{so} (MM58100 OUTPUT SIGNALING ENABLE)	When this line is high and F_O (OUTPUT SYNC) is low, the logic level on S_O (OUTPUT SIGNALING BIT) is transferred to the LSB of the OUTPUT PCM BUFFER.
8	5	F_C (MASTER CLOCK)	This is the principal clock of the CODEC system. All CODEC functions with the exception of F_i (INPUT SYNC) and F_{bi} (INPUT CLOCK) are synchronized to F_C. This clock frequency should be 128 kHz.
9	6	COMP OUT	This is the output of the analog comparator which is used in the successive approximation conversion.
10	7	MSB OUT	The encoded MSB appears on this line for use in the AUTO ZERO function.
11	8	PCM OUT	The result of the digital encoding is available on this line. A 1k external resistor to the digital positive supply is required.
12	9	D GND (DIGITAL GND)	All digital signals should be referenced to this line.

Description of Pin Functions (Continued)

CMOS PIN FUNCTIONS: (Continued)

MM58100 PIN NO.	MM58150 PIN NO.	NAME	FUNCTION
13	10	F_{bo} (OUTPUT PCM CLOCK)	The falling edges of this clock will serially shift the PCM word in the PCM OUTPUT BUFFER to the PCM OUT line.
14	–	No Connection	
15	11	F_o (OUTPUT SYNC)	When this line goes high, the output PCM word can be shifted out by F_{bo} (OUTPUT CLOCK). This line must be high for 8 clock pulses of F_{bo}. When F_o goes high, the following sequence is initiated: the INPUT SAMPLE AND HOLD first acquires the ANALOG IN voltage and a successive approximation conversion is made on that voltage using the NON-LINEAR D/A CONVERTER and the COMPARATOR. The resulting 8-bit PCM word is then loaded into the OUTPUT PCM BUFFER.
16	12	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
17	13	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
18	14	V_{REF}	This is the $+V_{REF}$ or the $-V_{REF}$ for the NON-LINEAR D/A CONVERTER.
19	–	No Connection	
20	15	POL CNTL (POLARITY CONTROL)	This is the digital command for $+V_{REF}$ or $-V_{REF}$.
21	16	OUT S/H CNTL (OUTPUT SAMPLE AND HOLD CONTROL)	This is the digital command for the OUTPUT SAMPLE AND HOLD to acquire a new voltage.
22	17	+COMP IN (NON-INVERTING COMPARATOR INPUT)	This is the output of the buffer amplifier for the input sample and hold. This is connected to the +COMP IN pin on the linear chip.
23	18	IN S/H OUT (OUTPUT OF THE INPUT SAMPLE AND HOLD)	This is the input of the buffer amplifier for the input sample and hold. This is connected to the output of the input sample and hold on the linear chip.
24	19	D/A OUT	This is the output voltage of the NON-LINEAR D/A CONVERTER.
25	20	V_{DD}	This is the positive voltage supply for the digital chip which is provided by the analog chip.
26	–	No Connection	
27	21	V_{EE}	This is the negative supply voltage for the digital chip (–12V).
28	22	IN S/H CNTL (INPUT SAMPLE AND HOLD CONTROL)	This is the digital command for the INPUT SAMPLE AND HOLD to acquire a new voltage.

LINEAR PIN FUNCTIONS:

LF3700 PIN NO.	NAME	FUNCTION
1	+COMP IN (NON-INVERTING COMPARATOR INPUT)	This is tied to the +COMP IN pin on the CMOS chip.
2	–COMP IN (INVERTING COMPARATOR INPUT)	This is tied to the D/A OUT pin on the CMOS chip and the OUTPUT SAMPLE AND HOLD INPUT pin on the linear chip.
3	POWER DOWN	Connect to Analog Gnd – LF3700 (LF3701 see note System Block Diagram)
4	IN S/H CNTL (INPUT SAMPLE AND HOLD CONTROL)	This is tied to the IN S/H CNTL pin on the CMOS chip.
5	COMP OUT (COMPARATOR OUTPUT)	This is tied to the COMP OUT pin on the CMOS chip.
6	POL CNTL (POLARITY CONTROL)	This is tied to the POL CNTL pin on the CMOS chip.
7	V_{REF}	This is tied to V_{REF} on the CMOS chip.
8	OUT S/H INPUT (INPUT TO OUTPUT SAMPLE AND HOLD)	This is the analog input to the OUTPUT SAMPLE AND HOLD. This should be connected to the D/A OUT pin on the CMOS chip and the inverting comparator input pin on the linear chip.
9	A GND (ANALOG GROUND)	All analog signals should be referenced to this line.
10	OUT S/H CAP (OUTPUT SAMPLE AND HOLD CAPACITOR)	A low leakage, 200 pF capacitor should be connected from this line to ANALOG GROUND.
11	A OUT (ANALOG OUT)	This is the output of the OUTPUT SAMPLE AND HOLD.
12	OUT S/H CNTL (OUTPUT SAMPLE AND HOLD CONTROL)	This is tied to the OUT S/H CNTL pin on the CMOS chip.
13	D GND (DIGITAL GROUND)	All digital signals should be referenced to this line.
14	AUTO Z (AUTO ZERO)	This is connected to the MSB OUT line of the CMOS chip after an external low pass filter.
15	A IN (ANALOG IN)	This is the appropriately filtered analog input.
16	V^+	This is the positive supply voltage for the analog chip.
17	IN S/H OUTPUT (OUTPUT OF INPUT SAMPLE AND HOLD)	This is the analog output voltage of the INPUT SAMPLE AND HOLD. This is tied to the IN S/H OUT pin on the CMOS chip.
18	IN S/H CAP (INPUT SAMPLE AND HOLD CAPACITOR)	A low leakage, 200 pF capacitor should be connected from this line to analog ground.
19	V_{DD}	This is the positive supply voltage for the CMOS chip. This is tied to V_{DD} on the CMOS chip.
20	V^-	This is the negative supply for the linear chip.

Typical Performance Characteristics

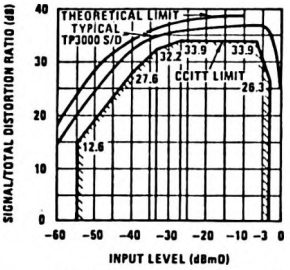


FIGURE 1. Typical Signal/ Total Distortion Ratio as a Function of Input Level with a White Noise Source

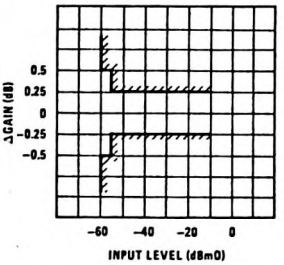


FIGURE 2. Maximum Gain Tracking Error (ΔGain) as a Function of Input Level with a White Noise Source

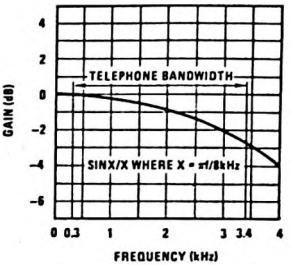
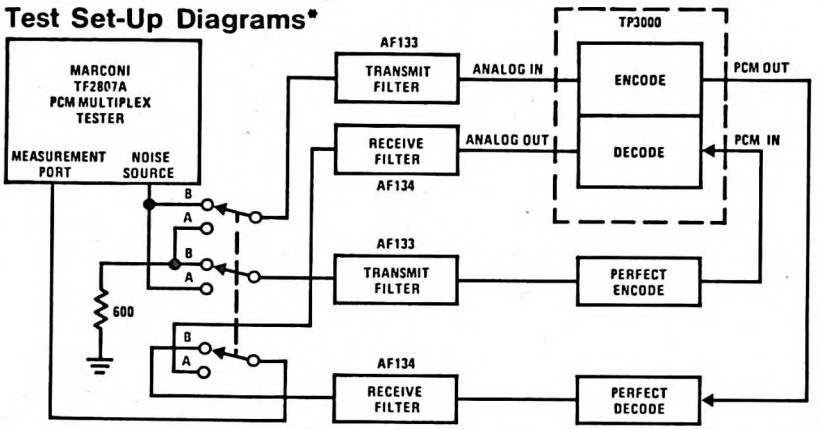


FIGURE 3. Output sinx/x Frequency Response

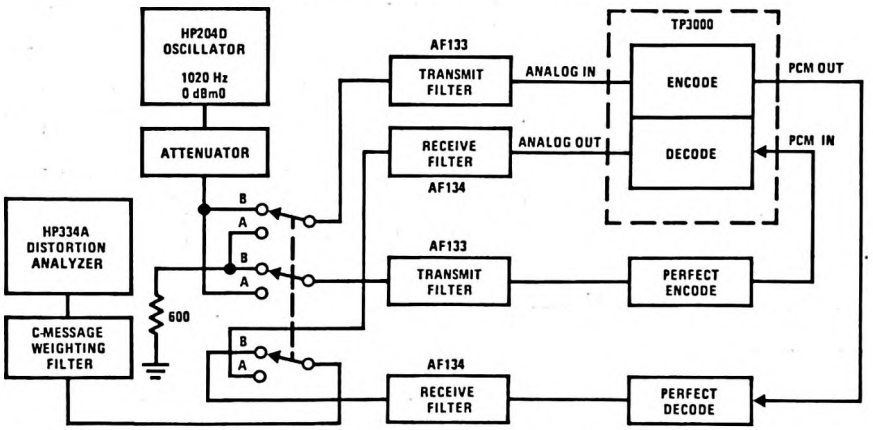
Test Set-Up Diagrams*



The Marconi TF2807A's noise output has a probability distribution of amplitude approximating a Gaussian distribution which is band limited to conform with the latest CCITT recommendations.

Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

FIGURE 4. Test Set-Up for Signal-to-Distortion and Gain Tracking Using a Noise Source

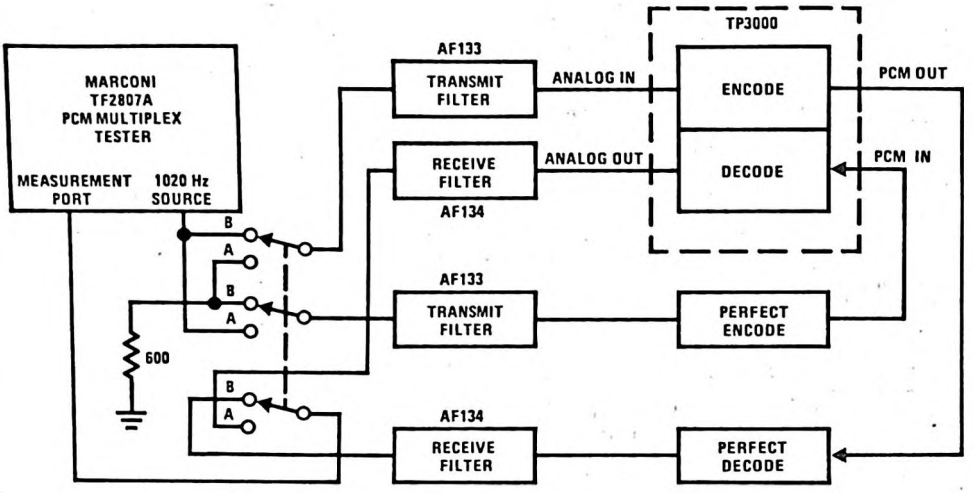


Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

FIGURE 5. Test Set-Up for Signal-to-Distortion Using a 1020 Hz Signal

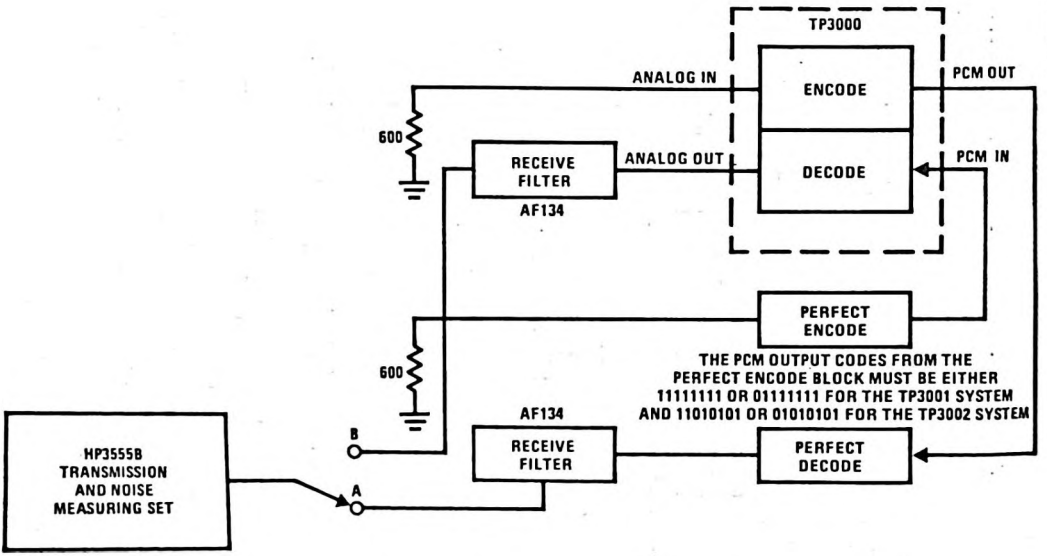
*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)



Switch position A - Perfect encode; decode TP3000
Switch position B – Encode TP3000; perfect decode

FIGURE 6. Test Set-Up for Gain Tracking Using 1020 Hz Signal

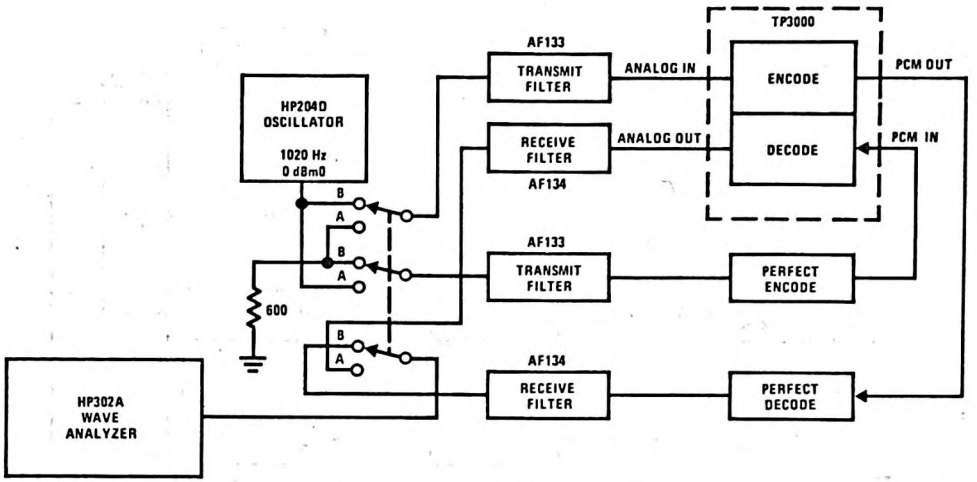


Determine the 0 dBm0 level on the HP3555B and then measure the idle channel noise with the HP3555B in the C-MSG-mode. The noise in dBrnc0 is 90 dBm0-A, where A is the idle channel noise measurement down from the 0 level (in dB).

FIGURE 7. Test Set-Up for Idle Channel Noise

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)



The output at any frequency (except 1020 Hz) should be at least 40 dB down. The two frequencies of interest are the second and third harmonics (2040 Hz and 3060 Hz).

Switch position A -- Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

FIGURE 8. Test Set-Up for Single Frequency Distortion

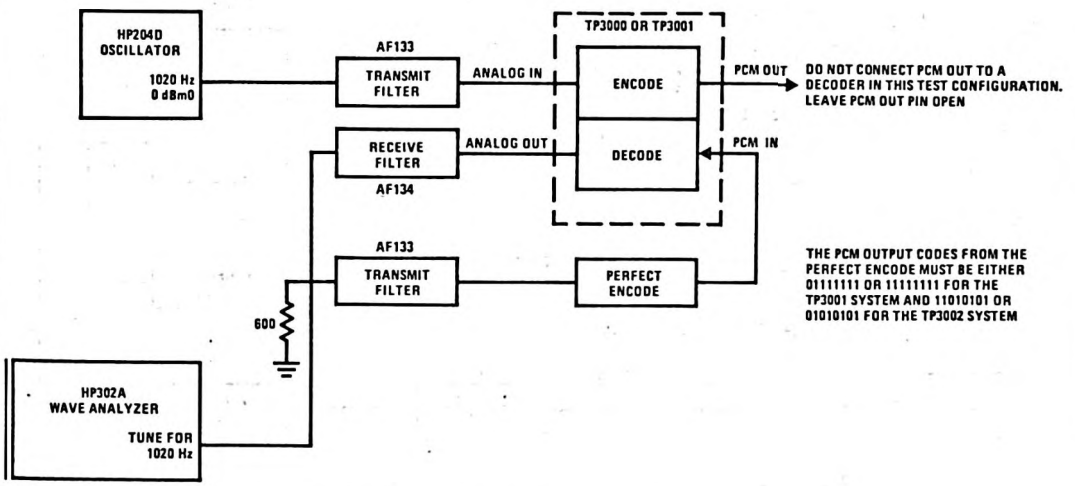


FIGURE 9. Test Set-Up for Go-to-Return Crosstalk

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

Test Set-Up Diagrams* (Continued)

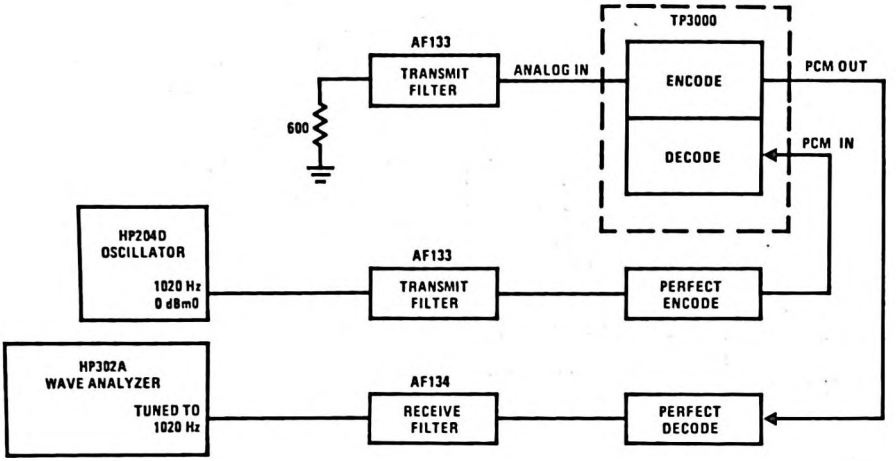
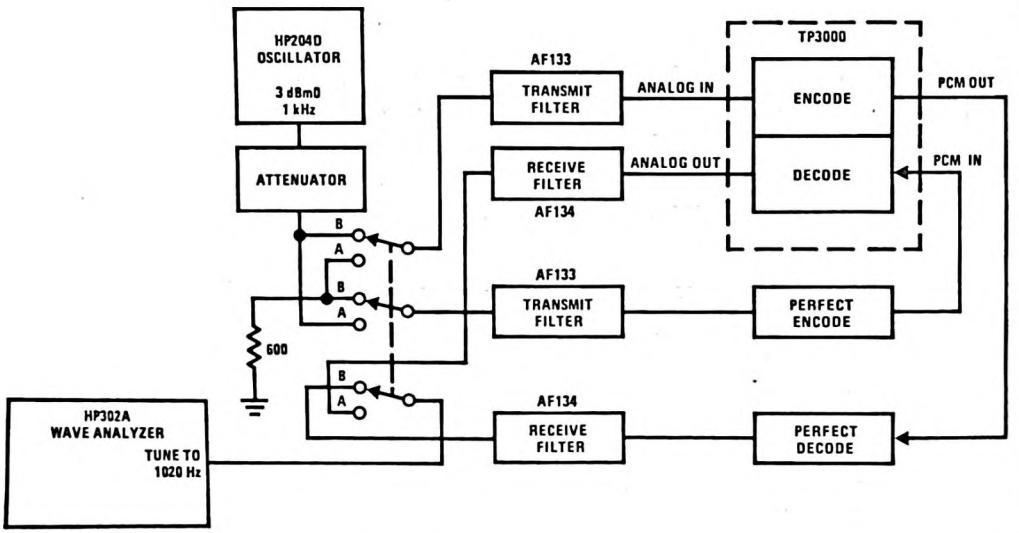


FIGURE 10. Test Set-Up for Return-to-Go Crosstalk



Switch position A — Perfect encode; decode TP3000
Switch position B — Encode TP3000; perfect decode

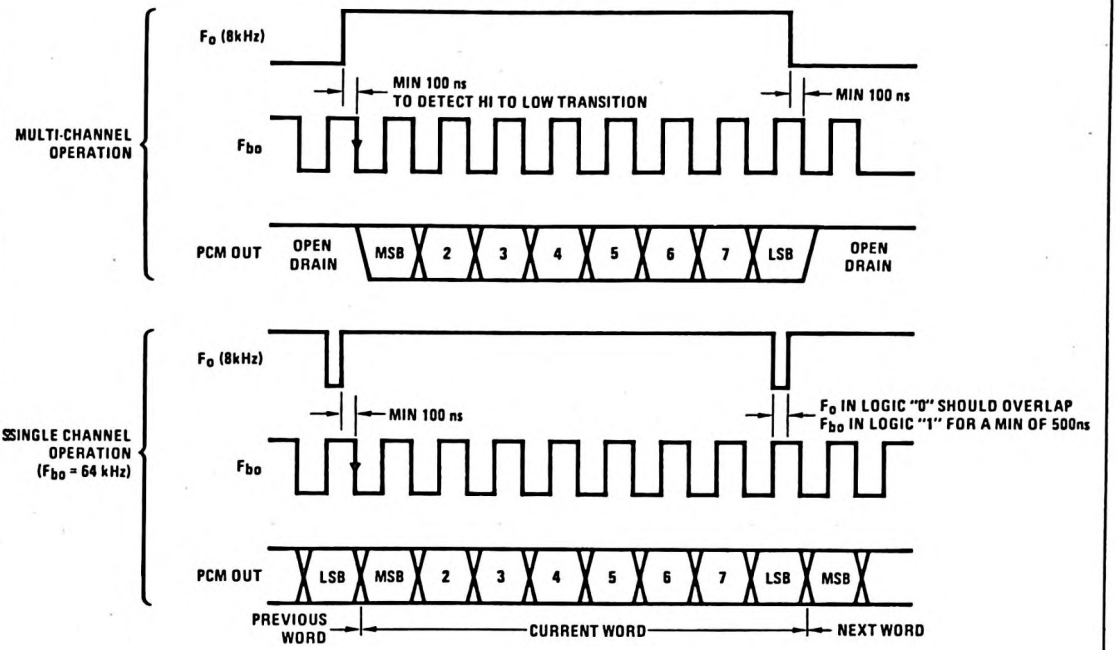
FIGURE 11. Test Set-Up for Interchannel Crosstalk

*Perfect encode or decode is μ-law when testing TP3001 and A-law when testing TP3002

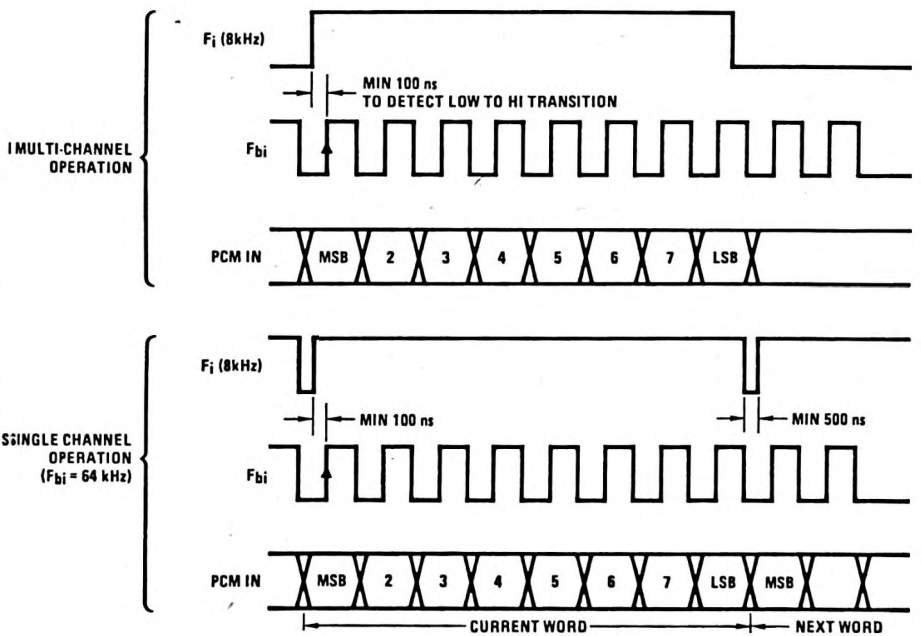
Timing Diagrams

SYSTEM TIMING

F_o, F_{bo} and PCM OUT Relationships



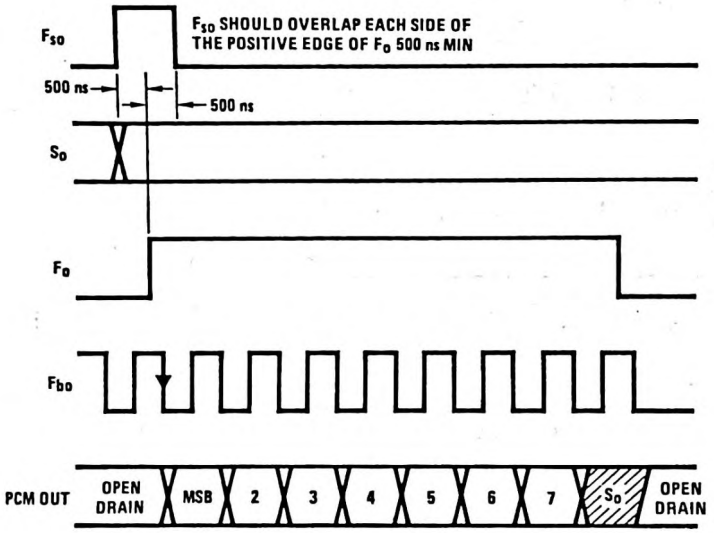
F_i, F_{bi} and PCM IN Relationships



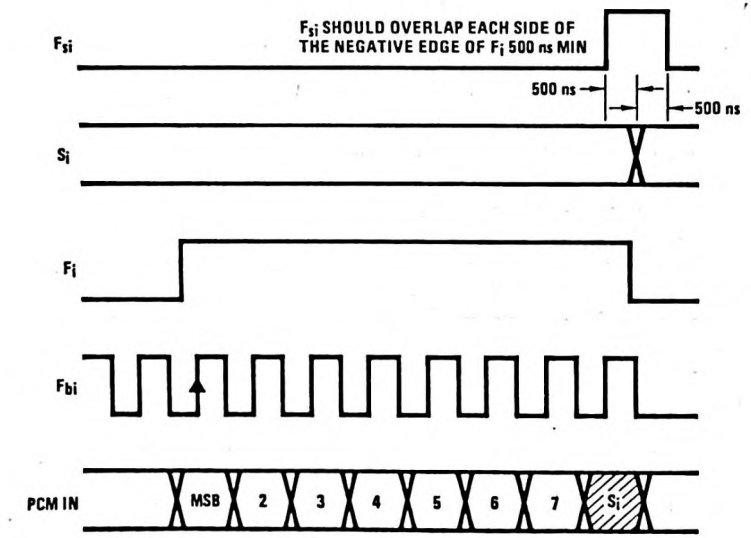
Timing Diagrams (Continued)

SIGNALING
(TP3001 Only)

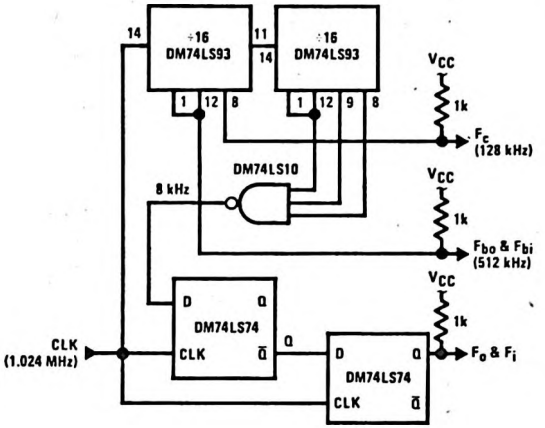
F_{so}, S_o, F_o Timing Relationships



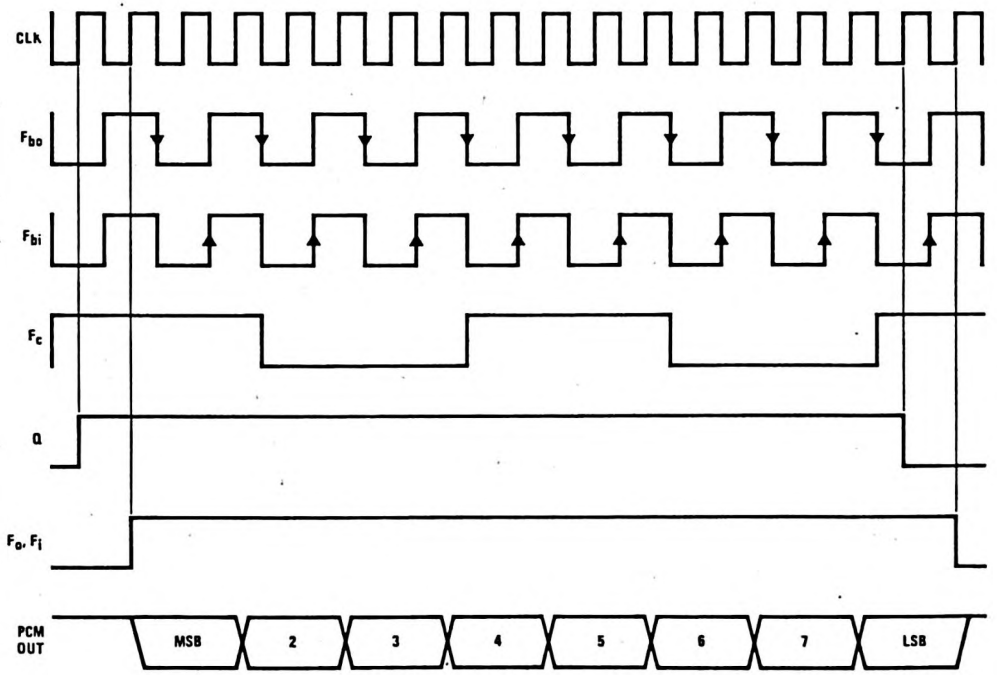
F_{si}, S_i, F_i Timing Relationships



Timing Generator



Timing Generator Outputs



Section 3

Digital-to-Analog Converters

3

National Semiconductor

AD7520 10-Bit Binary Multiplying D/A Converter
AD7521 12-Bit Binary Multiplying D/A Converter

General Description

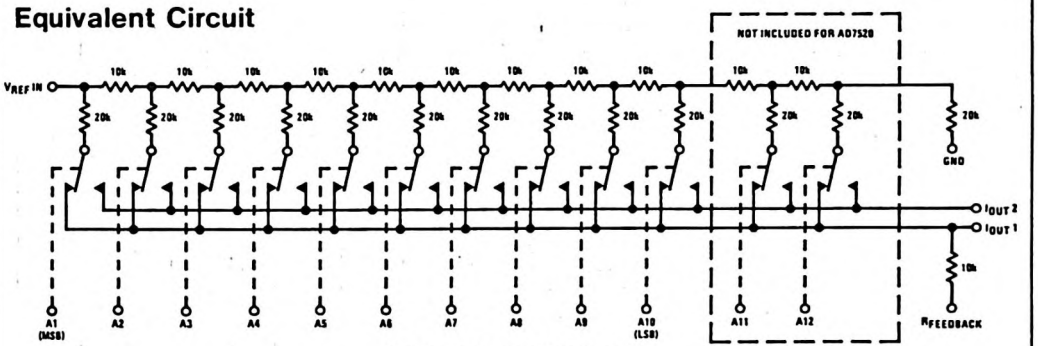
The AD7520 and the AD7521 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (typically 0.0002%/°C linearity error temperature coefficient). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference.

This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity. The AD7520L, AD7520K, and AD7520J are direct replacements for the 10-bit resolution AD7520 and AD7530 family. The AD7521K, AD7521J and AD7521L are direct replacements for the 12-bit resolution AD7521 and AD7531 family. For more information, see DAC1020 data sheet.

Features

- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—600 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

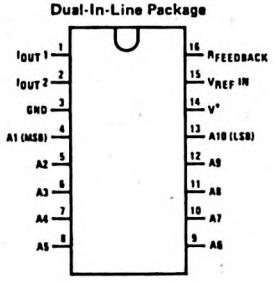
Equivalent Circuit



Switches shown in digital high state

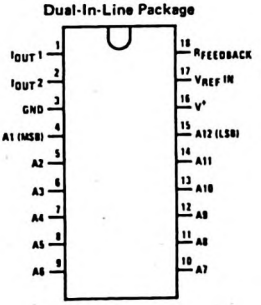
Connection Diagrams

AD7520
Dual-In-Line Package



TOP VIEW

AD7521
Dual-In-Line Package



TOP VIEW

Ordering Information

10-Bit D/A Converter

ACCURACY	OPERATING TEMPERATURE RANGE	
	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
0.05%	AD7520UD	AD7520LD
0.10%	AD7520TD	AD7520KD
0.20%	AD7520SD	AD7520JD

*See NS Package D16C

12-Bit D/A Converter

ACCURACY	OPERATING TEMPERATURE RANGE	
	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
0.05%	AD7521UD	AD7521LD
0.10%	AD7521TD	AD7521KD
0.20%	AD7521SD	AD7521JD

*See NS Package D18A

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature Range

	MIN	MAX	UNIT
Temperature (T_A)			
AD7520L, AD7520K	0	+70	°C
AD7520J, AD7521L	0	+70	°C
AD7521K, AD7521J	0	+70	°C
AD7520S, AD7520T	−55	+125	°C
AD7520U, AD7521S	−55	+125	°C
AD7521T, AD7521U	−55	+125	°C

Electrical Characteristics (V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	AD7520L, AD7520K, AD7520J			AD7521L, AD7521K, AD7521J			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$, $-10V \le V_{REF} \le +10V$, (Note 1)							
10-bit Parts	AD7520L, AD7520U, AD7521L, AD7521U			0.05			0.05	% FS
9-bit Parts	AD7520T, AD7520K, AD7521T, AD7521K			0.10			0.10	% FS
8-bit Parts	AD7520S, AD7520J, AD7521S, AD7521J			0.20			0.20	% FS
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Note 1)		0.0002			0.0002		% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3			0.3		% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current								
I_{OUT1}	All Digital Inputs Low, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
I_{OUT2}	All Digital Inputs High, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$		0.005			0.005		% FS/V
V_{REF} Input Resistance		5	10	20	5	10	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
Output Capacitance								
I_{OUT1}	All Digital Inputs Low		37			37		pF
	All Digital Inputs High		120			120		pF
I_{OUT2}	All Digital Inputs Low		120			120		pF
	All Digital Inputs High		37			37		pF
Digital Input	(Note 1)							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$,			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \le T_A \le T_{MAX}$							
	Digital Input High		1	100		1	100	µA
	Digital Input Low		−50	−200		−50	−200	µA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range		5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V.

Note 2: Using internal feedback resistor.

Note 3: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. For every millivolt offset between I_{OUT1} or I_{OUT2}, 0.005% linearity error will be introduced.

National Semiconductor

Digital-to-Analog Converters

DAC0800(LMDAC08) 8-Bit Digital-to-Analog Converter

general description

The DAC08 is a monolithic 8-bit high-speed current-output digital-to-analog converter (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC08 also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC08 will accept TTL levels with the logic threshold pin, V_{LC}, pin 1 grounded. Simple adjustments of the V_{LC} potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800L, DAC0802L, DAC0800LC, DAC0801LC and DAC0802LC are a direct replacement for the DAC08, DAC08A, DAC08C, DAC08E and DAC08H, respectively.

features

- Fast settling output current — 100 ns
- Full scale error — ±1 LSB
- Nonlinearity over temperature — ±0.1%
- Full scale current drift — ±10 ppm/°C
- High output compliance — −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

typical applications

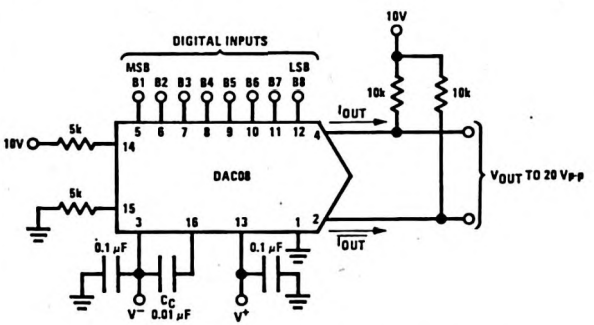
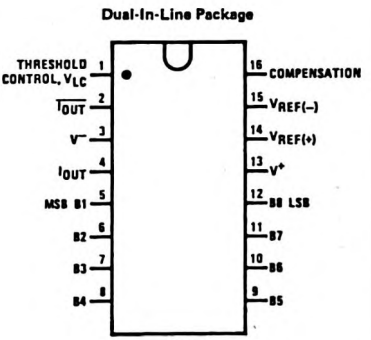


FIGURE 1. ±20 Vp-p Output Digital-to-Analog Converter

connection diagram



ordering information

NON LINEARITY	TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
±0.1% FS	$-55°C \le T_A \le +125°C$	DAC0802LD	LMDAC08AD	DAC0800LAJ	LMDAC08J		
±0.1% FS	$0°C \le T_A \le +70°C$			DAC0802LCJ	LMDAC08HJ	DAC0802LCN	LMDAC08HN
±0.19% FS	$-55°C \le T_A \le +125°C$	DAC0800LD	LMDAC08D	DAC0800LJ	LMDAC08J		
±0.19% FS	$0°C \le T_A \le +70°C$			DAC0800LCJ	LMDAC08EJ	DAC0800LCN	LMDAC08EN
±0.39% FS	$0°C \le T_A \le +70°C$			DAC0801LCJ	LMDAC08CJ	DAC0801LCN	LMDAC08CN

*Note. Devices may be ordered by using either order number.

absolute maximum ratings

Supply Voltage	±18V or 36V
Power Dissipation (Note 1)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs	*Figure 24*
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

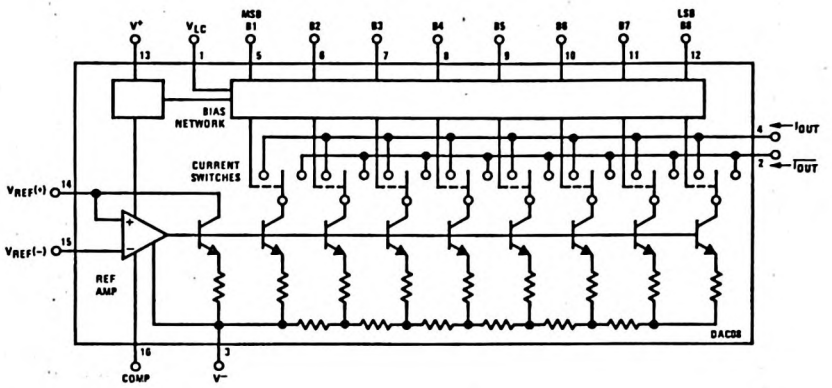
	MIN	MAX	UNITS
Temperature (T_A)			
DAC0802LA, LMDAC08A	−55	+125	°C
DAC0800L, LMDAC08	−55	+125	°C
DAC0800LC, LMDAC08E,	0	+70	°C
DAC0801LC, LMDAC08C,	0	+70	°C
DAC0802LC, LMDAC08H	0	+70	°C

electrical characteristics (V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

	PARAMETER	CONDITIONS	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±1/2 LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A = 25°C										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCIFS	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change < 1/2 LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −7V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	V_{LC} = 0V										
I_{IL}	Logic "0"	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^- = −15V	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 24)*		8.0			8.0			8.0		mA/μs
PSSIFS+	Power Supply Sensitivity	4.5V ≤ V^+ ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
PSSIFS−		−4.5V ≤ V^- ≤ 18V		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
		I_{REF} = 1 mA										
	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
I^+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		V_S = 5V, −15V, I_{REF} = 2 mA										
I^+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I^-				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		V_S = ±15V, I_{REF} = 2 mA										
I^+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I^-				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
		5V, −15V, I_{REF} = 2 mA		108	136		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

Note 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 100°C. For operating at elevated temperatures, devices in the dual-in-line J or D package must be derated based on a thermal resistance of 100°C/W, junction to ambient, 175°C/W for the molded dual-in-line N package.

block diagram



equivalent circuit

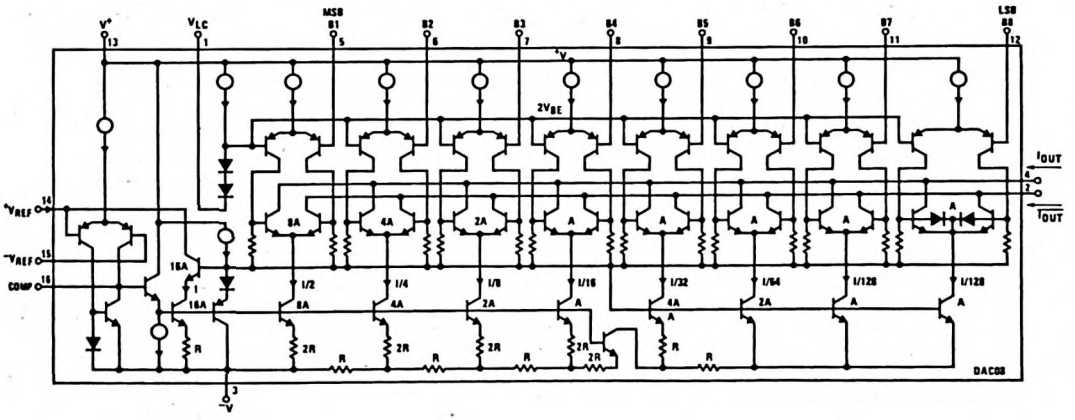


FIGURE 2

typical performance characteristics

Full Scale Current vs Reference Current

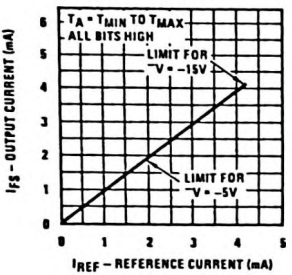


FIGURE 3

LSB Propagation Delay vs I_{FS}

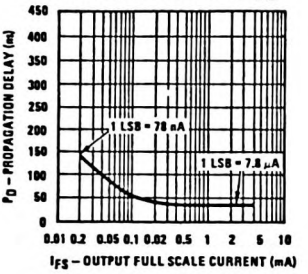
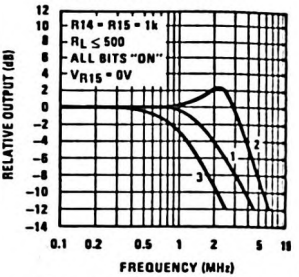


FIGURE 4

Reference Input Frequency Response



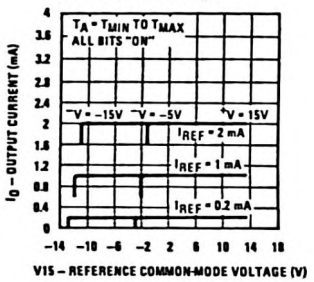
Curve 1: C_C = 15 pF, V_{IN} = 2 V_{p-p} centered at 1V.

Curve 2: C_C = 15 pF, V_{IN} = 50 mV_{p-p} centered at 200 mV.

Curve 3: C_C = 0 pF, V_{IN} = 100 mV_{p-p} at 0V and applied through 50 Ω connected to pin 14. 2V applied to R14.

FIGURE 5

Reference Amp Common-Mode Range


$T_A = T_{MIN}$ TO T_{MAX}
ALL BITS "ON"
−V = −15V
−V = −5V
+V = 15V
I_{REF} = 2 mA
I_{REF} = 1 mA
I_{REF} = 0.2 mA
I_O – OUTPUT CURRENT (mA)
V15 – REFERENCE COMMON-MODE VOLTAGE (V)

Note. Positive common-mode range is always (V+) − 1.5V.

FIGURE 6

Logic Input Current vs Input Voltage

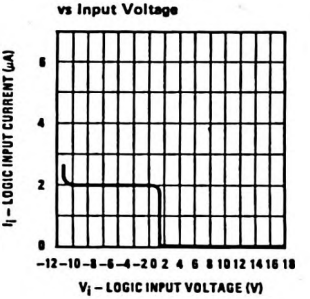


FIGURE 7

$V_{TH} - V_{LC}$ vs Temperature

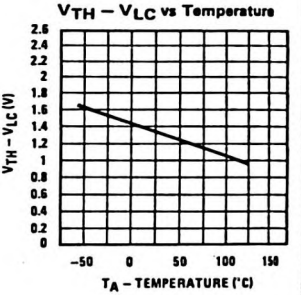


FIGURE 8

Output Current vs Output Voltage (Output Voltage Compliance)

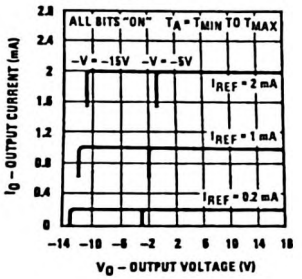


FIGURE 9

Output Voltage Compliance vs Temperature

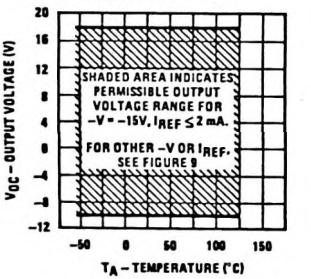
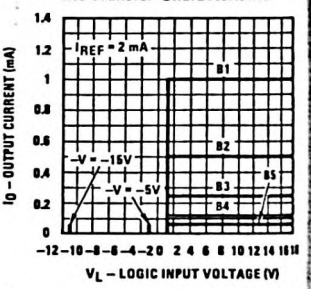

SHADED AREA INDICATES PERMISSIBLE OUTPUT VOLTAGE RANGE FOR −V = −15V, $I_{REF} \leq$ 2 mA.
FOR OTHER −V OR I_{REF}, SEE FIGURE 9
V_{OC} – OUTPUT VOLTAGE (V)
T_A – TEMPERATURE (°C)

FIGURE 10

Bit Transfer Characteristics



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to be between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

FIGURE 11

typical performance characteristics (Continued)

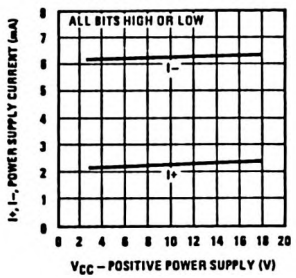


FIGURE 12

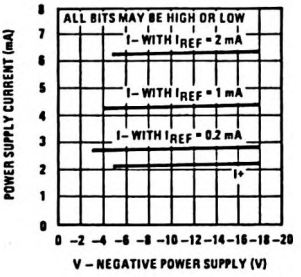

Power Supply Current vs −V
ALL BITS MAY BE HIGH OR LOW
I− WITH IREF = 2 mA
I− WITH IREF = 1 mA
I− WITH IREF = 0.2 mA
I+
POWER SUPPLY CURRENT (mA)
V – NEGATIVE POWER SUPPLY (V)

FIGURE 13

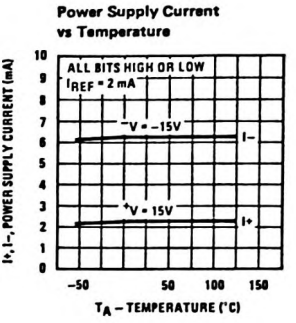
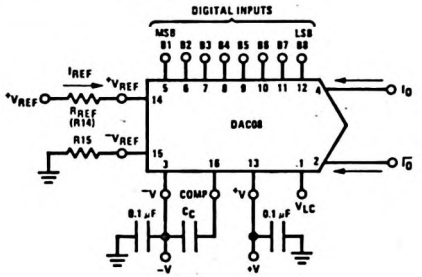


FIGURE 14

typical applications (Continued)



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:
$V_{REF} = 10.000V$
$R_{REF} = 5.000k$
$R15 \approx R_{REF}$
$C_C = 0.01\ \mu F$
$V_{LC} = 0V$ (Ground)

FIGURE 15. Basic Positive Reference Operation

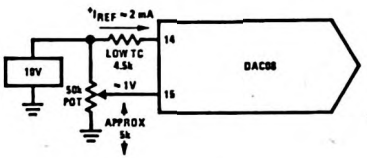
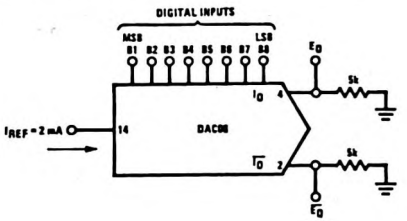


FIGURE 16. Recommended Full Scale Adjustment Circuit

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

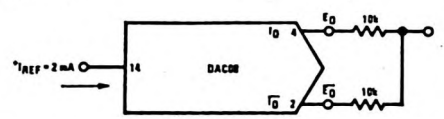
FIGURE 17. Basic Negative Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

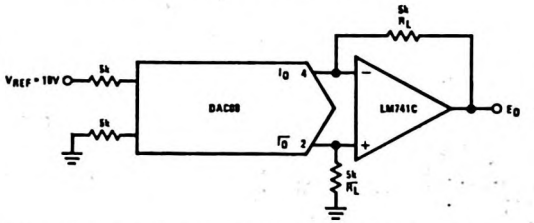
FIGURE 18. Basic Unipolar Negative Operation

typical applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

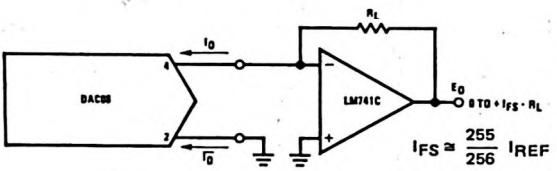
FIGURE 19. Basic Bipolar Output Operation



If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

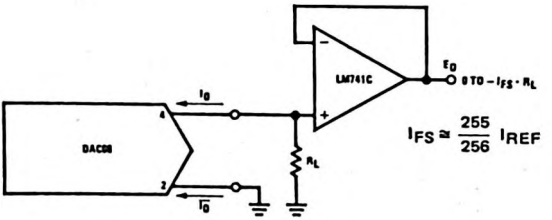
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

FIGURE 20. Symmetrical Offset Binary Operation



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

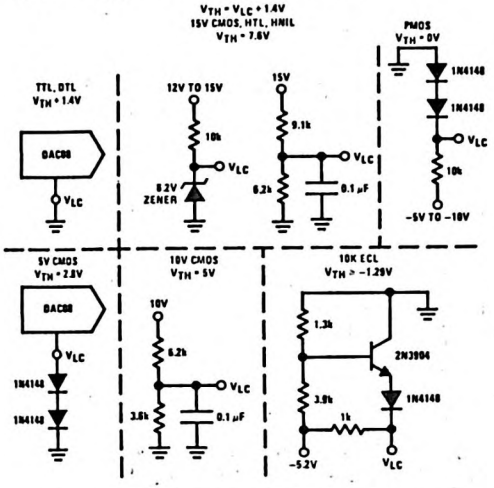
FIGURE 21. Positive Low Impedance Output Operation



For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

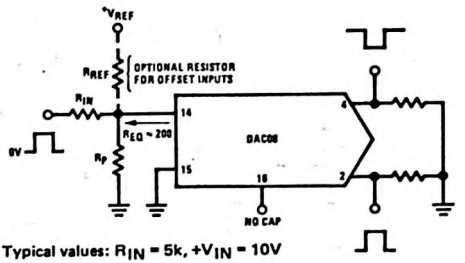
FIGURE 22. Negative Low Impedance Output Operation

typical applications (Continued)



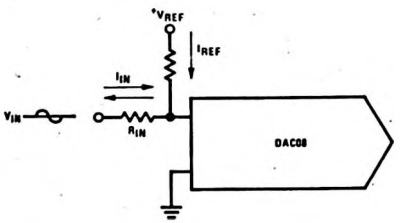
Note. Do not exceed negative logic input range of DAC.

FIGURE 23. Interfacing with Various Logic Families

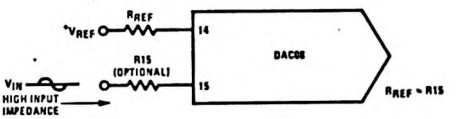


Typical values: R_{IN} = 5k, $+V_{IN}$ = 10V

FIGURE 24. Pulsed Reference Operation



(a) $I_{REF} \geq$ peak negative swing of I_{IN}



(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

FIGURE 25. Accomodating Bipolar References

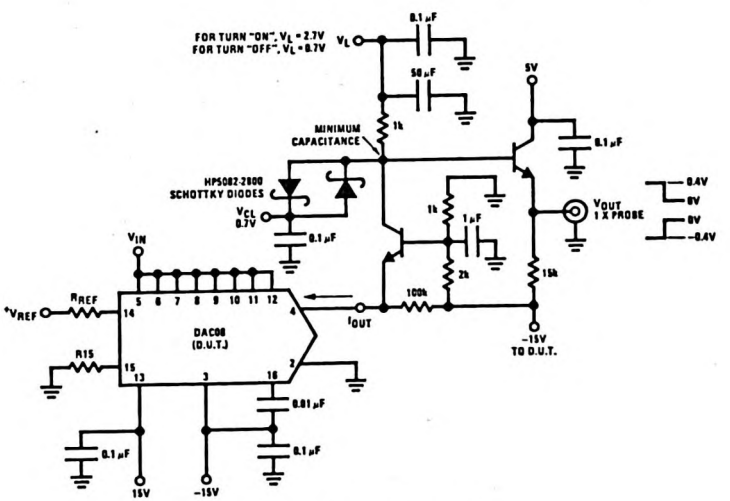
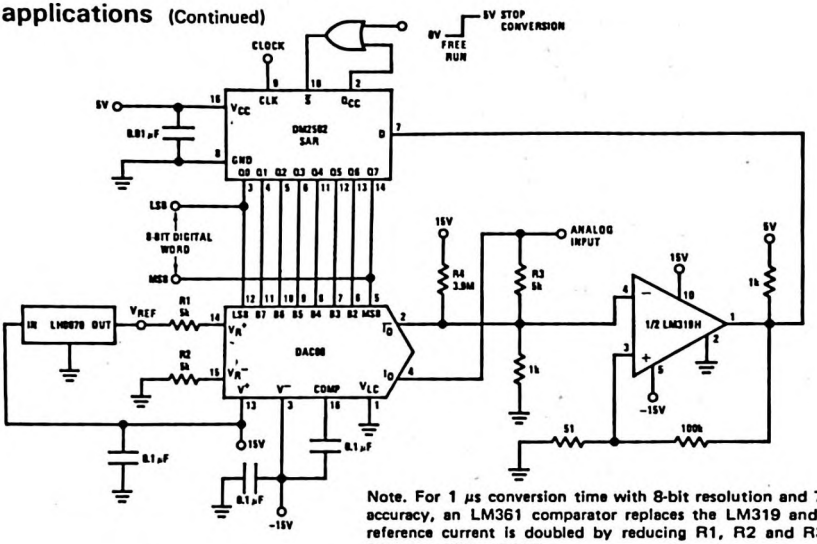


FIGURE 26. Settling Time Measurement

typical applications (Continued)



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 27. A Complete 2 μs Conversion Time, 8-Bit A/D Converter

National Semiconductor

Digital-to-Analog Converters

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

general description

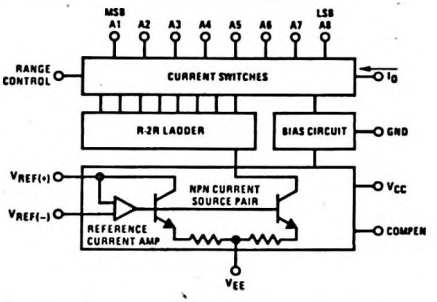
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

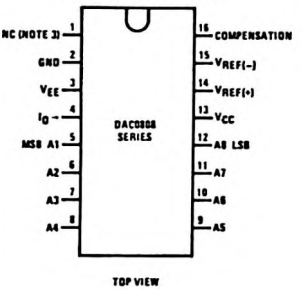
features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

block and connection diagrams



Dual-In-Line Package



typical application

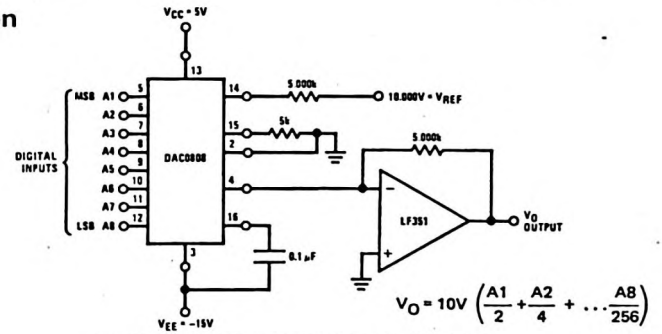


FIGURE 1. ±10V Output Digital to Analog Converter

ordering information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LD	LM1508D-8	DAC0808LJ	LM1508J-8		
8-bit	$0°C \leq T_A \leq +75°C$			DAC0808LCJ	LM1408J-8	DAC0808LCN	LM1408N-8
7-bit	$0°C \leq T_A \leq +75°C$			DAC0807LCJ	LM1408J-7	DAC0807LCN	LM1408N-7
6-bit	$0°C \leq T_A \leq +75°C$			DAC0806LCJ	LM1408J-6	DAC0806LCN	LM1408N-6

*Note. Devices may be ordered by using either order number.

absolute maximum ratings (T_A = 25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	5.5 V_{DC}
V_{EE}	−16.5 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
DAC0808L	−55°C ≤ T_A ≤ +125°C
DAC0808LC Series	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808L: T_A = −55°C to +125°C, DAC0808LC, DAC0807LC, DAC0806LC, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

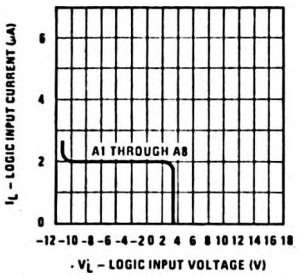
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 1)				±0.39	%
	DAC0806LC (LM1408-6), (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−5	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance Pin 1 Grounded, V_{EE} Below −10V	E_r ≤ 0.19%, T_A = 25°C			−0.55, +0.4 −5.0, +0.4	V_{DC} V_{DC}
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*		8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

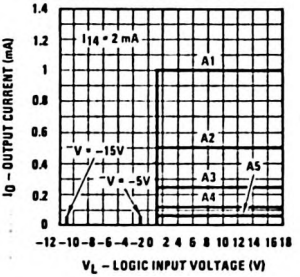
typical performance characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

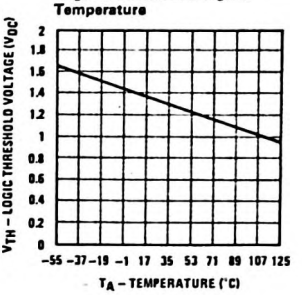
Logic Input Current vs Input Voltage



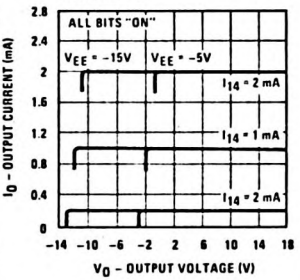
Bit Transfer Characteristics



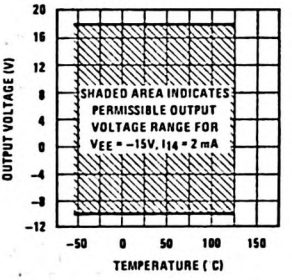
Logic Threshold Voltage vs Temperature



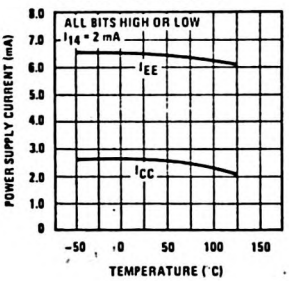
Output Current vs Output Voltage (Output Voltage Compliance)



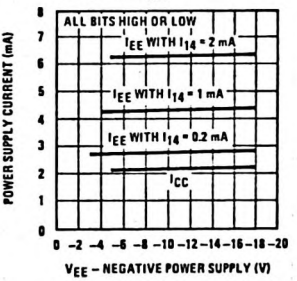
Output Voltage Compliance vs Temperature



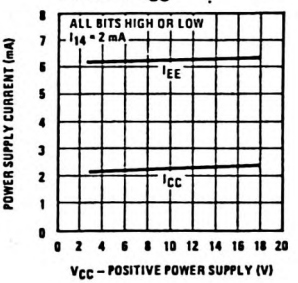
Typical Power Supply Current vs Temperature



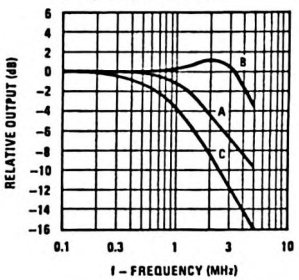
Typical Power Supply Current vs V_{EE}


ALL BITS HIGH OR LOW
IEE WITH I14 = 2 mA
IEE WITH I14 = 1 mA
IEE WITH I14 = 0.2 mA
ICC
POWER SUPPLY CURRENT (mA)
VEE – NEGATIVE POWER SUPPLY (V)

Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

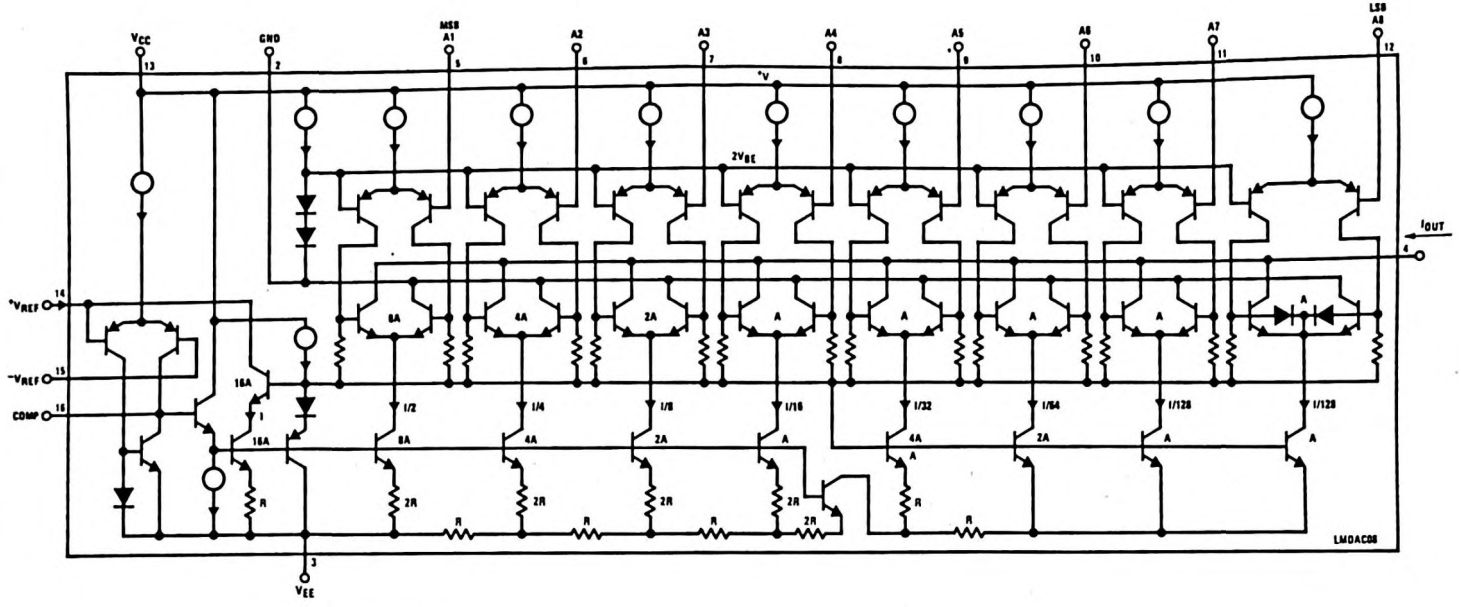
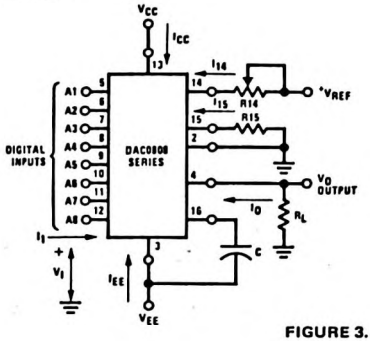


FIGURE 2. Equivalent Circuit of the DAC0808 Series

ıtest circuits



V_I and I_I apply to inputs A1—A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

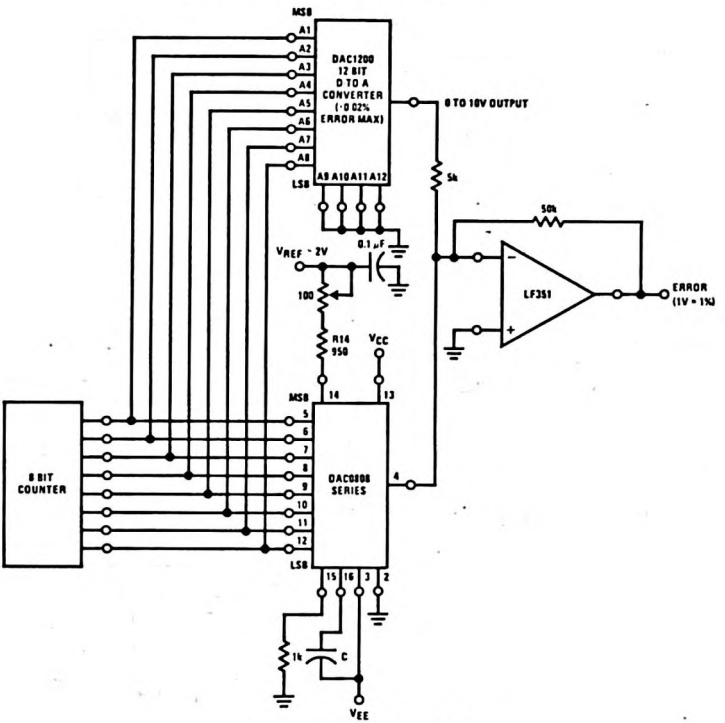


FIGURE 4. Relative Accuracy Test Circuit

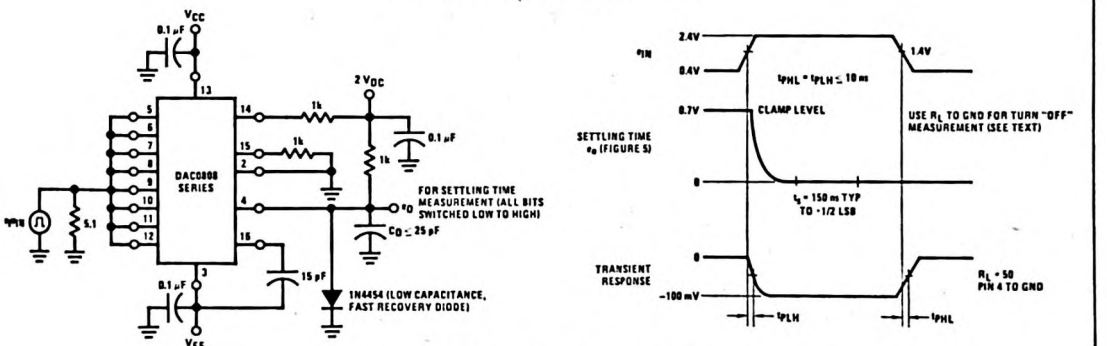


FIGURE 5. Transient Response and Settling Time

test circuits (Continued)

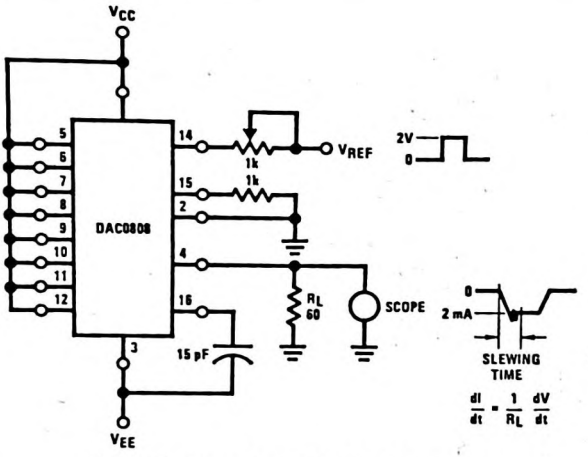


FIGURE 6. Reference Current Slew Rate Measurement

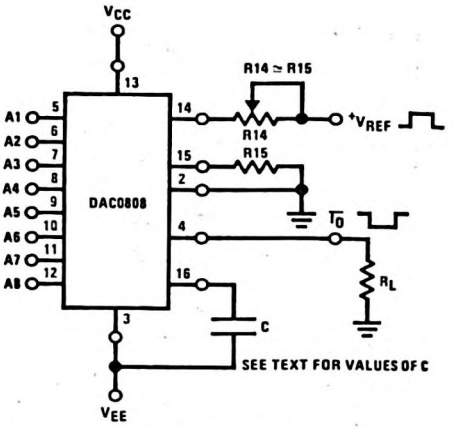


FIGURE 7. Positive V_{REF}

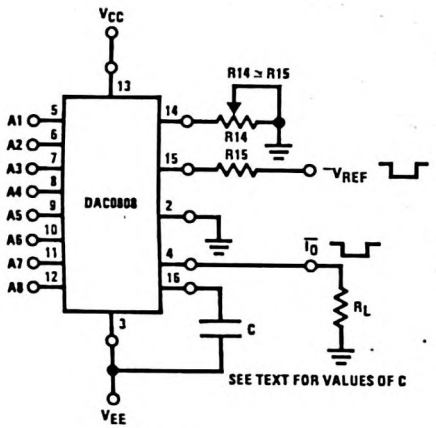


FIGURE 8. Negative V_{REF}

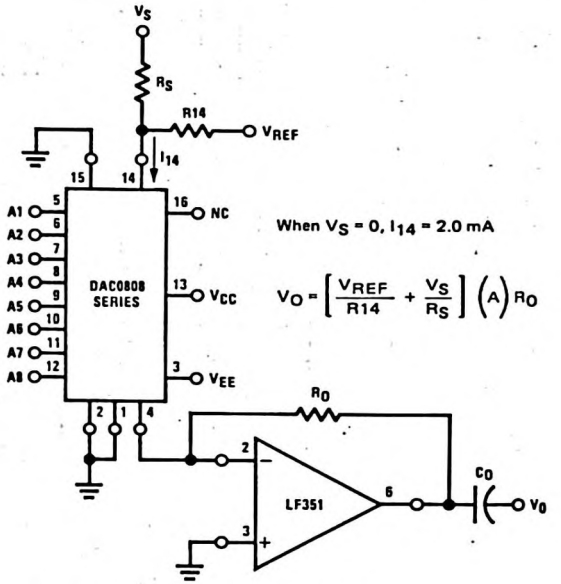


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit

application hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

application hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactoy test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

Digital-to-Analog Converters

DAC1020 10-Bit Binary Multiplying D/A Converter
DAC1220 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

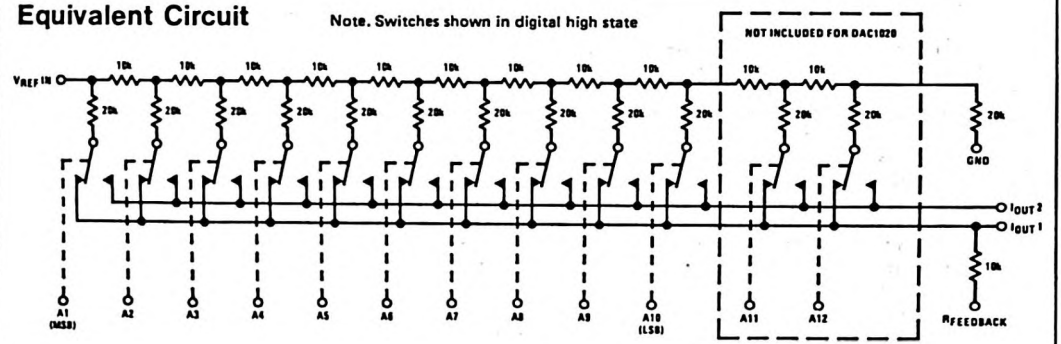
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guarenteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021, and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 family. The DAC1220, DAC1221, and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

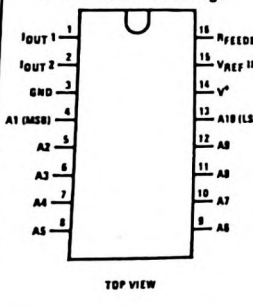
Equivalent Circuit

Note. Switches shown in digital high state



Connection Diagrams

DAC102X
Dual-In-Line Package



DAC122X
Dual-In-Line Package

Ordering Information

ACCURACY	ORDERING INFORMATION* TEMPERATURE RANGE			
	0°C TO +70°C		−55°C to +125°C	
0.05%	DAC1020LCD	AD7520LD	DAC1020LD	AD7520UD
0.10%	DAC1021LCD	AD7520KD	DAC1021LD	AD7520TD
0.20%	DAC1022LCD	AD7520JD	DAC1022LD	AD7520SD

*See NS Package D16C

ACCURACY	ORDERING INFORMATION* TEMPERATURE RANGE			
	0°C TO +70°C		−55°C TO + 125°C	
0.05%	DAC1220LCD	AD7521LD	DAC1220LD	AD7521UD
0.10%	DAC1221LCD	AD7521KD	DAC1221LD	AD7521TD
0.20%	DAC1222LCD	AD7521JD	DAC1222LD	AD7521SD

*See NS Package D18A

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DAC1020LD, DAC1021LD, DAC1022LD, DAC1220LD, DAC1221LD, DAC1222LD	−55°C	+125	°C
DAC1020LCD, DAC1021LCD, DAC1022LCD, DAC1220LCD, DAC1221LCD, DAC1222LCD	0	+70	°C

Electrical Characteristics

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 2)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FS
9-Bit Parts	DAC1021, DAC1221			0.10			0.10	% FS
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FS
Linearity Error Tempco	$-10V \leq V_{REF} \leq +10V$, (Note 1)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \leq V_{REF} \leq +10V$, (Notes 1 and 2)		0.3			0.3		% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
$I_{OUT\ 1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\ 2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \leq V^+ \leq 16V$, (Note 2), *(Figures 1 and 2)*		0.005			0.005		% FS/V
V_{REF} Input Resistance		5	10	20	5	10	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
Output Capacitance								
$I_{OUT\ 1}$	All Digital Inputs Low		37			37		pF
	All Digital Inputs High		120			120		pF
$I_{OUT\ 2}$	All Digital Inputs Low		120			120		pF
	All Digital Inputs High		37			37		pF
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V

Electrical Characteristics (Continued)

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	DAC1020, DAC1021 DAC1022			DAC1220, DAC1221 DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
	Digital Input High		1	100		1	100	µA
	Digital Input Low		−50	−200		−50	−200	µA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent but otherwise more useful specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. For every millivolt offset between I_{OUT1} or I_{OUT2}, 0.005% linearity error will be introduced.

Typical Performance Characteristics

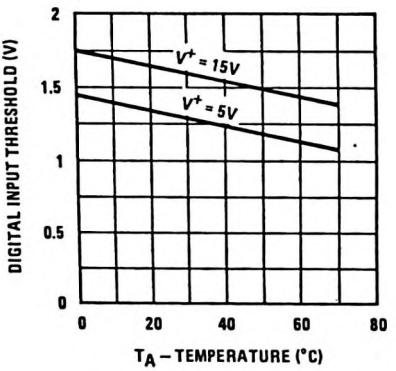


FIGURE 1. Digital Input Threshold vs Ambient Temperature

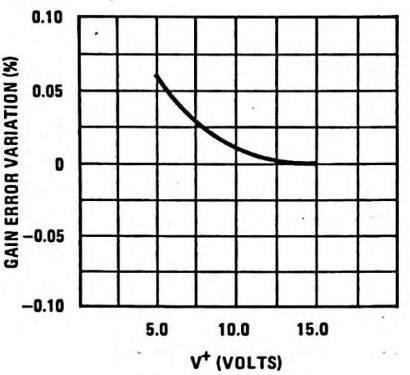


FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current *(Figure 3)*

The op amp bias current, I_b, flows through the 10k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 10k x I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications. The I_b of the LM741 type bipolar op amps is of the order of 200 μA and if a $V_{REF} \leq 10V$ is used, bias current cancellation schemes are recommended.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~10k if more than 4 digital inputs are high; R_{OUT} is ~30k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust *(Figure 3)*

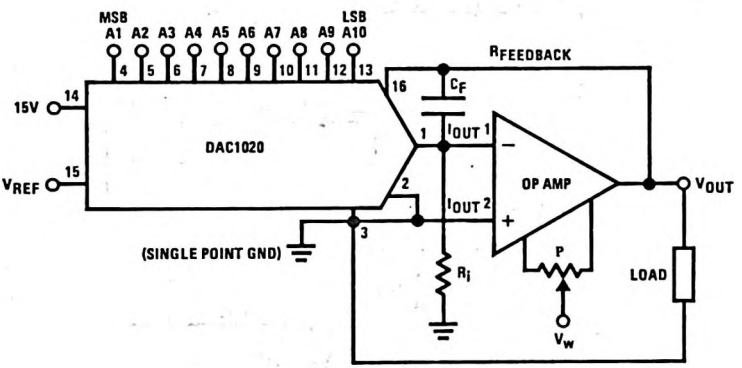
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ±1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust *(Figure 4)*

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $||V_{OUT}||$ to a voltage equal to V_{REF} x 1023/1024.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

OP AMP FAMILY	C_F	R_i	P	V_w	CIRCUIT SETTLING TIME, t_s	CIRCUIT SMALL SIGNAL BW
LM357	10 pF	2.4k	25k	V^+	1.5 μs	1M
LM356	22 pF	∞	25k	V^+	3 μs	0.5M
LF351	24 pF	∞	10k	V^-	4 μs	0.5M
LM741	0	∞	10k	V^-	40 μs	200 kHz



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

where $A_N = 1$ if the A_N digital input is high
$A_N = 0$ if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

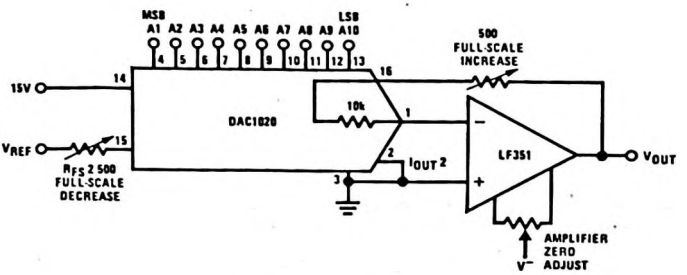


FIGURE 4: Full-Scale Adjust

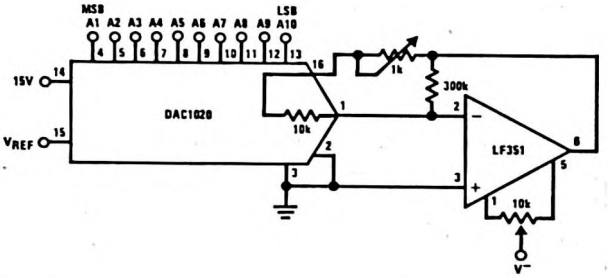
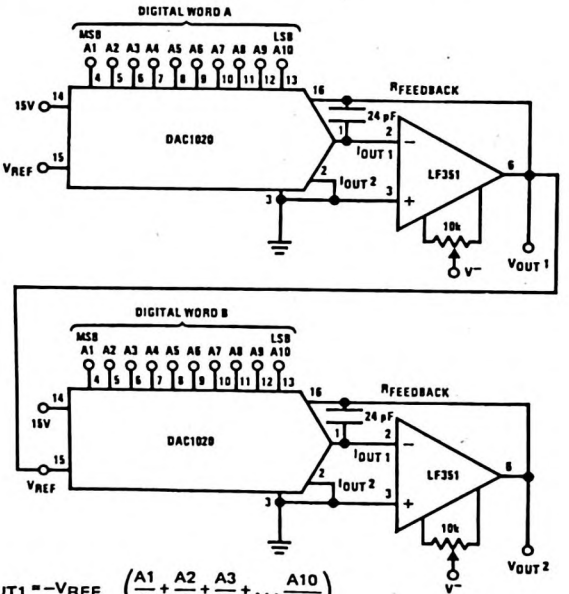


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



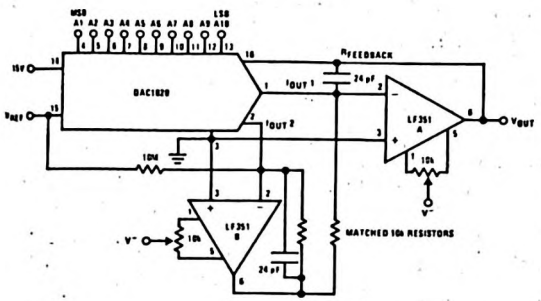
$$V_{OUT1} = -V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\ldots\frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\ldots\frac{A10}{1024}\right) \times \left(\frac{B1}{2}+\frac{B2}{4}+\frac{B3}{8}+\ldots\frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

Typical Applications (Continued)



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high
AN = −1 if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT										V_{OUT}
0	0	0	0	0	0	0	0	0	0	$+V_{REF}$
0	0	0	0	0	0	0	0	0	1	$V_{REF} \times 1022/1024$
0	1	1	1	1	1	1	1	1	1	$V_{REF} \times 2/1024$
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	$-V_{REF} \times 2/1024$
1	1	1	1	1	1	1	1	1	1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

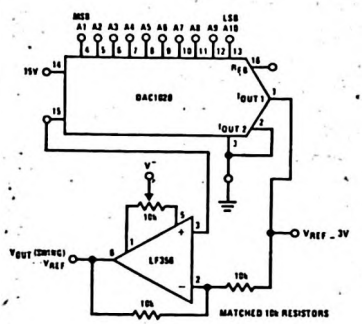
Operational Amplifiers V_{OS} Adjust *(Figure 7)*

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.

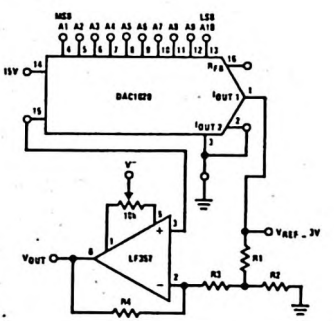


TRUE OFFSET BINARY OPERATION

DIGITAL INPUT										V_{OUT}
1	1	1	1	1	1	1	1	1	1	$V_{REF} \times 1022/1024$
1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	$-V_{REF}$

t_s = 1.8 μs
Use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp



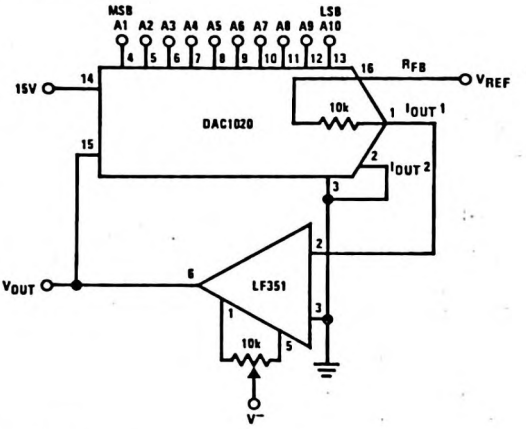
- $R4 = (2A_V^- - 1)R$, $\frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1}$,

  $R3 + R1 \| R2 = R$; $A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}}$, R = 20k

- Example: $V_{REF} = 2V$, V_{OUT} (swing) ≃ ±10V: $A_V^- = 5V$
  Then R4 = 9R, R1 = 0.8 R2. If R1 = 0.2R then R2 = 0.25R, R3 = 0.64R

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

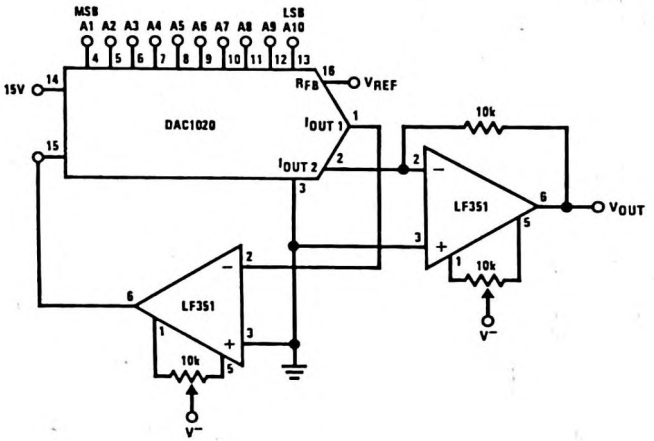


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)

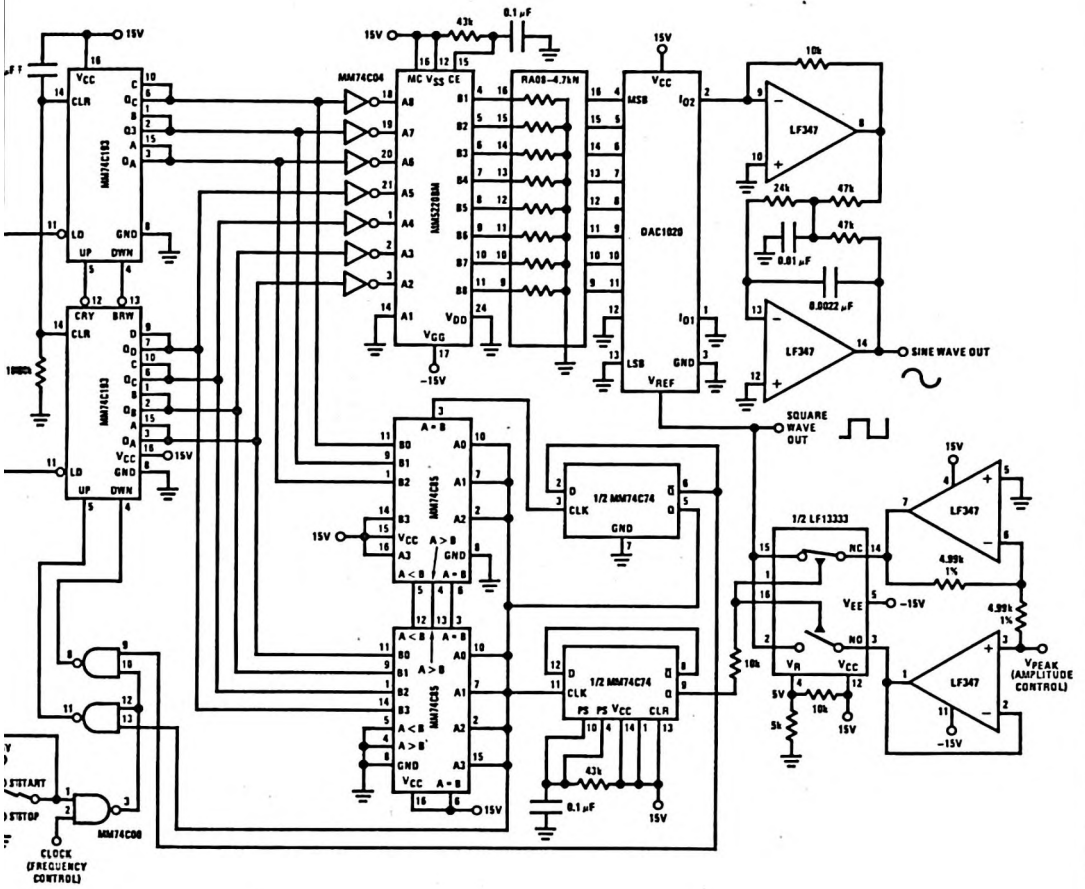


$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \cdots + \frac{\overline{A10}}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \cdots + \frac{A10}{1024}}\right] \quad \text{or} \quad V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \leq N \leq 1023$
$N = 0$ for A_N = all zeros
$N = 1$ for A10 = 1, A1—A9 = 0
.
.
.
$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally Controlled Amplifier-Attenuator

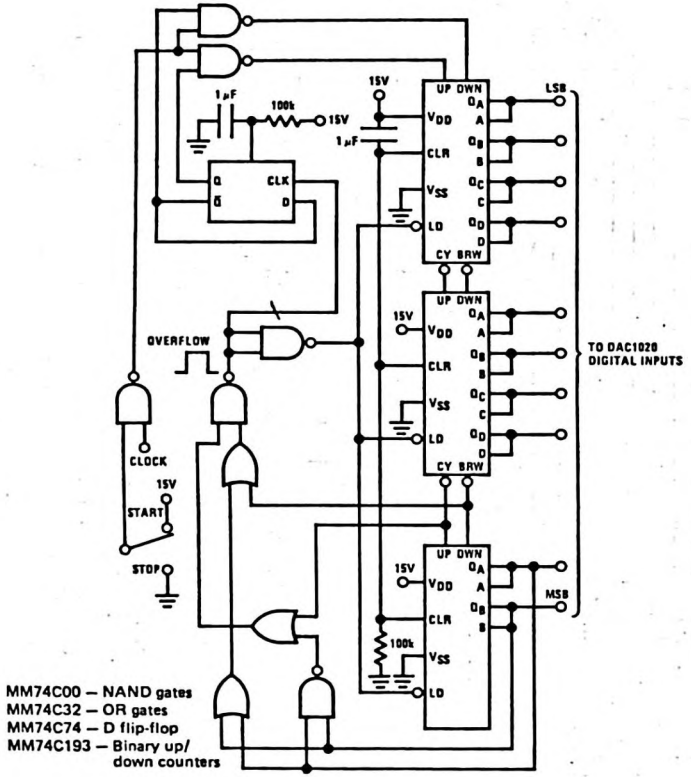
Typical Applications (Continued)



- Output frequency = $\frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V–10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition Of Terms

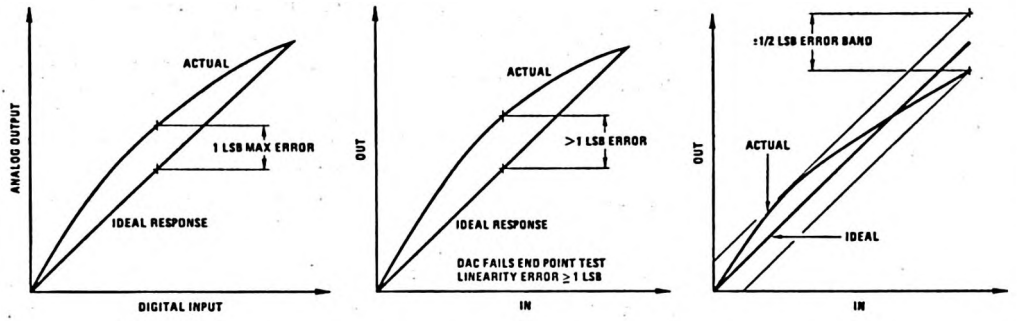
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within ±1/2 LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is V_{REF} − 1 LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10.0000V − 9.8 mV = 9.9902V. Full-scale error is adjustable to zero as shown in *Figure 5*.



(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the ±1/2 LSB linearity error specification

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the ±1/2 LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

National Semiconductor

DAC1200/DAC1201
12-Bit (Binary) Digital-to-Analog Converters
DAC1202/DAC1203
3-Digit (BCD) Digital-to-Analog Converters

General Description

The DAC1200 series of D/A converters is a family of precision low-cost converter building blocks intended to fulfill a wide range of industrial and military D/A applications. These devices are complete functional blocks requiring only application of power for operation. The design combines a precision 12-bit weighted current source (12 current switches and 12-bit thin-film resistor network), a rapid-settling operational amplifier, and 10.24V (for binary series) or 10.00V (for BCD series) buffered reference.

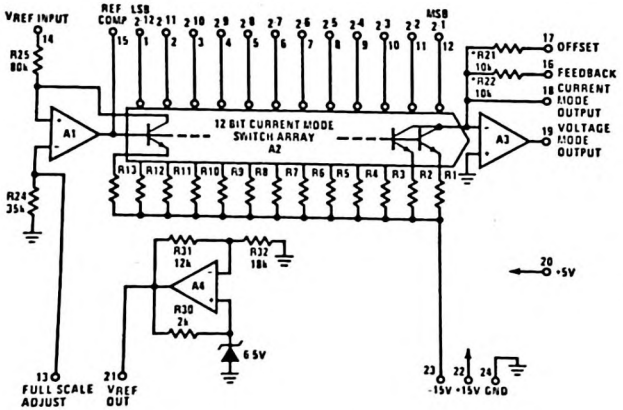
Input coding options include complementary binary and complementary BCD formats. In all instances, a logic "low" ($\leq$ 0.8V) turns a given bit ON, and a logic "high" ($\geq$ 2.0V) turns the bit OFF. Output format may be programmed for bipolar (±10V) or unipolar (0 to 10V) operation using internally supplied thin-film resistor pin strap options. Current mode operation is also available from 0 to 2 mA (for binary) or 0 to 1.25 mA (for BCD).

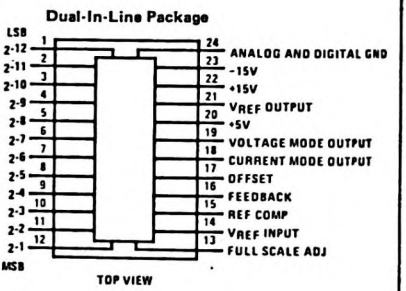
The entire series is available in hermetically sealed 24-lead DIP.

Features

- Circuit completely self-contained
- Both current and voltage-mode outputs
- Standard power supplies: ±15V and +5V
- Internal buffered reference: 10.24V for binary
  10.00V for BCD
- 0 to 2 mA, ±10V or 0 to 10V output by strapping internal resistors; other scales by external resistors
- ±1/2 LSB (binary) or ±1/10 LSD (BCD) linearity
- Fast settling time: 1.5 μs in current mode
  2.5 μs in voltage mode
- High slew rate: 15 V/μs
- TTL and CMOS compatible complementary binary or BCD input logic format
- 12 bit linearity
- Standard dual-width DIP package

Block and Connection Diagrams





*R21 = R22 = 16k for DAC1202/1203 (BCD)

Absolute Maximum Ratings

Supply Voltage (V^+ & V^-)	±18V
Logic Supply Voltage (V_{CC})	+10V
Logic Input Voltage	−0.7V to +18V
Reference Input Voltage	−0V, +18V
Power Dissipation	(see graphs)
Short Circuit Duration (pins 18, 19 & 21)	Continuous
Operating Temperature Range	
DAC1200HD, DAC1201HD, DAC1202HD, DAC1203HD	−55°C to +125°C
DAC1200HCD, DAC1201HCD, DAC1202HCD, DAC1203HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC Electrical Characteristics DAC1200/1201 Binary D/A (Notes 1, 2)

PARAMETER	CONDITIONS	DAC1200/1200C			DAC1201/1201C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error (Note 3)	$T_A = 25°C$			±0.0122			±0.0488	% FS
				±0.0244			±0.0976	% FS
Offset Voltage	$T_A = 25°C$		1	5		1	10	mV
				10			15	mV
Voltage Mode Full-Scale Error (Note 3)	$V_{REF} = 10.240V$		0.01	0.1		0.02	0.2	% FS
Voltage Mode Full-Scale Error	Pin 21 connected to Pin 14, $T_A = 25°C$		0.1	0.6		0.1	0.7	% FS
Monotonicity (Notes 3, 4)		Guaranteed over the temperature range						
Voltage Mode Power Supply Sensitivity	$\Delta V^+ = \pm 2V$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V^- = \pm 2V$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V_{CC} = \pm 1V$		0.002	0.02		0.002	0.02	% FS/V
	$T_A = 25°C$, $V_{REF} = 10.240V$							
Output Voltage Range	$R_L = 5k$	±10.5	±12		±10.5	±12		V
Voltage Mode Output Short Circuit Current Limit	$T_A = 25°C$		20	50		20	50	mA
Current Mode Voltage Compliance	(Note 6)	±2.5			±2.5			V
Current Mode Output Impedance			15			15		kΩ
Reference Voltage	$0mA \leq I_{REF} \leq 2mA$, $T_A = 25°C$	10.190	10.240	10.290	10.190	10.240	10.290	V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current (Bit OFF)	$V_{IN} = 2.5V$		1	10		1	10	μA
Logic "0" Input Current (Bit ON)	$V_{IN} = 0V$		-10	-100		-10	-100	μA
Power Supply Current I^+	$V^+ = 15.0V$		10	15		10	15	mA
Power Supply Current I^-	$V^- = -15.0V$, $T_A = 25°C$		25	30		25	30	mA
Power Supply Current I_{CC}	$V_{CC} = 5.0V$		20	25		20	25	mA

DC Electrical Characteristics DAC1202/1203 3-Digit BCD D/A (Notes 1, 2)

PARAMETER	CONDITIONS	DAC1202/1202C			DAC1203/1203C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		3			3			Digits
Linearity Error (Note 5)	$T_A = 25°C$			0.01			0.05	% FS
				0.02			0.1	% FS
Offset Voltage	$T_A = 25°C$		1	5		1	10	mV
				10			15	mV
Voltage Mode Full-Scale Error (Note 5)	$V_{REF} = 10.000V$		0.01	0.1		0.02	0.2	% FS
Voltage Mode Full-Scale Error	Pin 21 connected to Pin 14, $T_A = 25°C$		0.5	0.6			0.7	% FS
Monotonicity (Notes 4, 5)		Guaranteed over the temperature range						
Voltage Mode Power Supply Sensitivity	$\Delta V^+ = \pm 2V$ $T_A = 25°C$		0.002	0.02		0.002	0.02	% FS/%
	$\Delta V^- = \pm 2V$ $V_{REF} = 10.000V$		0.002	0.02		0.002	0.02	% FS/%
	$\Delta V_{CC} = \pm 1V$		0.002	0.02		0.002	0.02	% FS/%
Voltage Mode Output Voltage Range	$R_L = 5k$	±10.5	±12		±10.5	±12		V
Voltage Mode Output Short Circuit Limit	$T_A = 25°C$		20	50		20	50	mA
Current Mode Compliance	(Note 6)	±2.5			±2.5			V
Current Mode Output Impedance			10			10		kΩ
Reference Voltage	$0 \leq I_{REF} \leq 2mA$, $T_A = 25°C$	9.950	10.000	10.050	9.950	10.000	10.050	V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current (Bit OFF)	$V_{IN} = 2.5V$		1	10		1	10	μA
Logic "0" Input Current (Bit ON)	$V_{IN} = 0V$		−10	−100		−10	−100	μA
Power Supply Current I^+	$V^+ = 15.0V$		10	15		10	15	mA
Power Supply Current I^-	$V^- = -15.0V$ $T_A = 25°C$		25	30		25	30	mA
Power Supply Current I_{CC}	$V_{CC} = 5.0V$		20	25		20	25	mA

AC Electrical Characteristics DAC1200/1201/1202/1203

PARAMETER	CONDITIONS ($T_A = 25°C$)	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time (Note 6)	DAC1200/1202, $V_\epsilon \leq 1.25$ mV		1.5	3.0	μs
	DAC1201/1203, $V_\epsilon \leq 5.0$ mV		1	3.0	μs
Voltage Mode Full-Scale Change Settling Time (Note 6)	DAC1200/1202, $V_\epsilon \leq 1.25$ mV		2.5	5.0	μs
	DAC1201/1203, $V_\epsilon \leq 5.0$ mV		2.0	5.0	μs
Current Mode Full-Scale Settling Time	$R_L = 1k\Omega$, $C_L \leq 20pF$ $0 \leq \Delta I_{OUT} \leq 2mA$		1.5		μs
Voltage Mode Slew Rate	$-10V \leq \Delta V_{OUT} \leq +10V$		15		V/μs

Note 1: Unless otherwise noted, these specifications apply for $V^+ = 15.0V$, $V^- = -15.0V$, and $V_{CC} = 5.0V$ over the temperature range −55°C to +125°C for the DAC1200HD/1201/1202/1203 and −25°C to +85°C for the DAC1200HCD/1201/1202/1203.

Note 2: All typical values are for $T_A = 25°C$.

Note 3: Unless otherwise noted, this specification applies for $V_{REF} = 10.24V$, and over the temperature range −25°C to +85°C. Test conditions include adjustment of offset to 0V and full-scale to 10.2375V.

Note 4: The DAC1200, DAC1202 and DAC1203 are tested for monotonicity by stimulating all bits; the DAC1201 is tested for monotonicity by stimulating only the 10 MSBs and holding the 2 LSBs at 2.0V (i.e., 2 LSBs are OFF).

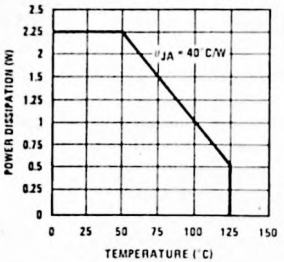
Note 5: Unless otherwise noted, this specification applies for $V_{REF} = 10.000V$, and over the temperature range −25°C to +85°C. Test conditions include adjustment of offset to 0V and full-scale to 9.990V.

Note 6: Not tested — guaranteed by design.

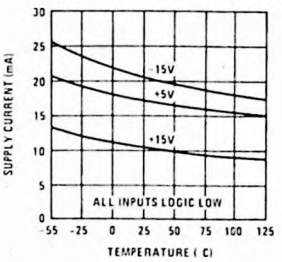
Note 7: ($\Delta V_{OUT} = 10V$)

Typical Performance Characteristics

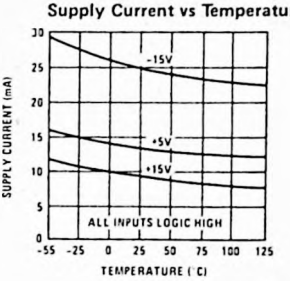
Maximum Power Dissipation

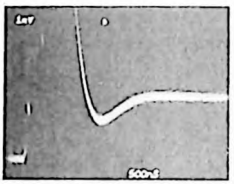


Supply Current vs Temperature

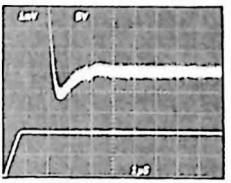


Supply Current vs Temperature

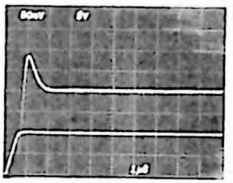




1 LSB Transition
1011 . . . 1 → 1100 . . . 0
V_O = 0, 10V
C_F = 30pF
T_A = 25°C



10V Full Scale Settling Time



10V Full Scale Pulse Response

Applications Information

1. Introduction

The DAC1200 series D/A converters are designed to minimize adjustments and user-supplied external components. For example, included in the package are a buffered reference, offset nulled output amplifier, and application resistors as well as the basic 12-bit current mode D/A.

However, the DAC1200 series is a sophisticated building block. **Its principles of operation and the following applications information should be read before applying power to the device.**

The user is referred to National Semiconductor Application Notes AN-156 and AN-157 for additional information.

2. Power Supply Selection & Decoupling

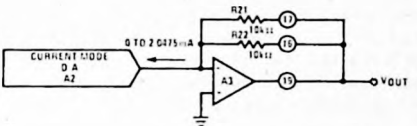
Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ± 0.1%) with less than 0.5mVrms of output noise and hum.

To realize the full speed capability of the device, all three power supply leads should be bypassed with 1μF tantalum electrolytic capacitors in shunt with 0.01μF ceramic disc capacitors no farther than ½ inch from the device package.

3. Unipolar and Bipolar Operation

The DAC1200 series D/A's may be configured for either unipolar or bipolar operation using resistors provided with the device. Figures 1A and 1B illustrate the proper connection for binary and BCD unipolar operation.

Bipolar operation is accomplished by offsetting the output amplifier A3 as shown in figures 2A and 2B.



*V_{OUT} = (I_{ZERO} to $I_{FULLSCALE}$)$\left(\frac{R21 \cdot R22}{R21 + R22}\right)$

= (0mA to 2.0475mA)(5kΩ)

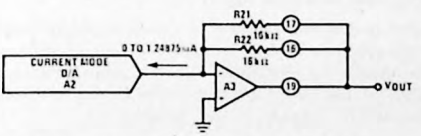
= 0V to +10.2375V

*Values shown are for V_{REF} = 10.240V.

1 LSB Voltage Step = $\frac{10.240V}{4096}$ = 2.5mV.

1 LSB Current Step = $\frac{2.5mV}{5.0k\Omega}$ = 0.5μA

FIGURE 1A. DAC1200/DAC1201 Unipolar Operation



*V_{OUT} = (I_{ZERO} to $I_{FULLSCALE}$)$\left(\frac{R21 \cdot R22}{R21 + R22}\right)$

= (0 to 1.24875mA)(8kΩ)

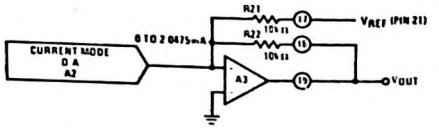
= 0V to 9.990V

*Values shown are for V_{REF} = 10.000V.

1 LSD Voltage Step = $\frac{10.000}{1000}$ = 10mV

1 LSD Current Step = $\frac{10mV}{8k\Omega}$ = 1.25μA

FIGURE 1B. DAC1202/DAC1203 Unipolar Operation



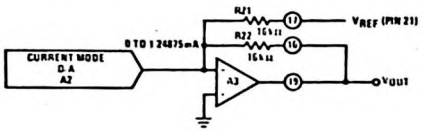
$$^{*}V_{OUT} = (0 \text{ to } 2.0475mA)R22 - \frac{V_{REF}}{R22} R21$$

$$= (0 \text{ to } 2.0475mA)R22 - V_{REF},\ R21 \equiv R22$$

$$= -10.240 \text{ to } +10.235V$$

*Values shown are for $V_{REF} = 10.240V$
1 LSB = 5mV.

FIGURE 2A. DAC1200/DAC1201 Bipolar Operation



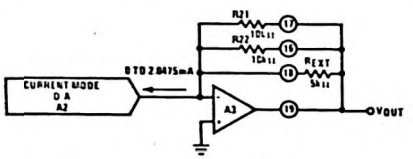
$$^{*}V_{OUT} = (0mA \text{ to } 1.24875mA)(R22) - \frac{R22}{R21} V_{REF}$$

$$= -10.000V \text{ to } +9.80V$$

*Values shown are for $V_{REF} = 10.000V$.
1 LSD Voltage Step = 20mV.

FIGURE 2B. DAC1202/DAC1203 Bipolar Operation

External resistors may be used to achieve alternate zero and full-scale voltages. It is advantageous to utilize R21 and R22 even in these applications since they are closely matched in TCR and temperature to the internal array. Figure 3 illustrates the recommended circuit for zero to 5V operation. R_{EXT} should be of metal film or wire-wound construction with a TCR of less than 10ppm/°C.



$$R_{TOTAL} = (R21) \| (R22) \| (R_{EXT}) = \frac{V_{FULLSCALE}}{2.0475mA} = 2.5k\Omega.$$

FIGURE 3. DAC1200 0 to 5.120V Operation

4. Offset and Full-Scale Adjust

If higher precision is required in the zero and full-scale, external adjustments may be made. The circuit of figure 4 illustrates the recommended circuit to adjust offset and full-scale of the DAC1200 series. The circuit will work equally well for unipolar or bipolar operation.

In bipolar operation, the offset is adjusted at minus full-scale; in the unipolar case at zero scale.

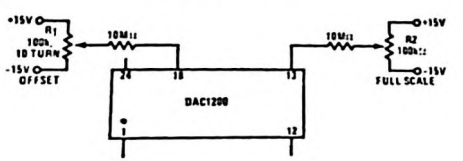


FIGURE 4. Offset & Full-Scale Adjust

For the values shown in figure 4, R1 will allow a ±7mV offset adjustment for the unipolar case and ±15mV for the bipolar case. R2 will allow a ±50mV adjustment of full scale.

5. Current Mode Operation

Access to the summing junction of A3 affords current mode operation either with a resistive load or to drive a fast-settling external operational amplifier. The loop around A3 should not be closed in current mode operation. There is a ±2.5V maximum compliance voltage at A2's output (pin 18) which restricts the maximum size of the load resistor; i.e., $R_L \times I_{FULLSCALE} \leq 2.5V$.

Note: $I_{FULLSCALE} \approx 2$ mA for DAC1200/DAC1201 and ≈ 1.25 mA for DAC1202/DAC1203.

6. Settling Time & Glitch Minimization

The settling time of the DAC1200 series and the glitch which occurs between major input code changes may be improved by placing a 10 to 30pF capacitor between pins 18 (current-mode output) and 19 (voltage mode output). The capacitor is used to cancel output capacitance of the current mode D/A and stray capacitance at pin 18.

7. Current Output Boosting

The DAC1200 series may be operated as a "power D/A" by including a current buffer such as the LH0002 or LH0063 in the loop with A3 as shown in figure 5.

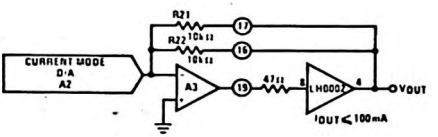


FIGURE 5. Current Boosted Output

8. Logic Input Coding

The sense of the logic inputs to the DAC1200 series is complementary; i.e., a given bit is turned ON by an active "low" input. Table I summarizes input status for the unipolar and bipolar complementary binary and BCD codes.

Other input codes may also be used. For example, the twos complement code, which is used extensively in computer and microprocessor applications, may be converted to the DAC1200 complementary bipolar format by inverting all bits except the MSB. The inversion may be accomplished in the microprocessor by software control, or by hardware using standard hex-inverters.

9. Reference Voltage

External reference voltages may be used with the DAC1200 series. Voltages other than 10.240 or 10.000V in the range of +5.0V to 11V will work satisfactorily for voltage mode operation. Full-scale voltage is always $V_{REF} - 1$ LSB where 1 LSB = $V_{REF}/4096$ (binary) or $V_{REF}/1000$ (BCD). Full-scale current (for binary) may be predicted by:

$$I_{FULLSCALE} = (V_{REF})(0.19995117)\text{mA}$$

CODE TYPE	(Note 8) INPUT CODE MSB LSB	OUTPUT STATE	OUTPUT VOLTAGE (Note 9)	OUTPUT CURRENT
Unipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.2375V	2.0475mA
	1111 1111 1110	1 LSB ON	+2.500mV	0.500μA
	1111 1111 1111	Zero Scale	Zero	Zero
Bipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.235V	+1.0235mA
	0111 1111 1111	Half Full-Scale	−0.000V	0.000mA
	1111 1111 1110	1 LSB ON	−10.235V	−1.0235mA
	1111 1111 1111	Zero Scale	−10.240V	−1.0240mA
Unipolar Complementary BCD	0110 0110 0110	Full-Scale	+9.990V	1.24875mA
	1111 1111 1110	1 LSB ON	10.000mV	1.250μA
	1111 1111 1111	Zero Scale	Zero	Zero
Bipolar Complementary BCD	0110 0110 0110	Full-Scale	9.980V	+0.62375mA
	1010 1111 1111	Half Full-Scale	0.000V	Zero
	1111 1111 1110	1 LSB ON	−9.980V	−0.62375mA
	1111 1111 1111	Zero Scale	−10.00V	−0.625mA

Note 8: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.
Note 9: V_{REF} = 10.240V for the DAC1200/1201 and 10.000V for the DAC1202/1203.

Definition of Terms

Resolution

Resolution is defined as the reciprocal of the number of discrete steps in the D/A output (as designed). It is directly related to the number of switches or bits within the D/A. For example, the DAC1200 has 2^{12} or 4096 steps. Resolution may therefore be expressed variously as 12 bits, as 1 part in 2^{12}, as 1 part in 4096, or as a percentage (1/4096 x 100 = 0.0244%). The DAC1202 has 1000 steps and 3 BCD digits. Resolution may be expressed as 0.1% or 3 BCD digits.

Linearity Error

Linearity error is the maximum deviation from a straight line passing through the endpoints of the D/A transfer characteristic. It is measured after calibrating for zero and full-scale. The linearity error of the DAC1200 series is guaranteed to be less than ±½ LSB or 0.0122% of F.S. for the DAC1200/1200C and ±0.0488% of F.S. for the DAC1201/DAC1201C. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Offset Voltage

Offset voltage is an output voltage other than zero volts for unipolar operation (and other than minus full-scale for bipolar operation) with all bits turned OFF. In the DAC1200 series this error resides primarily in the output amplifier, A3. Offset voltage is adjustable to zero as discussed in the applications section.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time

Two settling time parameters are specified for the DAC1200 series. Full-scale settling time requires a zero to full-scale or full-scale to zero output change. One LSB settling time requires one LSB output change. In both instances, settling time is the time required from a code transition until the D/A output reaches within ±½ LSB of final output value.

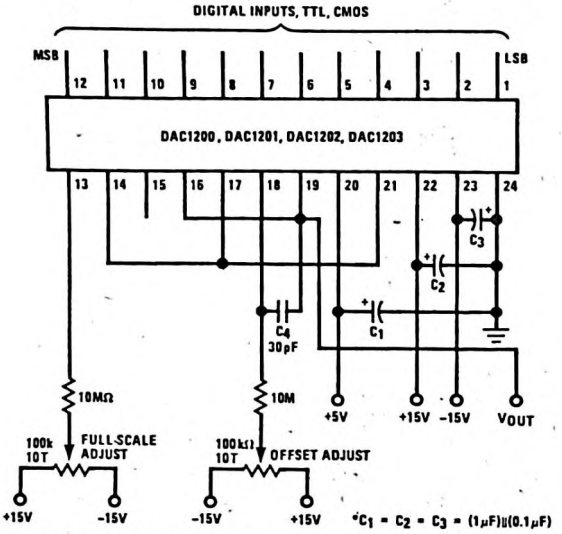
Monotonicity

Monotonicity is a characteristic of the D/A which requires a non-negative output step for an increasing input digital code. Monotonicity, therefore, demands no back steps or changes in sign of the slope of the D/A transfer characteristic.

Full-Scale Error

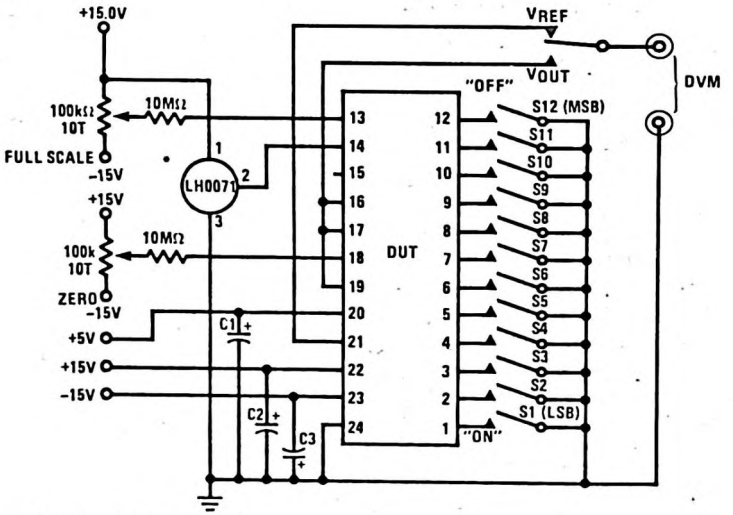
Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1200 full-scale is $V_{REF} - 1$ LSB. For V_{REF} = 10.240V and unipolar operation, $V_{FULLSCALE}$ = 10.240V − 2.5mV = 10.2375V. Departures from this value include internal gain, scaling, and reference errors. Full-scale error is adjustable to zero as discussed in the Applications section.

Typical Application



20 Volt Full-Scale Complementary D/A

DC Test Circuit



*LH0070 for DAC1202/1203

C1 = C2 = C3 = 4.7μF (solid tantalum) in parallel with a 0.01μF ceramic disc

Ordering Information

PART NUMBER		PACKAGE	25°C LINEARITY ERROR	OPERATING TEMPERATURE RANGE
BINARY	BCD			
DAC1200HD	DAC1202HD	Ceramic DIP	0.01%	−55°C to +125°C
DAC1201HD	DAC1203HD	Ceramic DIP	0.05%	−55°C to +125°C
DAC1200HCD	DAC1202HCD	Ceramic DIP	0.01%	−25°C to +85°C
DAC1201HCD	DAC1203HCD	Ceramic DIP	0.05%	−25°C to +85°C

*See NS Package HY24A

National Semiconductor

Digital-to-Analog Converters

DAC1280, DAC1285 12-Bit (Binary)
DAC1286, DAC1287 3-Digit (BCD)
Digital-to-Analog Converters

General Description

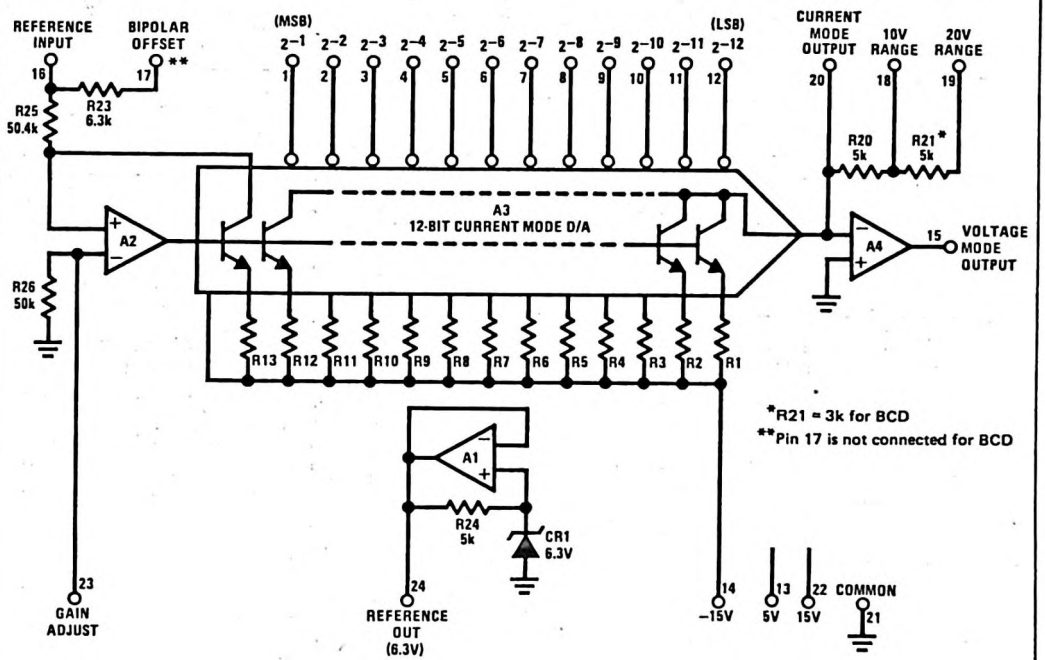
The DAC1280 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are available in complementary binary (CBI) and complementary BCD (CCD) coding formats. In all instances, a logic low ($\leq$ 0.8V) turns a given bit ON, and a logic high ($\geq$ 2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0 to 5V or 0 to 10V. Current mode output is also available 0 to 2 mA (binary models) and 1.25 mA (BCD models).

The entire series is available in a rugged side-brazed ceramic 24-lead DIP.

Features

- Completely self-contained with no external components required
- ±1/2 LSB linearity
- Standard power supplies: ±15V, 5V
- TTL, DTL, CMOS compatible binary or BCD
- ±2.5V, ±5V, ±10V, 0 to 5V, 0 to 10V voltage outputs
- 0 to 2 mA, 0 to 1.25 mA current output
- Internal reference
- Fast settling time: 300 ns current mode, 2.5 μs voltage mode
- Pin compatible with DAC80 and DAC85 series
- Full military temperature range operation

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V+ and V−)	±18V
Logic Supply Voltage (V_{CC})	10V
Logic Input Voltage	−0.7V, 18V
Reference Input Voltage (V_{REF})	0V, 18V
Power Dissipation	(See graph)
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous
Operating Temperature Range	
DAC1285HD, DAC1286HD	−55°C to +125°C
DAC1285HCD, DAC1286HCD, DAC1280HCD, DAC1287HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics DAC1285H, DAC1285HC, DAC1280HC Binary D/A (Notes 1 and 2)

PARAMETER	CONDITIONS	DAC1285HD			DAC1285HCD			DAC1280HCD			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			12			Bits
Linearity Error	T_A = 25°C			±1/2			±1/2			±1	LSB
	$T_{MIN} \le T_A \le T_{MAX}$, (Note 3)			±1/2			±1/2			±2	LSB
Differential Non-Linearity			±1/2			±1/2			±1/2		LSB
Zero-Scale Error (Offset)	(Notes 4 and 5)		±0.05			±0.05			±0.05		% FSR
Zero-Scale Drift (Offset Drift)	Unipolar, $T_{MIN} \le T_A \le T_{MAX}$		±1			±1			±1		ppm of FSR/°C
	Bipolar, $T_{MIN} \le T_A \le T_{MAX}$		±3	±10		±3	±15		±10		ppm of FSR/°C
Full-Scale Error (Gain Error)	(Note 5)		±0.1			±0.1			±0.1		% of FSR
Full-Scale Drift (Gain Drift)	$T_{MIN} \le T_A \le T_{MAX}$			±20			±30		±10		ppm/°C
Output Voltage Range	Using Internally Supplied Resistors	±2.5, ±5.0, ±10, 0 to +5, 0 to +10									V
Output Voltage Swing	$R_L \ge 5\ k\Omega$, Pin 15	±10	±12		±10	±12		±10	±12		V
Output Short-Circuit Current	Pin 15		±20			±20			±20		mA
Output Impedance	Pin 15, Closed Loop		0.05			0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20	0 to −2 mA									mA
	Bipolar, Pin 20	±1.0									
Current Mode Compliance		±2.5			±2.5			±2.5			V
Current Mode Output Impedance	Unipolar		15			15			15		kΩ
	Bipolar		4.4			4.4			4.4		kΩ
Reference Voltage	$-2\ mA \le I_{REF} \le 2\ mA$	6.0	6.3	6.6	6.0	6.3	6.6		6.3		V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8			0.8	V
Logic "1" Input Current	V_{IN} = 2.5V		1	10		1	10		1	10	μA
Logic "0" Input Current	V_{IN} = 0V		−10	−100		−10	−100		−10	−100	μA
Power Supply Current	I+		10			10			10		mA
	I−		25			25			25		mA
	I_{CC}		20			20			20		mA
Power Supply Sensitivity			0.002			0.002			0.002		% of FSR/%V

DC Electrical Characteristics DAC1286H, DAC1286HC, DAC1287HC BCD D/A (Notes 1 and 2)

PARAMETER	CONDITIONS	DAC1286HD			DAC1286HCD			DAC1287HCD			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		3			3			3			Digits
Linearity Error	$T_A = 25°C$			±1/2			±1/2			±1	LSB
	$T_{MIN} \leq T_A \leq T_{MAX}$, (Note 3)			±1/2			±1/2			±1	LSB
Differential Non-Linearity			±1/2			±1/2			±1/2		LSB
Zero-Scale Error (Offset Error)	(Notes 4 and 5)		±0.05			±0.05			±0.05		% FSR
Zero-Scale Drift (Offset Drift)	Unipolar, $T_{MIN} \leq T_A \leq T_{MAX}$		±1			±1			±1		ppm of FSR/°C
Full-Scale Error (Gain Error)	(Note 5)		±0.1			±0.1			±0.1		% of FSR
Full-Scale Drift (Gain Drift)	$T_{MIN} \leq T_A \leq T_{MAX}$			±20			±30		±10		ppm/°C
Output Voltage Range	Using Internally Supplied Resistors	0 to +10									V
Output Voltage Swing	$R_L \geq 5\ k\Omega$	±10	±12		±10	±12		±10	±12		V
Output Short-Circuit Current			±20			±20			±20		mA
Output Impedance	Pin 15, Closed Loop		0.05			0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20	0 to −1.25									mA
Current Mode Compliance		±2.5			±2.5			±2.5			V
Current Mode Output Impedance			15			15			15		kΩ
Reference Voltage	$-2\ mA \leq I_{REF} \leq 2\ mA$	6.0	6.3	6.6	6.0	6.3	6.6		6.3		V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		1	10		1	10		1	10	μA
Logic "0" Input Current	$V_{IN} = 0V$		−10	−100		−10	−100		−10	−100	μA
Power Supply Current	$I+$		10			10			10		mA
	$I-$		25			25			25		mA
	I_{CC}		20			20			20		mA
Power Supply Sensitivity			0.002			0.002			0.002		% of FSR/%V

Note 1: Unless otherwise specified, these specifications apply for $V^+ = 15V$, $V^- = -15V$ and $V_{CC} = 5V$ over the entire temperature range −55°C to +125°C for DAC1285HD and DAC1286HD, and −25°C to +85°C for DAC1285HCD, DAC1280HCD, DAC1286HCD and DAC1287HCD. For specified operation, the internal reference (pin 24) must be connected to the reference input (pin 16). The specifications are guaranteed after 360 seconds of warm-up after power turn-on.

Note 2: All typical values are for $T_A = 25°C$.

Note 3: These specifications apply to the limited temperature range $T_{MIN} = -25°C$ to $T_{MAX} = +85°C$ for DAC1285HD and DAC1286HD, and $T_{MIN} = 0°C$ to $T_{MAX} = +70°C$ for DAC1285HCD, DAC1280HCD, DAC1286HCD and DAC1287HCD. For the entire temperature range, double the above specifications.

Note 4: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V, etc.

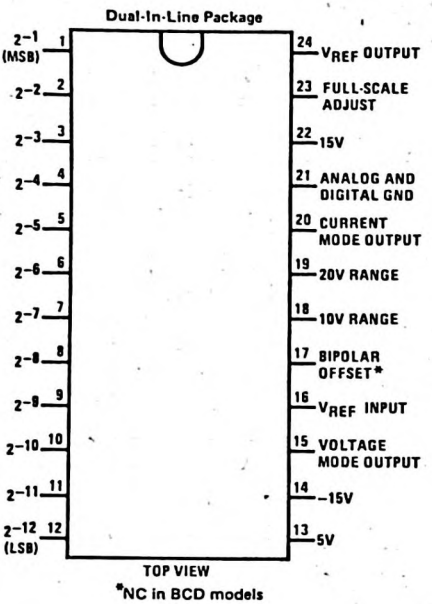
Note 5: Externally adjustable to zero.

AC Electrical Characteristics $T_A = 25°C$, (Note 6)

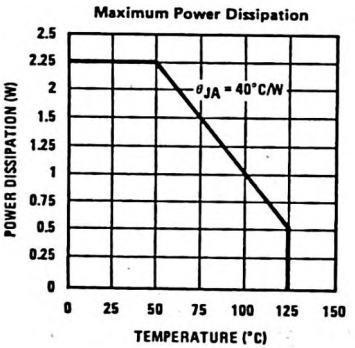
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time					
DAC1285, DAC1286	$V_E \leq 1\ mV$		1.5	3.0	μs
DAC1280C	$V_E \leq 5\ mV$		1.5	3.0	μs
Voltage Mode Full-Scale Settling Time	$V_E \leq 1\ mV$		2.5	5.0	μs
Current Mode Full-Scale Settling Time	$R_L = 100\Omega$		300		ns
Voltage Mode Slew Rate	$-10V \leq V_{OUT} \leq +10V$		20		V/μs

Note 6: Not tested, guaranteed by design.

Connection Diagram



Typical Performance Characteristics



Functional Description

The DAC1280 series is a sophisticated D/A building block. The user is encouraged to read the following applications information before applying power to the device. Refer to National Semiconductor Application Notes AN-156 and AN-159 for additional applications information.

Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ±0.1% with less than 0.5 mVrms of output noise and ripple.

To realize full speed capability of the device, all 3 power supply leads should be bypassed no further than 1/2 inch from the device, with 1 μF tantalum electrolytic capacitors in parallel with 0.01 μF ceramic disc capacitors.

VOLTAGE MODE OPERATION

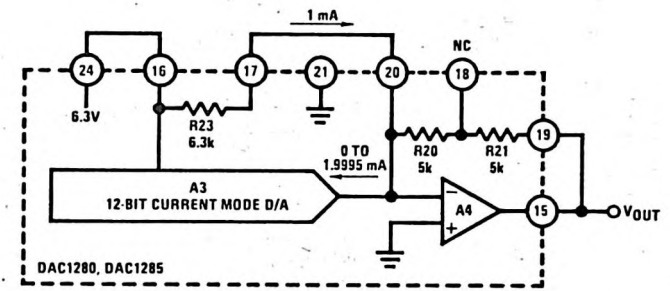
The DAC1280, DAC1285 binary and DAC1286, DAC1287 BCD D/A's provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ±2.5V, ±5V, ±10V and unipolar formats of 0 to 5V and 0 to 10V are possible using resistor strap options included within the device. Table I and *Figures 1–4* summarize the proper pin connections required for these formats.

Functional Description (Continued)

TABLE I. Output Voltage/Current Ranges for DAC1280 Series

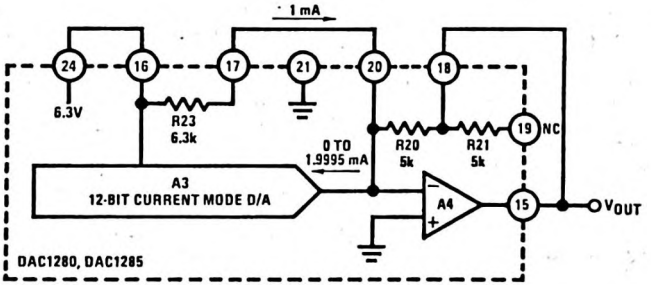
OUTPUT VOLTAGE RANGE	DIGITAL INPUT CODE	CONNECT PIN 15 TO	CONNECT PIN 16 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO
±10V	Complementary Offset Binary	19	24	20	15
±5V	Complementary Offset Binary	18	24	20	NC
±2.5V	Complementary Offset Binary	18	24	20	20
+10V	Complementary Binary	18	24	21*	NC
+5V	Complementary Binary	18	24	21*	20
±1 mA	Complementary Offset Binary	NC	24	20	NC
−2 mA	Complementary Binary	NC	24	21*	NC
+10V	Complementary BCD	19	24	NC	15
−1.25 mA	Complementary BCD	NC	24	NC	NC

*Optional, no connection necessary



V_{OUT} = (0 to 1.9995 mA) (R20 + R21) − (6.3V/R23)(R21 + R22)
= (0 to 1.9995 mA) (10k) − (1 mA) (10k)
= −10V to +9.995V
1 LSB = 20V/4096 = 4.88 mV

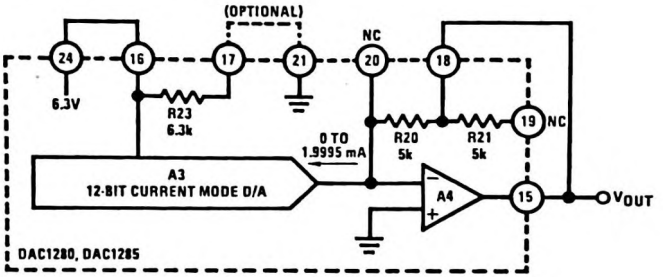
FIGURE 1. ±10V Bipolar Operation



V_{OUT} = (0 to 1.9995 mA) (R20) − (R20/R23)(6.3V)
= (0 to 1.9995 mA) (5k) − (5k/6.3k) (6.3V)
= −5V to 4.9975V
1 LSB = 10V/4096 = 2.44 mV

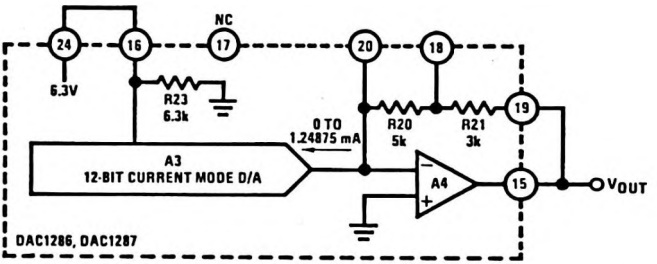
FIGURE 2. ±5V Bipolar Operation

Functional Description (Continued)



V_{OUT} = (0 to 1.9995 mA) (R20)
= (0 to 1.9995 mA) (5k)
= 0 to 9.9976V
1 LSB = 2.44 mV

FIGURE 3. 10V Unipolar Operation



V_{OUT} = (0 to 1.24875 mA) (R20 + R21)
= (0 to 1.24875 mA) (8k)
= 0 to 9.990V
1 LSB = 10 mV

FIGURE 4. 10V BCD Operation

CURRENT MODE OPERATION

Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1280 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 5* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load should also utilize the internally supplied resistors. A compliance restriction of ±2.5V at pin 20 is required for operation in the current output mode.

OFFSET AND FULL-SCALE ADJUST

The DAC1280 series may be offset and full-scale adjusted using the circuit shown in *Figure 6*. Offset voltage should be adjusted first. A logic "1" ($\geq$ 2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" ($\leq$ 0.8V) to all inputs for binary operation. For BCD, apply 011001100110 input coding. The range of R1 and R2 shown in *Figure 6* is approximately ±0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

LOGIC INPUT CODING

The logic inputs to the DAC1280 series are complementary; i.e., a given bit is turned ON by an active low input. Table II summarizes input status for unipolar and bipolar codes.

Functional Description (Continued)

REFERENCE SUPPLY

The DAC1280 series is supplied with an internal 6.3V reference supply voltage (pin 24). In order to obtain the specified performance, pin 24 should be connected to the Reference Voltage Input (pin 16). Since the reference is buffered by an op amp, the reference may be used externally at currents up to 5 mA. The reference output is short-circuit limited to a nominal 20 mA. An external reference voltage may be used with the DAC1280 series. Voltage values between 5V and 11V will work satisfactorily. Full-scale current may be predicted by:

$$I_{FULL\text{-}SCALE} = (V_{REF})\ (0.317381\ mA/V)$$

LOGIC INPUT COMPATIBILITY

The design of the current mode switches in the DAC1280 series give the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 18V, the DAC1280 series may be driven directly from high (or low) voltage CMOS.

TABLE II

CODE TYPE	INPUT CODE (Note 7) MSB											LSB	OUTPUT STATE	UNIPOLAR OUTPUT RANGES 0 to 10V	0 to 5V	0–2 mA 0–1.25 mA
Unipolar	0	0	0	0	0	0	0	0	0	0	0	0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1	1	1	1	1	1	1	1	1	1	1	0	1 LSB ON	0.0024V	0.0012V	0.0005 mA
Binary	1	1	1	1	1	1	1	1	1	1	1	1	Zero-Scale	0.0000V	0.0000V	0.0000 mA
Unipolar	0	1	1	0	0	1	1	0	0	1	1	0	Full-Scale	9.990V		1.2488 mA
Complementary	1	1	1	1	1	1	1	1	1	1	1	0	1 LSB ON	0.010V		0.00125 mA
BCD	1	1	1	1	1	1	1	1	1	1	1	1	Zero-Scale	0.000V		0.0000 mA

CODE TYPE	INPUT CODE (Note 7) MSB											LSB	OUTPUT STATE	BIPOLAR OUTPUT VOLTAGE RANGES ±10V	±5V	±2.5V	±1 mA
Bipolar	0	0	0	0	0	0	0	0	0	0	0	0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0	1	1	1	1	1	1	1	1	1	1	1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1	1	1	1	1	1	1	1	1	1	1	0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1	1	1	1	1	1	1	1	1	1	1	1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

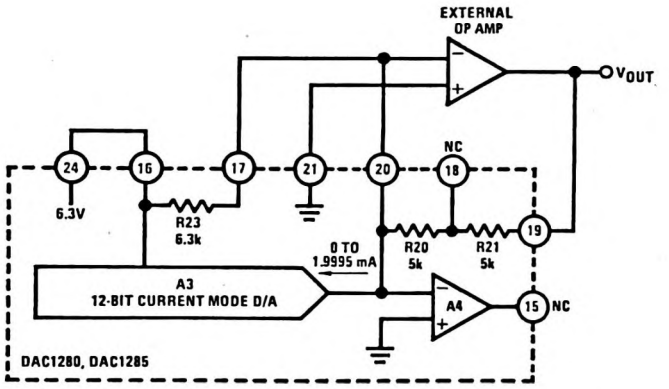


FIGURE 5. ±10V Bipolar Operation with External Operational Amplifier

Functional Description (Continued)

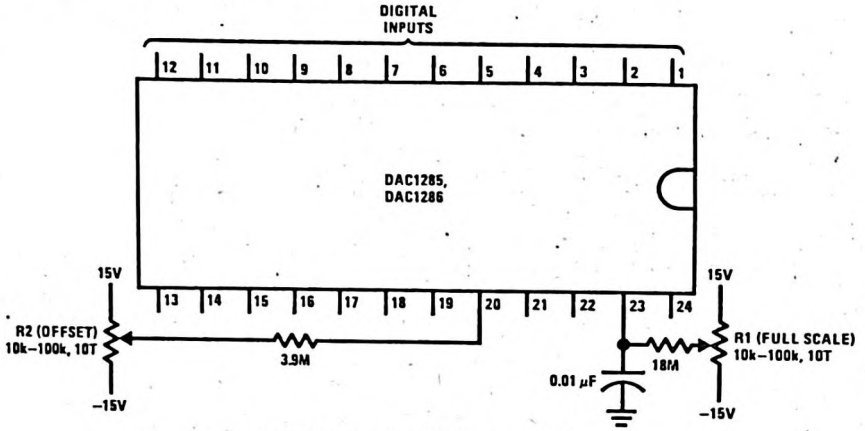


FIGURE 6. Full-Scale and Adjustment Circuits

Ordering Information

PART NUMBER		25°C LINEARITY	PACKAGE	TEMPERATURE RANGE
BINARY	BCD			
DAC1285HD	DAC1286HD	0.01%	DIP	−55°C to +125°C
DAC1285HCD	DAC1286HCD	0.01%	DIP	−25°C to +85°C
DAC1280HCD	DAC1287HCD	0.025%	DIP	−25°C to +85°C

*See NS Package HY24A

National Semiconductor

Digital-to-Analog Converters

LM1508/LM1408 8-Bit D/A Converter

general description

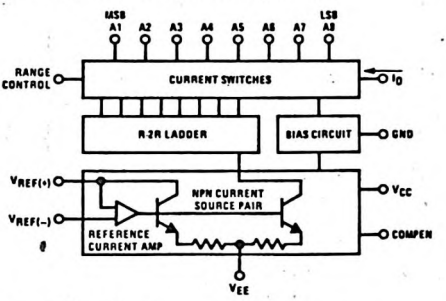
The LM1508/LM1408 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the LM1508/LM1408 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The LM1508/LM1408 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet. For more information, see DAC0808 data sheet.

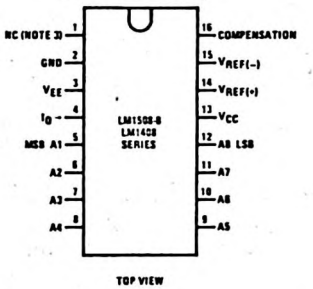
features

- Relative accuracy: ±0.19% error maximum LM1508-8 and LM1408-8
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

block and connection diagrams



Dual-In-Line Package



TOP VIEW

typical application

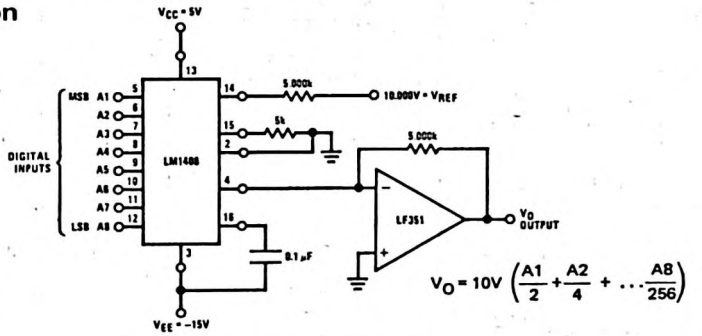


FIGURE 1. ±10V Output Digital to Analog Converter

ordering information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*		
		HERMETIC PACKAGE (D16C)	HERMETIC PACKAGE (J16A)	PLASTIC PACKAGE (N16A)
8-Bit	$-55°C \leq T_A \leq +125°C$	LM1508D-8	LM1508J-8	
8-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-8	LM1408N-8
7-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-7	LM1408N-7
6-Bit	$0°C \leq T_A \leq +75°C$		LM1408J-6	LM1408N-6

*Note. Devices may be ordered by using either order number.

absolute maximum ratings (T_A = 25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	5.5 V_{DC}
V_{EE}	−16.5 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
LM1508-8	−55°C ≤ T_A ≤ +125°C
LM1408-8 Series	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, LM1508-8: T_A = −55°C to +125°C; LM1408-8, LM1408-7, LM1408-6, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)					%
	LM1508-8				±0.19	%
	LM1408-8					
	LM1408-7, (Note 1)				±0.39	%
	LM1408-6, (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels					
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current					
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current			−1	−5	μA
	Output Current Range					
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	mA
	Output Current, All Bits Low			0	4	μA
	Output Voltage Compliance Pin 1 Grounded, V_{EE} Below −10V	E_r ≤ 0.19%, T_A = 25°C			−0.55, +0.4	V_{DC}
					−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate			8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)					
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Section 4

Data Acquisition Systems

4

National Semiconductor

Data Acquisition Systems

ADS1216HC 16-Channel, 12-Bit Data Acquisition System with Memory

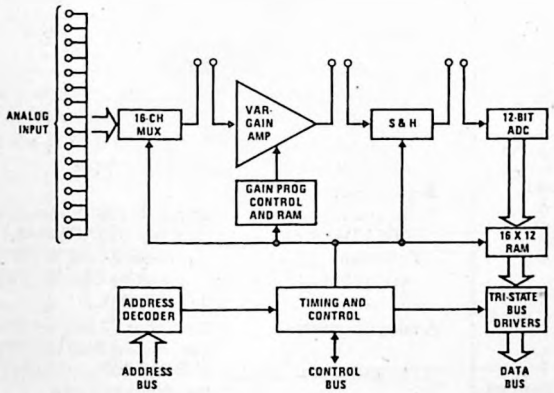
General Description

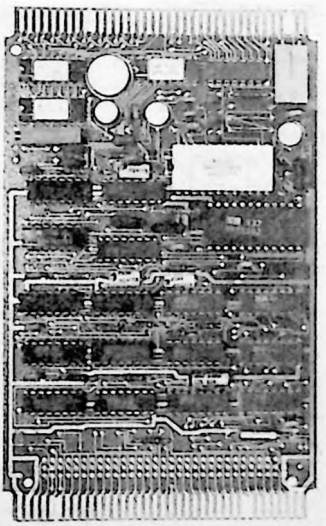
The ADS1216HC is a complete 16-channel (differential 8-channel) data acquisition system with 12-bit linearity and resolution. It features on-card memory and micro or mini-computer TTL bus driving capability. The system contains a 16-channel or differential 8-channel multiplexer; programmable gain amplifier with program memory loaded by software; sample-and-hold amplifier; 12-bit analog-to-digital converter, TRI-STATE® TTL bus drivers; and all timing, control, and interface circuits necessary for interfacing any micro or mini-computer. The system operates in a continuous, asynchronous, sequential scanning mode, updating the self-contained RAM upon completion of each data conversion. In this way, latest data for all channels is always resident in RAM. The system is memory-mapped so it appears to the computer exactly like main memory. The interface presents selected channel data to the data bus within 220 ns after data is requested, therefore data is accessible at main memory access speed. The system will operate with any of the popular computer systems by selection of appropriate off-card strap connections.

Features

- 16 single-ended, 16 quasi-differential, or 8 differential channels
- 12-bit resolution and linearity
- 220 ns data access time
- 16 channels of on-card memory
- Memory-mapped interface
- On-card precision gain-set network for gains of 1, 2, 2 1/2, 5, 10, 20, 50, 100
- Full-scale ranges 0–100 mV to ±10V including 1–5V
- Gain program memory provides any of 4 selected gains at any of 16 channels
- Internal precision reference divider for calibration at 0.1, 1, 5, 10V
- Internal 10.24V reference
- Drives fully loaded TTL data bus
- Continuous sequential channel scanning
- Supplied with mating card-edge connectors
- Operates with all TTL compatible 8-bit or 16-bit processors

Functional Block Diagram





Preliminary Specifications

ANALOG INPUTS

Data Channels	16 single-ended, 16 pseudo-differential, or 8 differential
Full Scale Range	±10.24V, 0–10.24V ±5.12V, 0–5.12V, 1–5.096V ±4.096V, 0–4.096V ±2.048V, 0–2.048V ±1.024V, 0–1.024V ±512 mV, 0–512 mV ±205 mV, 0–205 mV ±102 mV, 0–102 mV
Absolute Maximum, V_{IN}	±15V
Input Leakage Current	≤ 10 nA @ 25°C ≤ 60 nA –25°C to +85°C
Input Bias Current of S&H Amplifier	25 nA @ 25°C 75 nA –25°C to +85°C
Input Capacitance	≤ 100 pF for ON channel ≤ 10 pF for OFF channel
Input Channel MUX Switches ON for Power OFF	

SIGNAL DYNAMICS

Throughput Rate	8000 ch/sec (scans each of 16 channels every 2 ms)
S & H Feedthrough	≤ –80 dB @ 1 kHz
Crosstalk, OFF to ON Channel	≤ –80 dB @ 1 kHz
Differential Amp CMRR	≥ 60 dB @ f = 0–1 kHz, Gain = 1–100

ACCURACY

Resolution	12 bits
Quantizing Error	±1/2 LSB
Linearity Error	≤ ±1/2 LSB 25°C ≤ ±1 LSB –25°C to +85°C
Full Scale Error*	≤ ±1/2 LSB 25°C ≤ ±1 LSB –25°C to +85°C
Zero Scale Error*	≤ ±1/2 LSB 25°C ≤ ±1 LSB –25°C to +85°C
Power Supply Sensitivity*	≤ ±1/2 LSB, V_S = 14–16V, –25°C to +85°C
3 Sigma Noise Peak-Peak*	≤ ±1/2 LSB, 0–3 kHz
No Missing Codes*	
Amplifier Gain	1, 2, 2.5, 5 ±0.05%; 10, 20, 50 ±0.1%, 100 ±0.25%

REFERENCE

Voltage	10.240 ±0.015V @ 25°C 10.240 ±0.020V –25°C to +85°C
Reference Divider Ratio	10.24:10.00, 5.00, 1.00 ±0.05%; 0.100 ±0.1%

DATA OUTPUT

Standard TTL Levels TRI-STATE Bus Drivers 10 Standard TTL Loads	
Bus Structure	8-bit double byte right-justified or 16-bit single byte right or left-justified data.
Coding	Natural binary Offset binary 2's complement binary
Data Access Time	220 ns after address and read signals

ADDRESS INPUT

Standard TTL Levels	BA0, 2 low power TTL loads BA1–BA4, 1 low power TTL load BA5–BA16, high impedance with 0.65V hysteresis
Channel Select	4-bit channel select, 12-bit card select, or 4-bit channel select, 1-bit byte select, 11-bit card select

CONTROL BUS

Standard TTL Levels Logic "1" or Logic "0" True (Strap Select)	
Address Enable Strobe	3 standard TTL loads
Memory Select Strobe	1 low power Schottky TTL load
Memory Read Strobe	1 low power Schottky TTL load
Memory Write Strobe	1 low power Schottky TTL load
Memory Ready Signal	Will drive 10 standard TTL loads
NINIT	2 standard TTL loads

POWER REQUIREMENTS

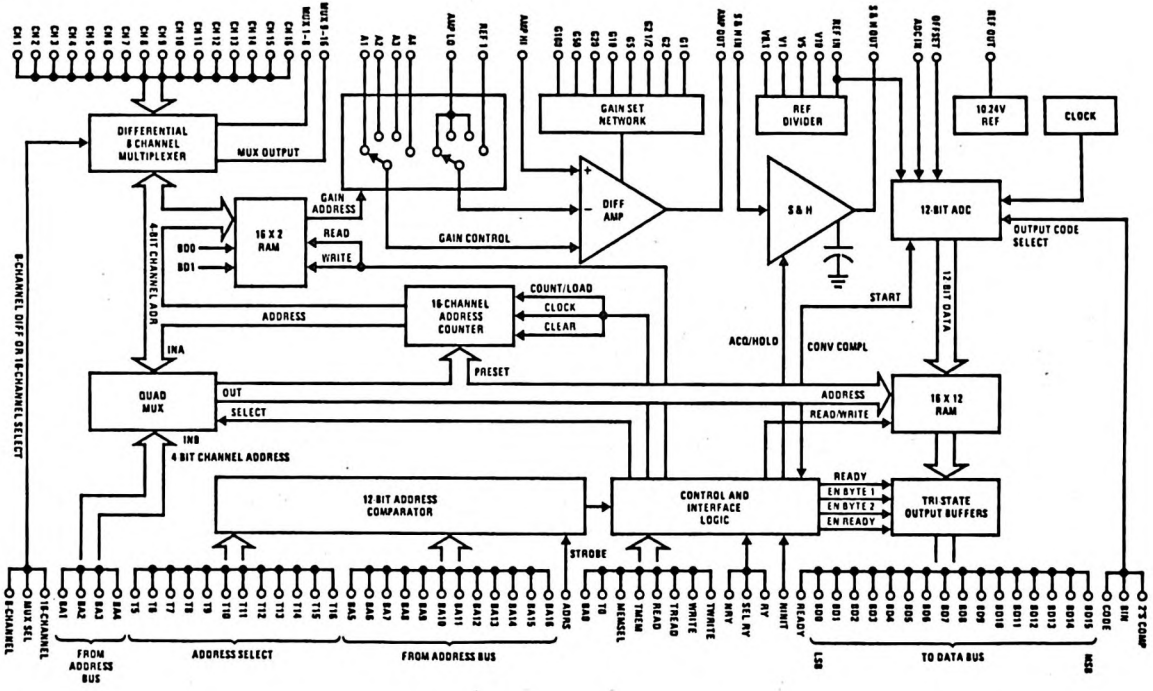
±15V	25 mA
5V	600 mA

PHYSICAL

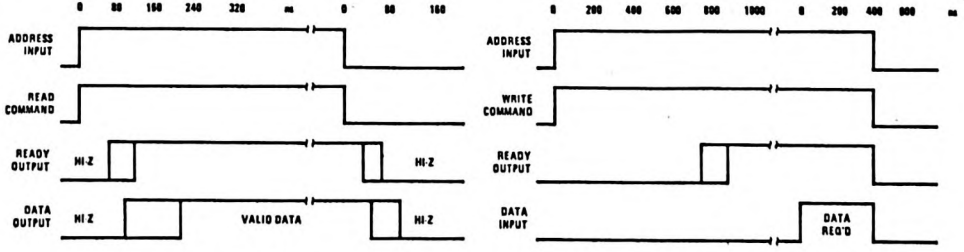
Dimensions	
Eurocard Version ADS1216HCE	100 mm W x 160 mm L x 11.2 mm loaded thickness
L Version ADS1216HCL	4.375" W x 6.70" L x 5/16" loaded thickness
Bus Connector	
Eurocard Version ADS1216HCE	96 pin, 0.100" ctrs mating Elco No. 8257-096-648-123
L Version ADS1216HCL	Card-edge 72 pin, 0.100" ctrs, mating Elco No. 6307-072-472-001
Analog Connector	Card-edge 72 pin, 0.100" ctrs, mating Elco No. 6042-072-000-002 or Continental No. 600-121-72XA

*Amplifier gain = 1

Block Diagram



Timing Diagrams



Read Cycle **Write Gain Program**

Important Note. Always load gain program after power-up and before beginning data acquisition operation.

Connection Tables

DIGITAL/BUS CONNECTIONS

Pin listing for Eurocard Version. Mating connector for Eurocard Version is Elco No. 8257-096-648-123.

POSITION	ROW A	ROW B	ROW C	POSITION	ROW A	ROW B	ROW C
1	5V	5V	5V	17	BA16	L0	T16
2	BIN	CODE	COMP	18	BA15	L0	T15
3	VL	VL	READY	19	BA14	L0	T14
4	BD8	VL	BD0	20	BA13	L0	T13
5	BD9	VL	BD1	21	BA12	L0	T12
6	BD10	VL	BD2	22	BA11	L0	T11
7	BD11	VL	BD3	23	BA2	L0	BA3
8	BD12	VL	BD4	24	BA1	L0	BA4
9	BD13	VL	BD5	25	BA10	L0	T10
10	BD14	VL	BD6	26	BA9	L0	T9
11	BD15	VL	BD7	27	BA8	L0	T8
12	READ	VL	TREAD	28	BA7	L0	T7
13	BA0	VL	T0	29	BA6	ADRS	T6
14	WRITE	VL	TWRITE	30	BA5	NINIT	T5
15	MEMSEL	D12	TMEM	31	MUX SEL	8-CH	16-CH
16	NRY	SEL RY	RY	32	GND	GND	GND

DIGITAL/BUS CONNECTIONS

Pin listing for L Version. Mating connector for L Version is Elco No. 6307-072-472-001.

POSITION		POSITION		POSITION		POSITION	
1	5V	19	BD13	37	BA16	55	BA9
2	5V	20	BD5	38	T16	56	T9
3	COMP	21	BD14	39	BA15	57	BA8
4	5V	22	BD6	40	T15	58	T8
5	BIN	23	BD15	41	BA14	59	BA7
6	CODE	24	BD7	42	T14	60	T7
7	VL	25	READ	43	BA13	61	BA6
8	READY	26	TREAD	44	T13	62	T6
9	BD8	27	BA0	45	BA12	63	BA5
10	BD0	28	T0	46	T12	64	T5
11	BD9	29	WRITE	47	BA11	65	ADRS
12	BD1	30	TWRITE	48	T11	66	INIT
13	BD10	31	MEMSEL	49	BA2	67	8-CH
14	BD2	32	TMEM	50	BA3	68	16-CH
15	BD11	33	SEL RY	51	BA1	69	MUX SEL
16	BD3	34	D12	52	BA4	70	GND
17	BD12	35	NRY	53	BA10	71	GND
18	BD4	36	RY	54	T10	72	GND

ANALOG CONNECTIONS

Mating connector for either format is the Elco No. 6042-072-000-002 or Continental 600-121-72XA.

POSITION		POSITION		POSITION		POSITION	
1	+15V	19	G5	37	MUX 9–16	55	CH 11
2	+15V	20	V10	38	AMP HI	56	COM 11
3	−15V	21	G2 1/2	39	ANA COM	57	COM 6
4	−15V	22	TP3	40	MUX 1–8	58	CH 6
5	PS COM	23	G2	41	COM 8	59	CH 14
6	PS COM	24	TP2	42	CH 8	60	COM 14
7	REF IN	25	G1	43	CH 16	61	COM 5
8	ADC IN	26	TP1	44	COM 16	62	CH 5
9	REF OUT	27	TP0	45	COM 4	63	CH 13
10	OFFSET	28	AMP OUT	46	CH 4	64	COM 13
11	G100	29	ANA GND	47	CH 12	65	COM 2
12	S&H OUT	30	S&H IN	48	COM 12	66	CH 2
13	G50	31	A3	49	COM 7	67	CH 10
14	V0. 1	32	A4	50	CH 7	68	COM 10
15	G20	33	A1	51	CH 15	69	COM 1
16	V1	34	A2	52	COM 15	70	CH 1
17	G10	35	AMP LO	53	COM 3	71	CH 9
18	V5	36	REF 1	54	CH 3	72	COM 9

Applications Information

ANALOG INPUTS

Sixteen pairs of input terminals are provided. Those marked CH 1 to CH 8 are multiplexed by an 8-channel multiplexer to MUX 1–8. Those marked CH 9 to CH 16 are multiplexed by another 8-channel multiplexer to MUX 9–16. Sixteen additional terminals, marked COM 1 to COM 16 are not multiplexed, but are connected to ANA COM. These are normally connected to the transducer or signal common lines except when multiplexing differential signals. The card connections are flexible enough to permit 16-channel single-ended, 16-channel quasi-differential or 8-channel differential connections.

8-Channel Differential Connection

Connect channel 1 signal high and low inputs to CH 1 and CH 9, respectively. Repeat with channels 2–8 high and low to CH 2–CH 8 and CH 10–CH 16, respectively. Connect MUX 1–8 to AMP HI and MUX 9–16 to AMP LO; also connect REF 1 to AMP LO as shown in *Figure 1*. The data out will represent the difference in signal levels as seen by MUX 1–8 and MUX 9–16; that is, V_O = CH 1–CH 9 and so forth to CH 8–CH 16. Input signals must be somewhere referenced to ANA GND to insure that the input signals are within the ±10V common-mode voltage range of the system. To set the multiplexer logic to the differential mode, it is necessary to strap MUX SEL to 8-CH.

16-Channel Single-Ended Connection

Connect channel 1 signal high through channel 16 signal high to CH 1–CH 16, respectively. Connect channel 1 signal low through channel 16 signal low to COM 1–COM 16 as in *Figure 2*. Interconnect ANA GND, ANA COM, AMP LO, and REF 1; interconnect MUX 1–8, MUX 9–16 and AMP HI. Also strap MUX SEL to 16-CH.

16-Channel Quasi-Differential Connection

Connect all 16 pairs of signal lines as for 16-channel single-ended connection. Strap ANA COM, AMP LO, and REF 4 as in *Figure 3*, interconnect MUX 1–8, MUX 9–16 and AMP HI. Do not connect signals to ANA GND, however, signals must somewhere be referenced to ANA GND. Also strap MUX SEL to 16-CH.

AMPLIFIER

Gain

The amplifier gain may be set to any of the following values on a per-channel basis; 1, 2, 2 1/2, 5, 10, 20, 50, 100. Up to 4 different gains may be selected for use with any of the 16 data channels. Gain is selected by strapping the gain select terminals A1–A4 to the gain set terminals G1–G100. For example, gain 4 is set to 100 in *Figure 4* by strapping A4 to G100, gain 2 is set to unity by strapping A2 to G1, gain 3 is set to 2 by strapping A3 to G2, and gain 1 is set to 2.5 by strapping A1 to G2 1/2. If all channels have a range of 0–10.2375V, the amplifier need not be used at all unless desired. In this case, strap AMP LO, AMP HI and REF 1 to ANA GND; and strap MUX 1–8, MUX 9–16, and S&H IN, thus bypassing the amplifier as in *Figure 5a*.

An alternate connection will provide more precise gain accuracy when a unity gain, single-ended amplifier is required. The connection shown in *Figure 5b* bypasses the programmable gain amplifier, but retains a precise, unity gain, FET input, buffer amplifier. With this connection, it may be necessary to readjust the ADC zero. Do not change the AMP zero control.

An on-card memory must be loaded with the gain program for each channel from software control in the computer program. Gain A1 is selected by writing $XXX3_{16}$ into each desired channel at the selected channel addresses. Gain A2–A4 are selected by writing XXX2, XXX1 and XXX0, respectively.

Offset

When analog input signals range from zero upward or ± from zero, the amplifier should not be offset. Connecting REF 1, AMP LO, ANA COM, and ANA GND provides no offset. However, when analog input signals have a fixed minimum value and it is desired to utilize the entire scale range (e.g., V_{IN} = 1–5V), AMP LO can be offset by connecting to any of the reference voltages available from the on-card reference divider. These voltages are 0.1, 1, 5 and 10V; they are available at terminals V0.1, V1, V5 and V10. AMP LO can be offset to one value for gains A2–A4, and REF 1 can be offset to another value for gain A1. Perhaps, most common usage would be with only gain A1 offset, say to 1V for full scale range of 1–5V on A1 and zero referenced signals on the other gain settings. To effect this schedule, connect AMP LO to ANA GND and connect REF 1 to V1 as shown in *Figures 4, 6 and 7*. The AMP LO terminal is common for gains selected by A2–A4, while REF 1 is the equivalent AMP LO terminal for gain A1.

SAMPLE AND HOLD

The sample and hold circuit may be bypassed by connecting the AMP OUT and ADC IN terminals directly, as in *Figure 8*. If the sample and hold circuit is to be used, strap AMP OUT to S&H IN and strap S&H OUT to ADC IN, as in *Figure 7*. Since the S&H amplifier exhibits some offset and a slight gain error, both controls on the ADC for offset and full-scale may need readjustment if the S&H is bypassed. These 2 controls are factory adjusted for use with the S&H amplifier in the circuit.

ANALOG-TO-DIGITAL CONVERTER CONNECTIONS

The ADC may be used for either positive unipolar or for bipolar signals. When bipolar signals are to be coded, strap OFFSET to REF IN, strap CODE to COMP and strap D12 to BD11, as in *Figure 8*. This offsets the ADC range so that −10.240V is zero scale or $F800_{16}$ and 10.2375V is full-scale or $07FF_{16}$ in a 2's complement binary code with extended sign bit. If desired to use an offset binary code on bipolar signals, strap OFFSET to REF IN, CODE to BIN and D12 to L0, as in *Figure 11*. The result will be 0000_{16} for −10.240V input and $0FFF_{16}$ for 10.2375V input. To obtain extended sign, strap D12 to BD11 instead of L0.

Applications Information (Continued)

Channel Selection Logic

BA4	BA3	BA2	BA1	16-CH	8-CH
0	0	0	0	1	1–9
0	0	0	1	2	2–10
0	0	1	0	3	3–11
0	0	1	1	4	4–12
0	1	0	0	5	5–13
0	1	0	1	6	6–14
0	1	1	0	7	7–15
0	1	1	1	8	8–16
1	0	0	0	9	None
1	0	0	1	10	None
1	0	1	0	11	None
1	0	1	1	12	None
1	1	0	0	13	None
1	1	0	1	14	None
1	1	1	0	15	None
1	1	1	1	16	None

When using unipolar positive signals, strap OFFSET to ADC IN, strap CODE to BIN, and strap D12 to LO, as in *Figure 12* to obtain 0000_{16} at 0V input and $0FFF_{16}$ at 10.2375V input.

In all cases, the analog signal from the S&H is applied to the ADC by strapping S&H OUT to ADC IN.

REFERENCE

To use the internal reference, strap REF OUT to REF IN, as in *Figures 10 and 12*. To use an external 10.24V reference, connect the external reference positive to REF IN and negative to ANA GND, as in *Figure 10*. To use an external 10.00V reference, connect as for external 10.24V reference and also strap REF IN to V10. When using an external reference, it may be necessary to readjust the full-scale potentiometer which is factory set for the internal reference.

CHANNEL SELECTION

Channel selection is made by applying the appropriate digital code to terminals BA1 through BA4 in the following manner:

For 16 channel, strap MUX SEL to 16-CH. For 8 channel differential, strap MUX SEL to 8-CH.

Loading an address location with a gain-set data word (see AMPLIFIER, Gain, on previous page) will set the MUX to the addressed channel and initiate a conversion. The new data will be available approximately 120 μs later. By repeated (or selective) write gain operations, a desired channel may be repeatedly (or selectively) commanded to generate new data if desired.

ADDRESS DECODING

The data acquisition card is memory mapped and data is accessible by a memory read instruction at normal memory speeds. The system will work with either a 16 or an 8-bit data bus; addressing connections are slightly different for the two.

The BA terminals and the T terminals are compared to select the appropriate address code. For example, if a code of 0111 is desired, set the T terminals to code 0111.

The logic signals presented to address lines BA0–BA4 must remain stable during the data read or write access period. However, it is possible to latch address lines BA5–BA16 on a rising edge at the ADRS line. When no latching is required, strap ADRS to LO.

CONTROL BUS CONNECTIONS

The control bus connections are ADRS, MEMSEL, READ, WRITE, READY, and NINIT. READY is an output signal to the processor, and the other 5 are inputs to the data acquisition card. Logic sense select pins are also available as TMEM, TREAD and TWRITE. The sense of the READY signal may also be strap selected. These sense selections allow use of the card with almost any processor bus.

NINIT

An initializing signal from the processor at time of power-up or whenever commanded will initialize the data acquisition card by resetting the internal address counter to channel 1. This must be a negative true signal.

Applications Information (Continued)

CONNECT TERMINAL	FOR 16-BIT DATA BUS	FOR 8-BIT DATA BUS	STRAP FOR 8-BIT DATA BUS
T0	L0	VL	BD0 to BD8
BA0	L0	ADR0	BD1 to BD9
BA1	ADR0	ADR1	BD2 to BD10
BA2	ADR1	ADR2	BD3 to BD11
BA3	ADR2	ADR3	BD4 to BD12
BA4	ADR3	ADR4	BD5 to BD13
BA5	ADR4	ADR5	BD6 to BD14
BA6	ADR5	ADR6	BD7 to BD15
BA7	ADR6	ADR7	
BA8	ADR7	ADR8	
BA9	ADR8	ADR9	
BA10	ADR9	ADR10	Note. See *Figures 13–16* for examples
BA11	ADR10	ADR11	
BA12	ADR11	ADR12	
BA13	ADR12	ADR13	
BA14	ADR13	ADR14	
BA15	ADR14	ADR15	
BA16	ADR15	L0	
T16	L0 or VL	L0	
T5–T15	L0 or VL	L0 or VL	

MEMSEL

This input must be true to select the data card; it is normally connected to a memory select line or a memory/IO line. For positive true select, strap TMEM to L0. For zero true select, strap TMEM to VL. If there is no processor line of similar function, MEMSEL is strapped to READ and TMEM is strapped to WRITE. This insures that the on-card clock will be interrupted for the minimum possible period corresponding to the actual READ time.

READ

This input must be true to read data from the card; it is normally connected to a memory read control line. For positive true read, strap TREAD to VL. For zero true read, strap TREAD to L0.

WRITE

This input must be true to write a gain program into the card; it is normally connected to a memory write control line. For positive true write, strap TWRITE to L0. For zero true write, strap TWRITE to VL.

READ/WRITE

For use with processors having a single READ/WRITE control line, strap the READ and WRITE lines together and connect to the processor read/write line. For READ/$\overline{\text{WRITE}}$ operation, strap both TREAD and TWRITE to VL. For $\overline{\text{READ}}$/WRITE operation, strap both TREAD and TWRITE to V0.

ADRS

The ADRS line may be used to latch address data presented to inputs BA5–BA16. Data is latched on a rising (trailing) edge and is unlatched on the next falling edge. There is no latching capability at any other input. In most applications, the ADRS line is strapped to L0; and no latching takes place. However, there are some processors such as the PACE which utilize a single set of lines for both address and data. In these systems, an interface latch must be provided to hold the address data during the data transmission period. Using this card with a PACE system requires only a single 4-bit latch to hold address bits applied at BA1–BA4.

READY

The ready output signal indicates to the processor that the data card is ready to accept data in the write mode or that valid data will be on the bus in the read mode; it is normally connected to the processor ready or wait control line. In the read mode, the READY output will be available by 120 ns after a read command is received by the card; data will be on the bus by 220 ns after the read command. In the write mode, READY will be available by 850 ns after the write signal is received. The processor will not have to enter a wait cycle in the read mode; however, a wait cycle is necessary in the write mode due to internal timing requirements on the data card. To obtain a positive true READY signal, strap SEL RY to RY. To obtain a zero true READY signal, strap SEL RY to NRY.

DATA LINES

The data card may be used with either 8 or 16-bit data busses. For 16-bit busses, all 16 data lines are available. For 8-bit busses, the lower 8 bits must be paralleled with the upper 8 bits. Connect BD0 to BD8, BD1 to BD9, and so forth through BD7 to BD15. See under heading Analog-to-Digital Converter Connections for consideration of bits 12–15. The 12-bit data appears right justified on a 16-bit data field. For 2's complement bipolar data, the sign bit is extended to the 4 most significant bits. For binary data, the 4 most significant bits are zeros. All data is positive true. By reconnecting or reassigning data bus terminals, it is possible to connect for left-justified data on a 16-bit data bus. This is not possible for an 8-bit data bus. In this case, connect the CODE terminal to L0 to set the 4 unused bits to zero, per *Figure 10*.

Applications Information (Continued)

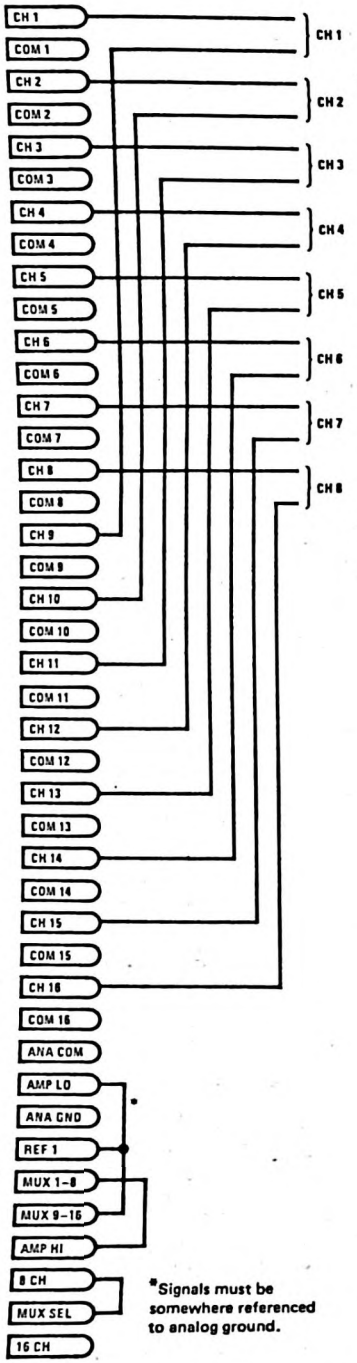


FIGURE 1. 8-Channel Differential Connection

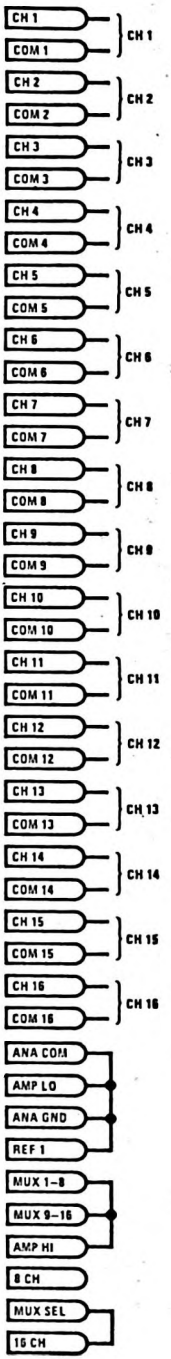


FIGURE 2. 16-Channel Single-Ended Connection

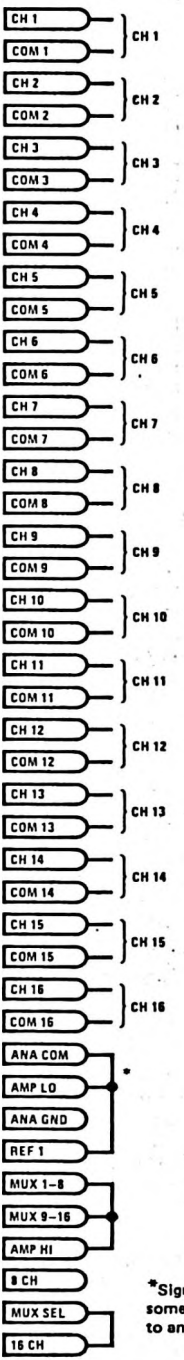
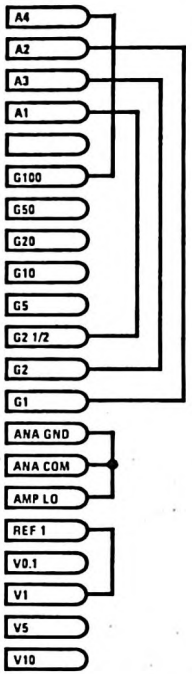


FIGURE 3. 16-Channel Quasi-Differential Connection

Applications Information (Continued)



A4 Gain = 100 Range = 0–102.375 mV 1 LSB = 25 μV
A2 Gain = 1 Range = 0–10.2375V 1 LSB = 2.5 mV
A3 Gain = 2 Range = 0–5.11875V 1 LSB = 1.25 mV
A1 Gain = 2 1/2 Range = 1–5.095V 1 LSB = 1 mV

FIGURE 4. Gain and Offset Connections, An Example **(See Page 5)**

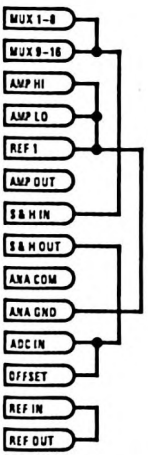


FIGURE 5a. Amplifier Completely Bypassed

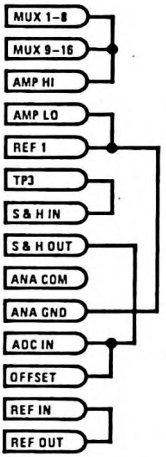


FIGURE 5b. Amplifier Bypassed Except for Single-Ended, Precise Unity-Gain FET Buffer

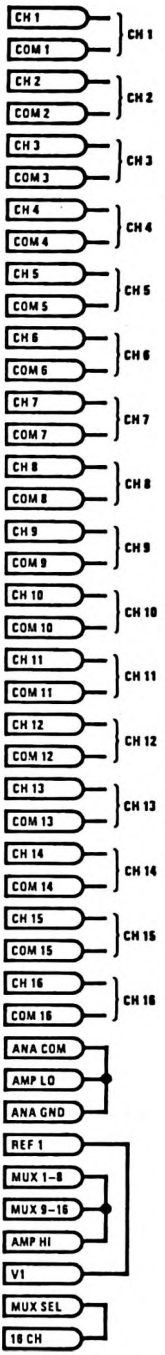
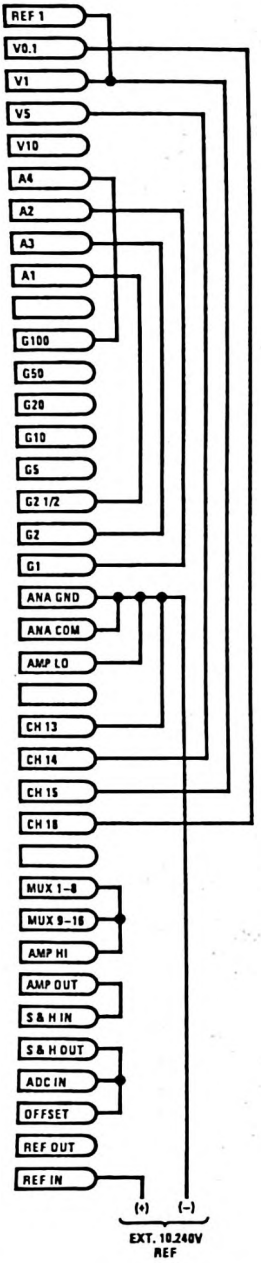


FIGURE 6. 16-Channel Single Ended Connection, One or More Channels Offset 1V as with V_{IN} = 1–5V

Applications Information (Continued)



Ch 13 = 0V REF A4 Gain = 100 Range = 0–102.375 mV 1 LSB = 25 μV
Ch 14 = 5V REF A2 Gain = 1 Range = 0–10.2375V 1 LSB = 2.5 mV
Ch 15 = 1V REF A3 Gain = 2 Range = 0–5.11875V 1 LSB = 1.25 mV
Ch 16 = 100 mV REF A1 Gain = 2 1/2 Range = 1–5.095V 1 LSB = 1 mV

FIGURE 7. Example of Analog Connection with Multiplexed Reference Voltages for Calibration Purposes (Consider Accuracy of Internal REF If Used)

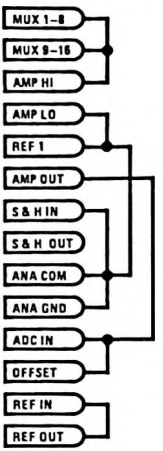


FIGURE 8. Sample and Hold Bypassed

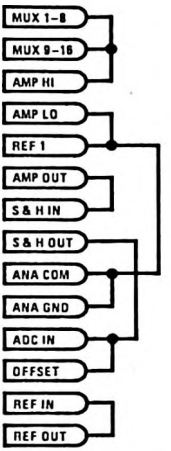


FIGURE 9. Normal MUX, AMP, S & H and ADC Interconnections

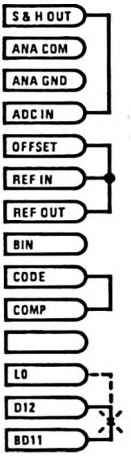


FIGURE 10. ADC, CODE and Logic Connections for Bipolar Inputs with Internal REF; 2's Complement Binary Output Code Data is Right-Justified, Extended Sign. For Left-Justified Data, Connect D12 to L0 Rather than to BD11, and Reassign Bits 12–15 as Bits 0–3. This is applicable Only to 16-Bit Data Bus Operations.

Applications Information (Continued)

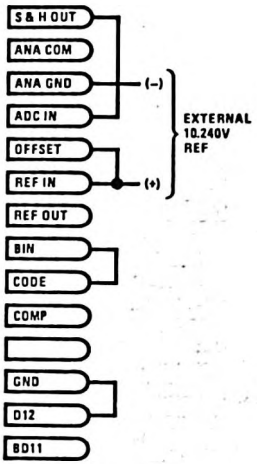


FIGURE 11. ADC, CODE and Logic Connections for Bipolar Inputs with External REF; Offset Binary Output Code Data is Right-Justified, Bits 12–15 are Zeros. For Left-Justified Data on a 16-Bit Data Bus, Reassign Data Bits 12–15 as Bits 0–3.

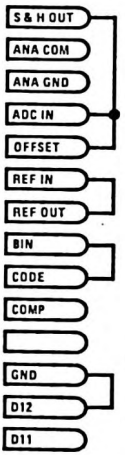


FIGURE 12. ADC, CODE and Logic Connections for Unipolar Inputs with Internal REF; Binary Output Code Data is Right-Justified, Bits 12–15 are Zeros.

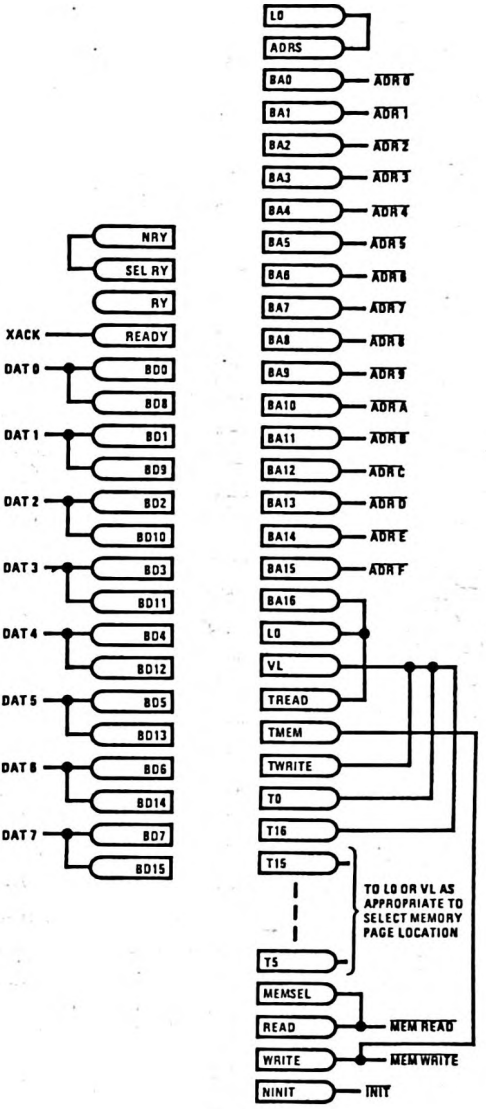


FIGURE 13. Bus and Logic Connections for 80/10 System

Applications Information (Continued)

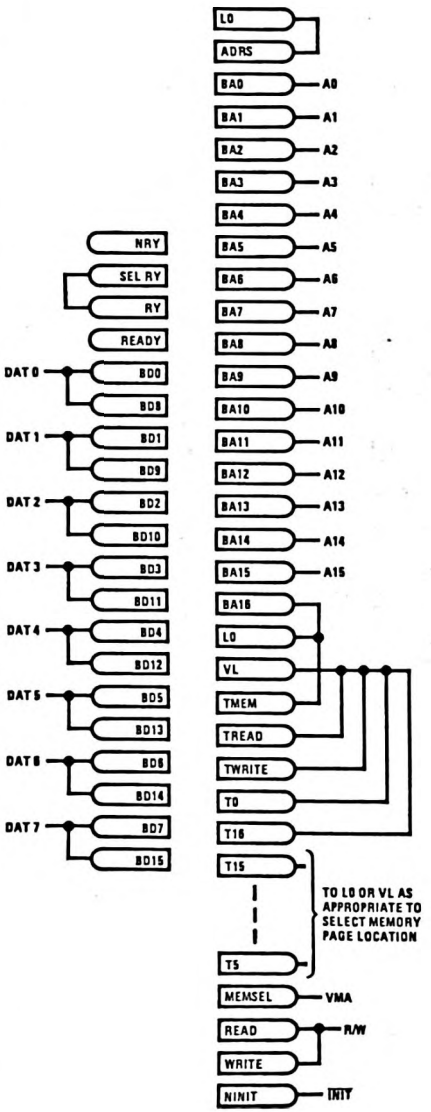
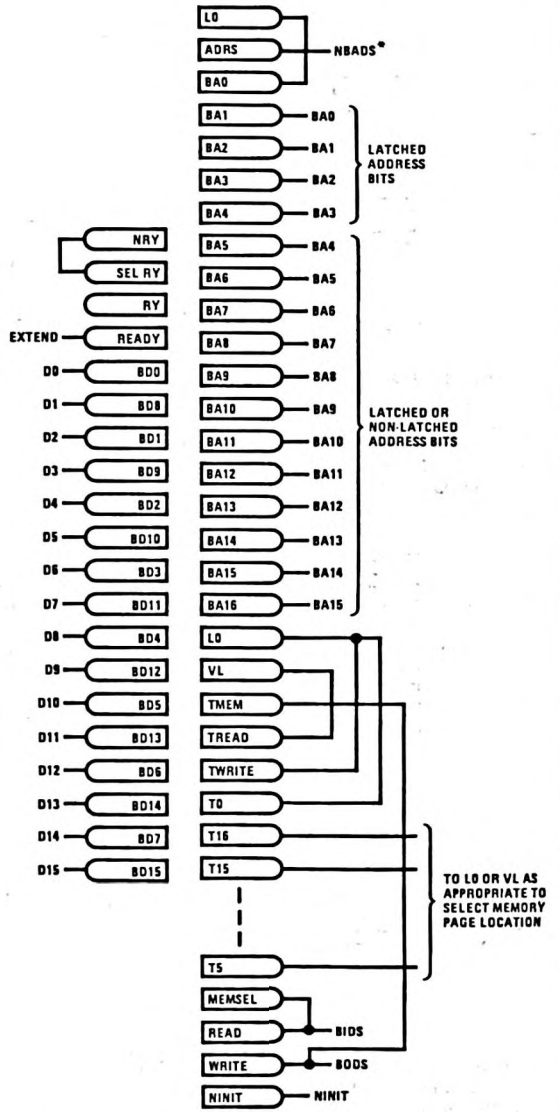


FIGURE 14. Bus and Logic Connections for 6800 System



*To LO when all address bits are latched on the CPU card

FIGURE 15. Bus and Logic Connections for PACE

Applications Information (Continued)

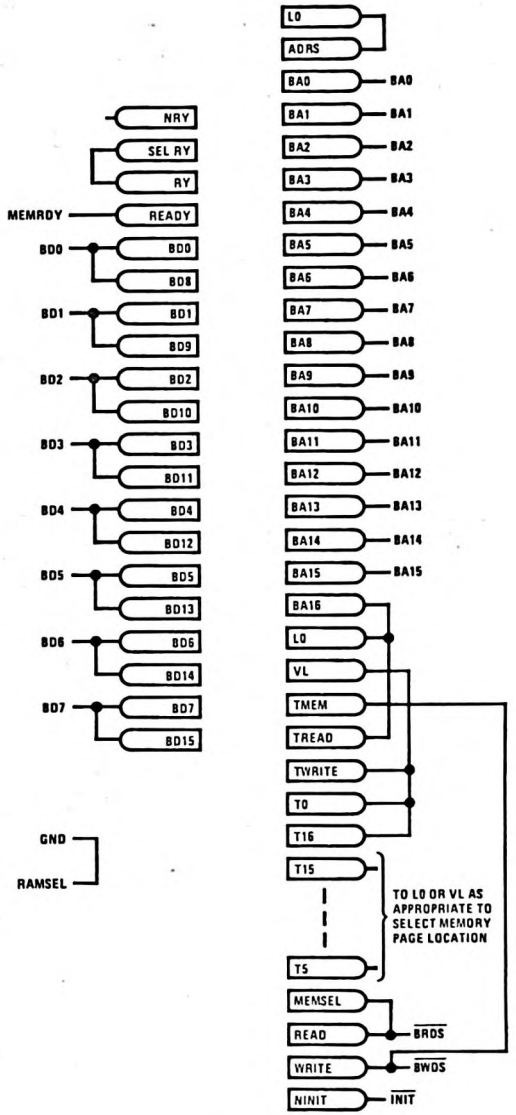
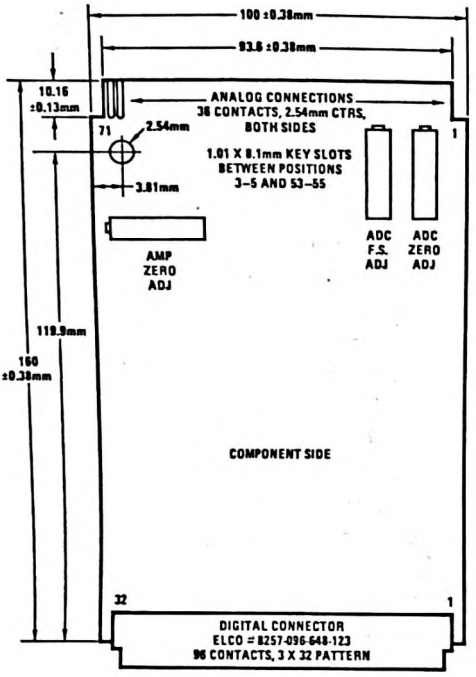
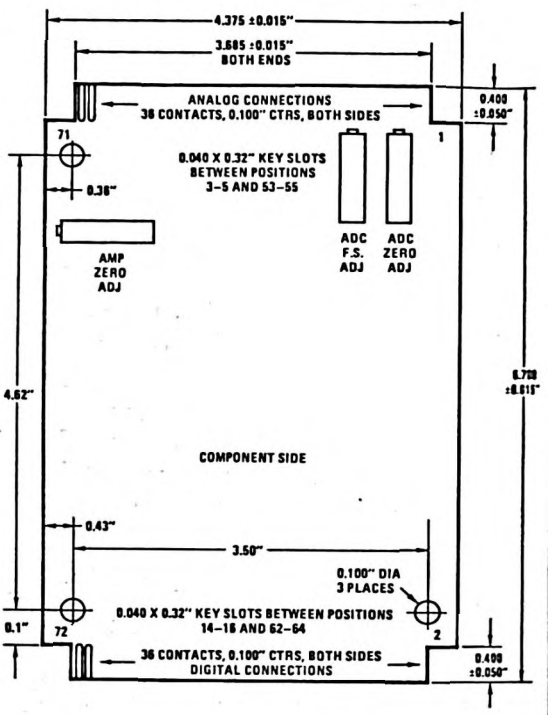
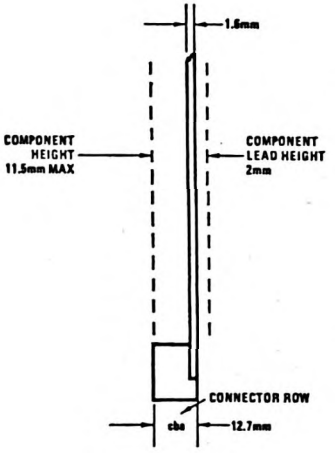


FIGURE 16. Bus and Logic Connections for SC/MP CPU with External RAM

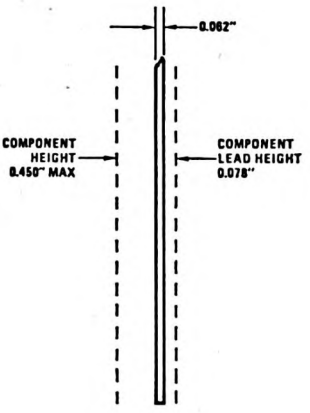
Physical Dimensions inches (millimeters)







Eurocard Version
Order Number ADS1216HCE



L Version
Order Number ADS1216HCL

Section 5

Digital Voltmeters

5

National Semiconductor

ADB4511 4 1/2-Digit Digital Panel Meter Controller

General Description

The ADB4511 (DM8703) is a complete controller for a low-cost 4 1/2-digit dual slope digital panel meter. It is designed to complement the LF13300 integrating A/D building block to provide a low cost, minimum parts count 4 1/2-digit DPM. The ADB4511 uses I^2L technology. It provides segment current for large digit 7-segment displays which is programmable with a single resistor. Overrange with valid polarity is indicated by displaying +EEEE or −EEEE. Auto zeroing, polarity output and all other required control functions are provided. The end-of-conversion output may be tied to the start conversion input enabling continuous conversion. An on-chip clock oscillator is provided or an external clock may be used.

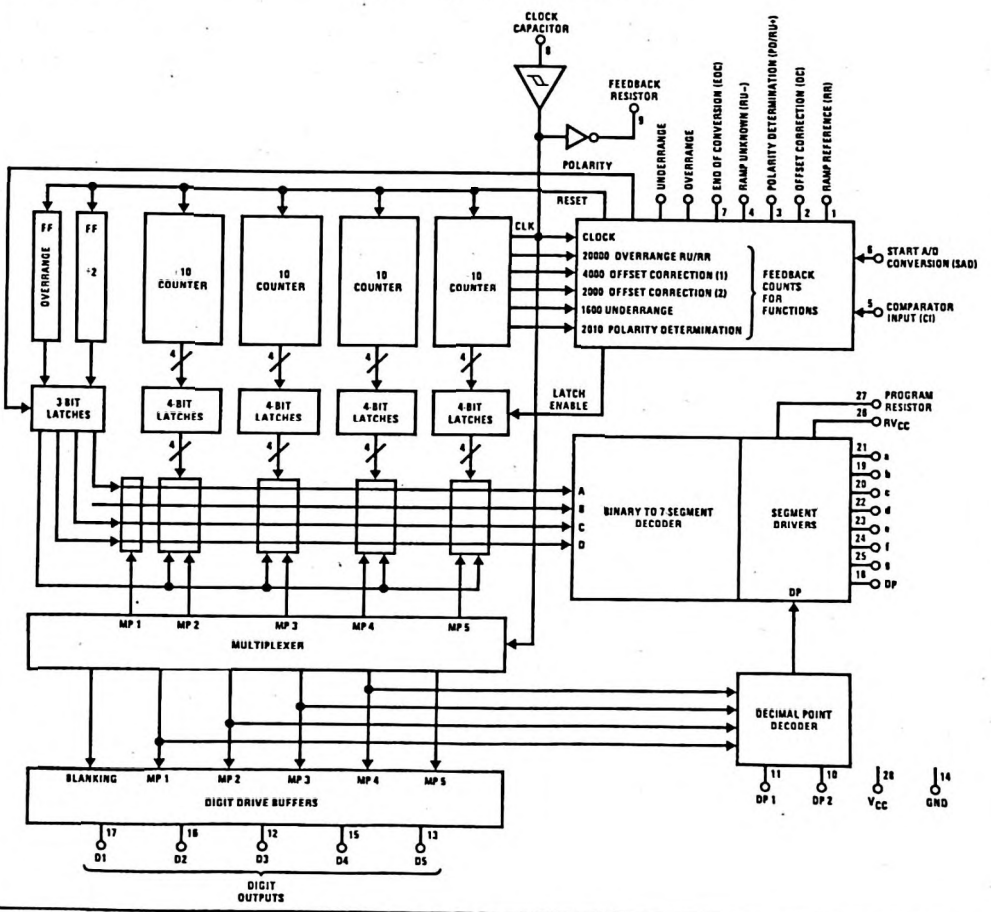
Features

- Complete controller for low cost 4 1/2-digit dual slope DPM
- Minimum external parts count
- Complements LF13300 analog building block
- Drives large LED segments directly
- Polarity indication
- Overrange indication
- Auto zero control
- Single 5V supply
- On-chip clock oscillator

Note. See LF13300 data sheet for additional information.

Block Diagram

4 1/2-Digit Panel Meter Controller



Absolute Maximum Ratings (Note 1)

Supply Voltage	5.5V
Input Voltage	5.5V
Output Voltage (Digits)	5.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	See graph 4
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
V_{CC1}	4.5	5.5	V
V_{CC2} (Note 2)	4.5	5.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 3 and 4)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS (EXCEPT CLOCK)						
V_{IH}	Logic "1" Input Voltage	V_{CC} = Min	2.0			V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IN} = 2.7V			20	µA
		V_{CC} = Max, V_{IN} = 5.5V			0.1	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−1.5	V
V_{IL}	Logic "0" Input Voltage	V_{CC} = Min			0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.36	mA
CLOCK INPUT						
V_{IHC}	Logic "1" Input Voltage		1.9		2.6	V
V_{ILC}	Logic "0" Input Voltage		1.0		1.6	V
I_{IHC}	Logic "1" Input Current				50	µA
V_{CDC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
OUTPUTS — (EXCEPT SEGMENTS & DIGITS)						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OUT} = −400 µA	2.4			V
I_{OH}	Logic "1" Output Current	V_{CC} = Min			−400	µA
I_{OS}	Output Short-Circuit Current (Note 5)	V_{CC} = Max, V_{OUT} = 0V	−18		−55	mA
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 4 mA			0.4	V
I_{CC}	Supply Current	V_{CC1} = Max, Pin 28			90	mA
$I_{CC2\text{-}ON}$	Supply Current	V_{CC2} = Max, All Segments ON, Pin 26			600	mA
$I_{CC2\text{-}OFF}$	Supply Current	V_{CC} = Max, All Segments OFF, Pin 26 (@ Pin 27 = 0V)			1	mA
SEGMENT OUTPUTS						
I_{OL3}	Low Level Output Current	V_{CC} = Max, V_{OUT} = 1.0V			−100	µA
I_{OH3}	High Level Output Current	V_{CC} = Max, R_{PROG} = 7.2k, (Note 6)	−50		−75	mA
V_{OH3}	High Level Output Voltage	V_{CC} = Max, I_{OUT} = −75 mA	2.7			V
RV_{CC}	Supply Pin	V_{CC} = Min, I_{CCR} = 600 mA, V_{OUT} = 2.7V			3.2	V
DIGIT OUTPUTS						
V_{OL4}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 0 µA			0.2	V
I_{OH4}	High Level Output Current	V_{CC} = Min, V_{OUT} = 1V	7			mA
CLOCK						
f_c	Clock Frequency	R = 80k to 200k, C = 50 pF to 200 pF	30		300	kHz
f_{MUX}	Multiplex Frequency	1/320th of Clock Frequency	94		940	Hz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{CC2} supply is connected to RV_{CC} pin on package through a protection resistor, which dissipates power external to the package, according to the graph *(Figure 3)*.

Note 3: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the device. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: All currents into device pins shown as positive, out of device as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 5: Only one output at a time should be shorted.

Note 6: The current/segment specified is peak current for a 5-digit multiplexed system, which works out to be 15 mA/segment average DC current.

Functional Description

OPERATION

The ADB4511 is designed for use with the LF13300 dual slope DVM analog front end. Four control signals are supplied to the LF13300 and one control signal is required from the LF13300. The conversion cycle is composed of 5 distinct phases *(Figure 4)*:

Phase I – Polarity Determination
Phase II – Initialization
Phase III – Ramp Unknown
Phase IV – Ramp Reference
Phase V – Offset Correction and Standby

Phase I – Polarity Determination (2,010 Clock Periods)

This phase is initiated by taking the start A/D conversion (SAD) input to a logic "1" momentarily ($\geq$ 1 CP). It is used to determine polarity of the analog input. At the 2000th clock period, COMP from the LF13300 is examined for polarity. If COMP = logic "1", then the input voltage is positive. If COMP = logic "0", then the input is negative. The polarity determination signal (PD/RU+) will be at a logic "1" during this entire phase. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion (see LF13300 data sheet).

Phase II – Initialization (4000 Clock Periods)

This phase is identical to Phase V and is used by the LF13300 to eliminate any offsets induced as a result of the Polarity Detect Phase. Offset Correction (OC) will be at a logic "1".

Phase III – Ramp Unknown (20,000 Clock Periods)

The unknown input voltage is integrated for a fixed time, 20,000 clock periods, during this phase. The result of the Phase I Polarity Detect Cycle determines whether PD/RU+ or RU– will be at logic "1". If Phase I indicates a positive input, the PD/RU+ signal will be a logic "1". If Phase I indicates a negative output, Ramp Negative (RU–) will be a logic "1". These 2 signals will never be at logic "1" simultaneously.

Phase IV – Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be in the logic "1" state. When COMP goes to a logic "0" state, or when the internal counter reaches 100% of full-scale (20,000 periods), the Ramp Reference (RR) signal goes to the logic "0" state and the counter output is loaded into the output register. The Polarity Bit will reflect whatever value was determined during Phase I. The output register will hold the data until a new conversion is completed and new data is loaded into the register. "EEEE" will be displayed in case of overrange.

Phase V – Offset Correction (2000 Clock Periods)

The LF13300 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase. The end of conversion (EOC) goes to logic "1" after this cycle and the system goes into the Standby mode.

Offset Correction (OC) output remains at logic "1" after OEC, thus the system is continuously corrected during the Standby mode.

Clock Generator: The ADB4511 has an on-chip clock generator whose frequency is adjustable by external R_{OSC} and C_{OSC} components. An external clock could be used with C_{OSC} as the clock input.

Counters: The ADB4511 has four ÷10 counters and one ÷2 counter for a count of 20,000 clock pulses. The counters advance at the negative-going clock edge.

Decimal Point: The decimal point output is a constant current source. Decimal point inputs 1 and 2 are decoded to drive either of the 4 positions MSD, SSD, ThSD, FSD (most, second, third and fourth significant digits). The decimal point inputs are CMOS and TTL compatible.

Digit Drivers: The digit drive buffers are multiplexed emitter follower outputs. The modulo 5 multiplex counter is triggered by the positive-going clock edge, making the multiplex rate 1/320 of the clock frequency. One-eighth of each digit ON interval is blanked, to avoid ghosting.

Segment Outputs: The 7-segment outputs are multiplexed in a similar fashion to the digit outputs. These outputs are constant current sources, and are programmable with one external resistor, Rp, *(Figure 2)*. The most significant digit (+1) is also decoded to be displayed with the same 7-segment outputs.

Power Supply: Only one supply is required for the system. Two supply pins are provided on the chip in order to make the interface between the digital and analog chip noise-free and to lower the power dissipation on-chip. RV_{CC} is connected to the output segment source drivers through an external resistor, R_{EX}, to reduce on-chip power dissipation *(Figure 3)*.

Typical Performance Characteristics

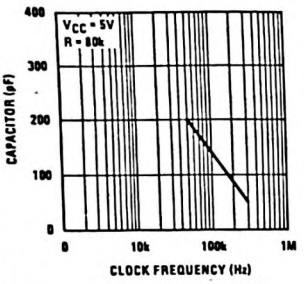


FIGURE 1. Capacitor vs Clock Frequency

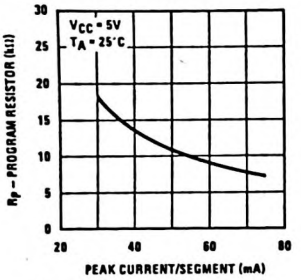
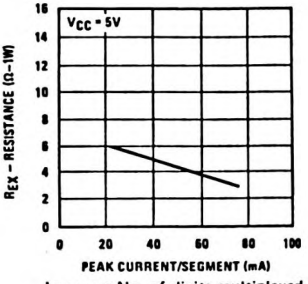


FIGURE 2. Program Resistor vs Peak Current/Segment



I_{PEAK} = No. of digits multiplexed x DC current/segment

Note. R_{EX} should be ±1W, ±5% tolerance.

FIGURE 3. Resistance vs Peak Current/ Segment

Timing Diagram

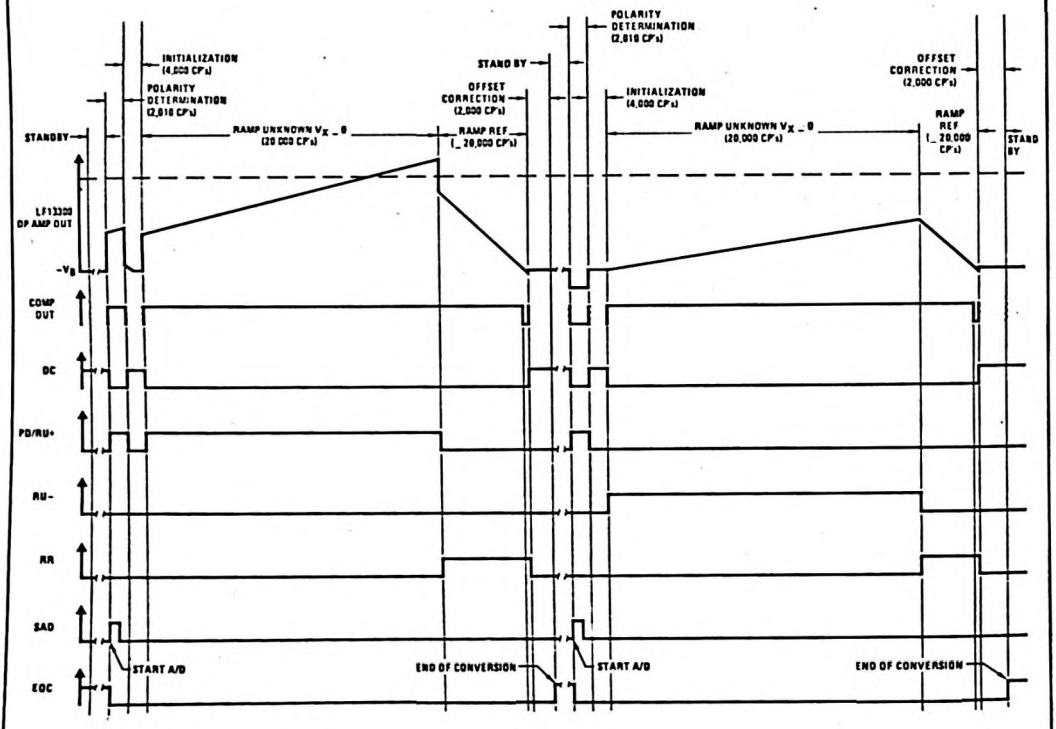
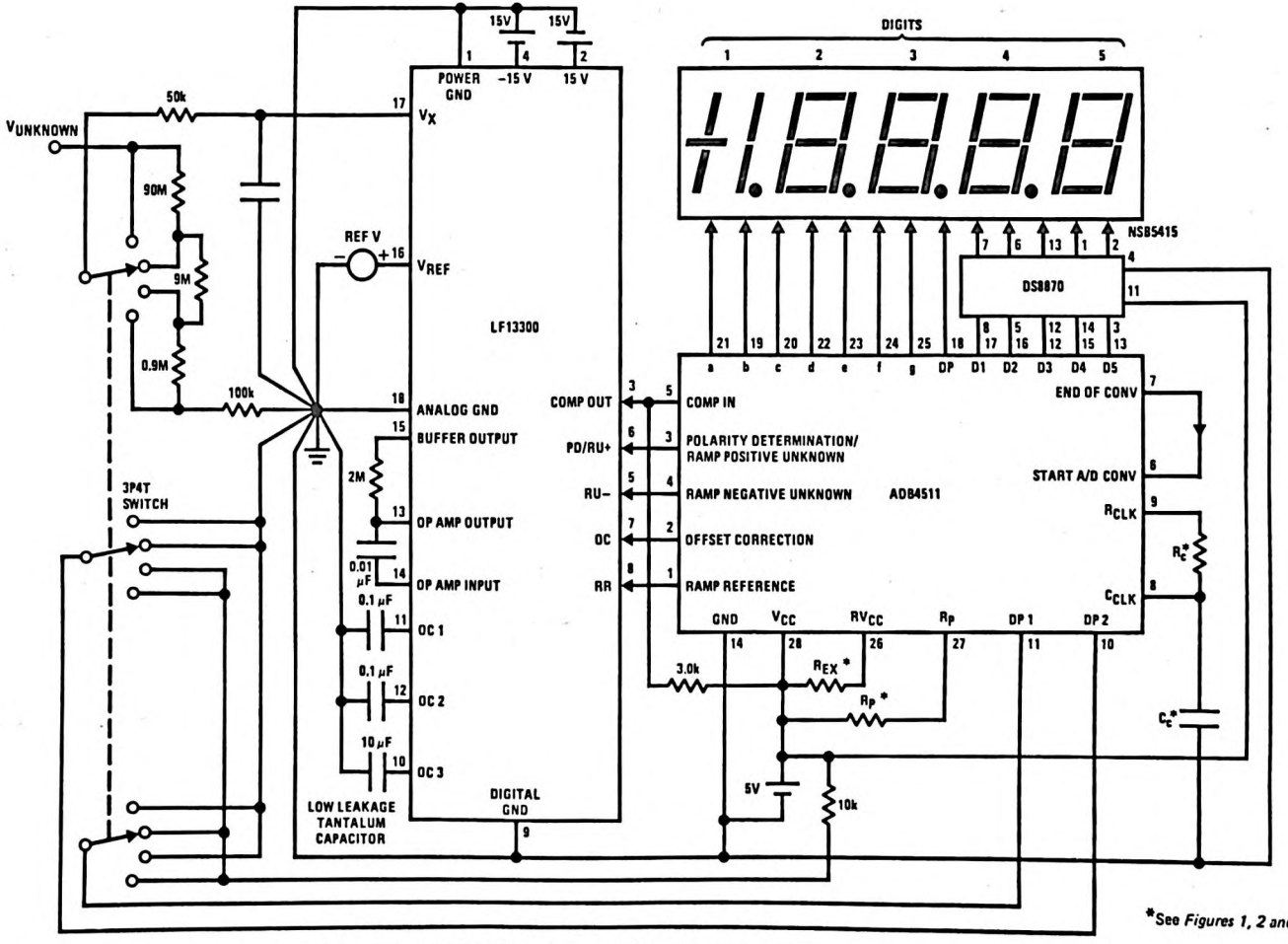


FIGURE 4

4 1/2-Digit DVM Application



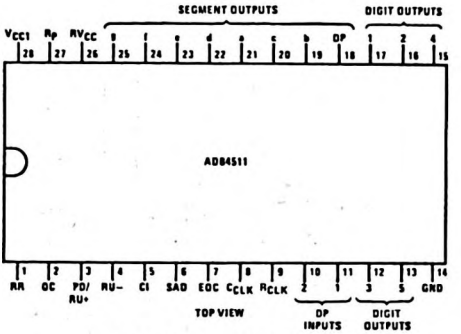
*See *Figures 1, 2 and 3* for values

Connection and Schematic Diagrams

Decimal Point Addressing

DP 1	DP 2	DIGIT POSITION
0	0	D4, FSD
1	0	D3, ThSD
0	1	D2, SSD
1	1	D1, MSD

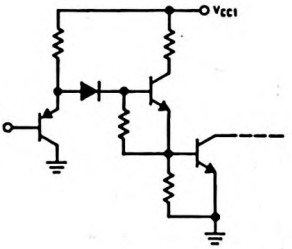
Dual-In-Line Package


SEGMENT OUTPUTS
DIGIT OUTPUTS
VCC1 RP RVCC g f e d a c b DP 1 2 4
28 27 26 25 24 23 22 21 20 19 18 17 16 15
ADB4511
1 2 3 4 5 6 7 8 9 10 11 12 13 14
RR OC PD/RU+ RU− CI SAD EOC CCLK RCLK 2 1 3 5 GND
TOP VIEW
DP INPUTS
DIGIT OUTPUTS

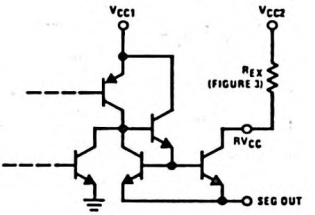
Order Number ADB4511N
See NS Package N28A

Inputs

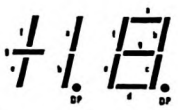
Decimal Point (DP)
Start A/D (SAD)
Comparator (CI)

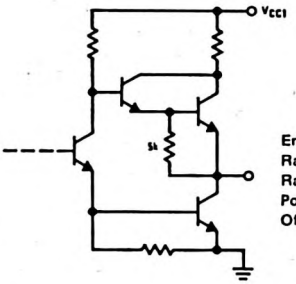


Segment Outputs



Segment Identification

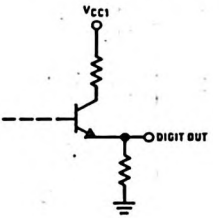




Control Outputs

End of Conversion (EOC)
Ramp Unknown (RU)
Ramp Reference (RR)
Polarity Determination (PD)
Offset Correction (OC)

Digit Outputs



National Semiconductor

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

general description

The ADD3501 (MM74C935-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

features

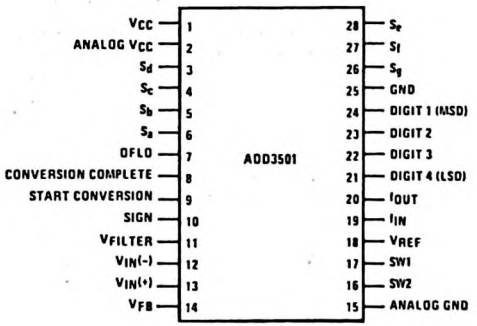
- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed — 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

connection diagram (Top View)

Dual-In-Line Package



Order Number ADD3501CCN
See NS Package N28A

absolute maximum rating (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A = 25°C$	800mW
derate at $\theta_{JA(MAX)} = 125°C/Watt$ above $T_A = 25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

electrical characteristics $4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

ADD3501

PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA @ $T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30$ mA @ $T_J = 100°C$	$V_{CC} - 1.6$ $V_{CC} - 1.6$	$V_{CC} - 1.3$ $V_{CC} - 1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/–, Oflo Outputs)	$V_{CC} - 0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	–1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64,512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

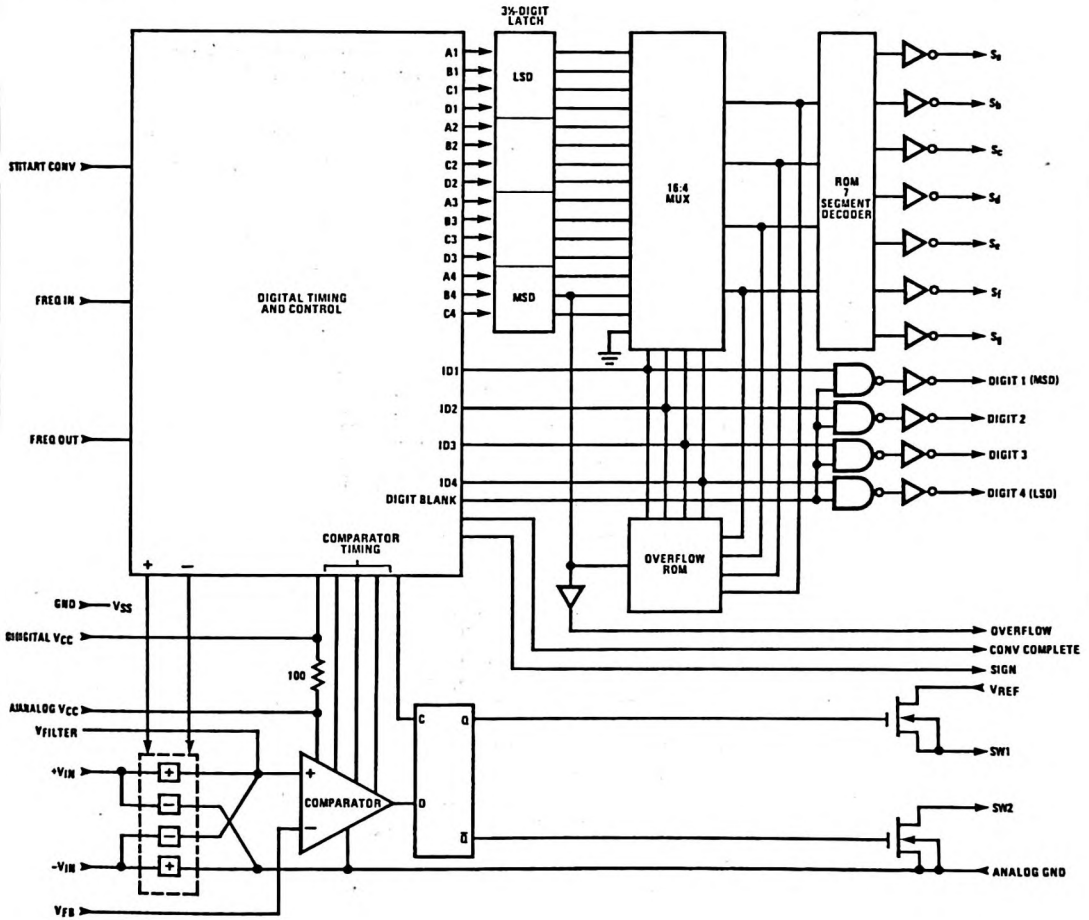
Note 2: All typicals given for $T_A = 25°C$.

electrical characteristics ADD3501

t_C = 5 conversions/second, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

Non-Linearity	V_{IN} = 0 – 2V Full Scale V_{IN} = 0 – 200mV Full Scale	–0.05	±0.025	+0.05	% of full scale
Quantization Error		–1		+0	counts
Offset Error, V_{IN} = 0V		–0.5	+1.5	+3	mV
Rollover Error		–0		+0	counts
Analog Input Current (V_{IN}+, V_{IN}–)	T_A = 25°C	–5	±0.5	+5	nA

block diagram



ADD3501 3½-Digit DVM Block Diagram

theory of operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON}+T_{OFF}}\right) = V_{REF}(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

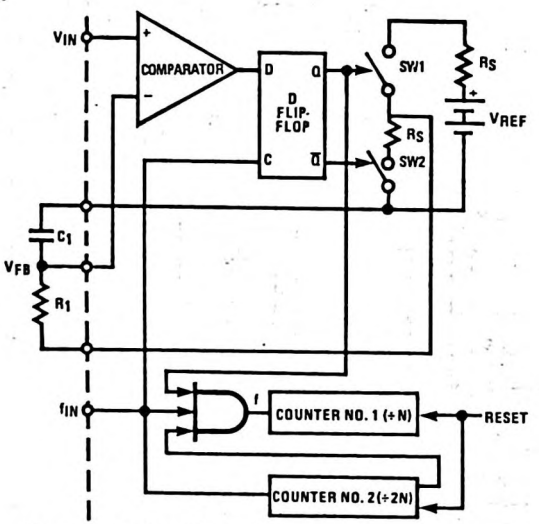
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3501, N = 2000.

schematic diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

general information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 64,512 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ and the minimum time is 256 x $1/f_{IN}$.

timing waveforms

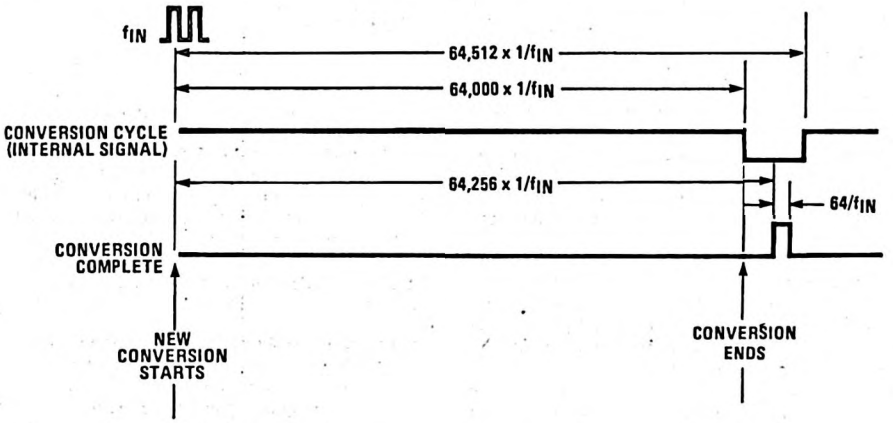


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

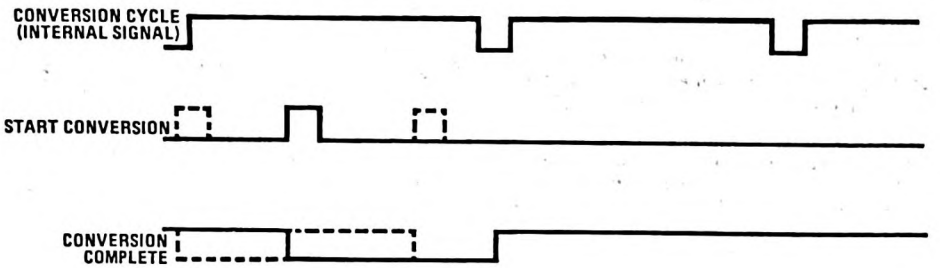


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

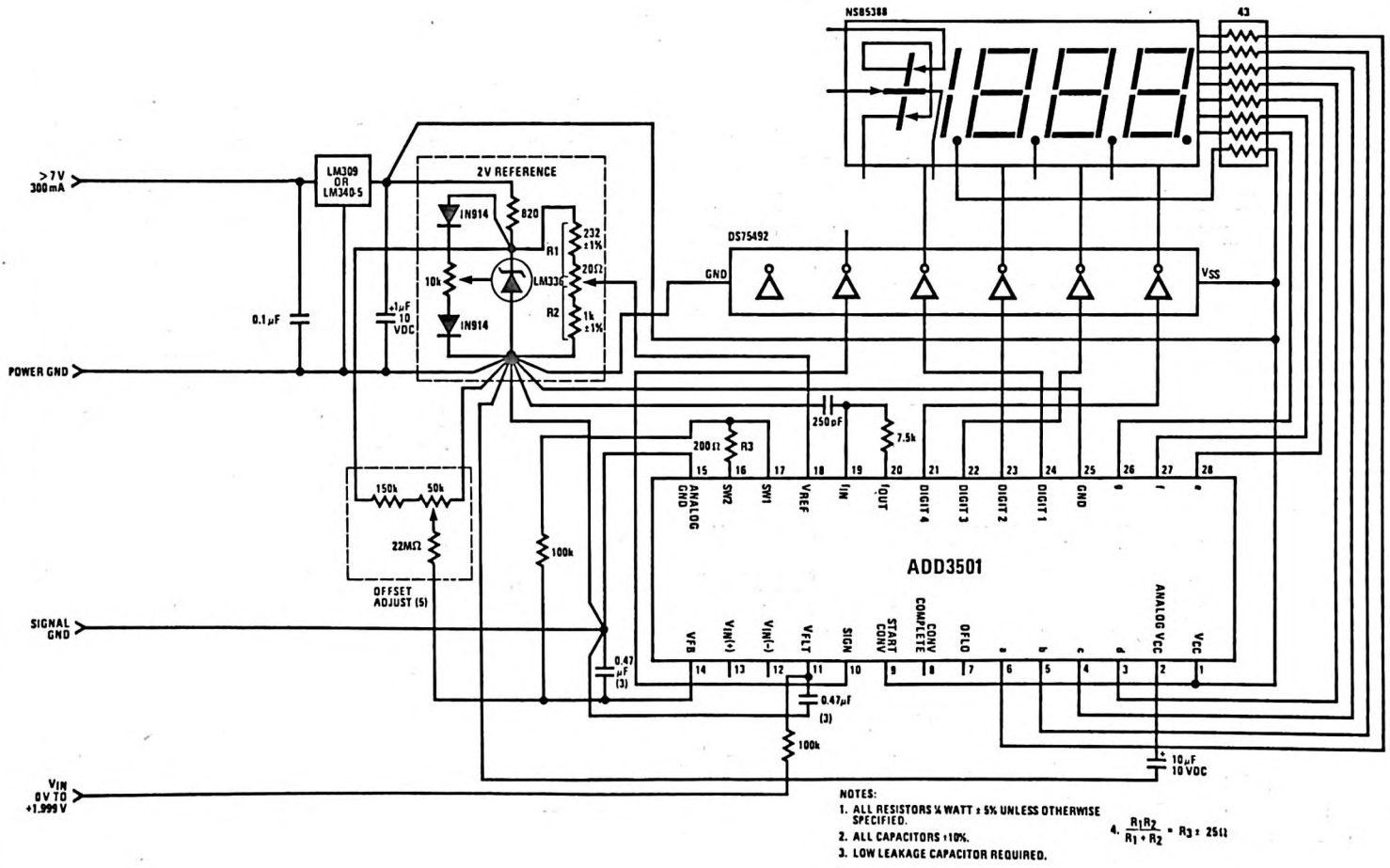
Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 6.

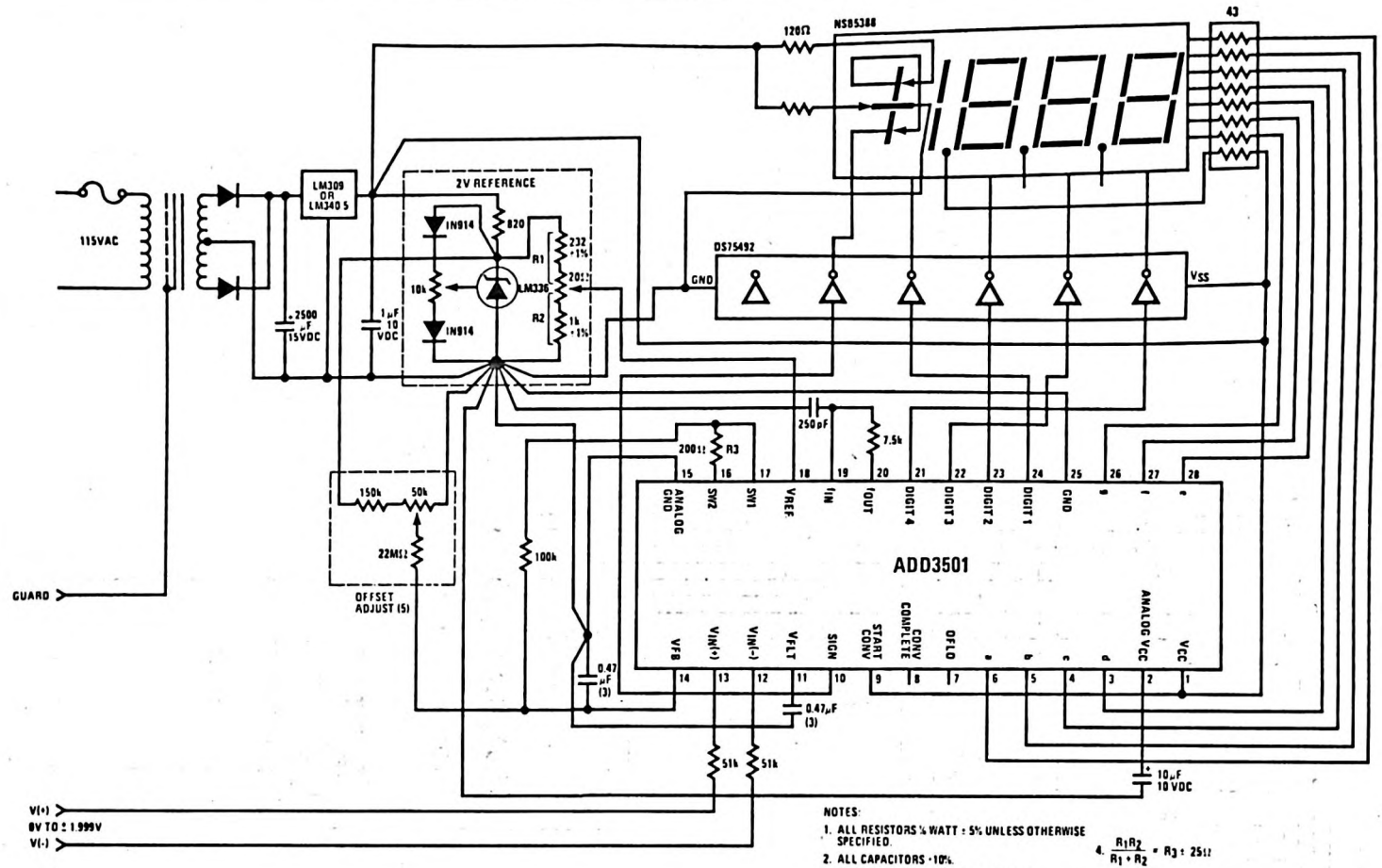
Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:
1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 4. 3½-Digit DPM, +1.999 Volts Full Scale



NOTES:
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4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 5. 3½-Digit DPM, ±1.999 Volts Full Scale

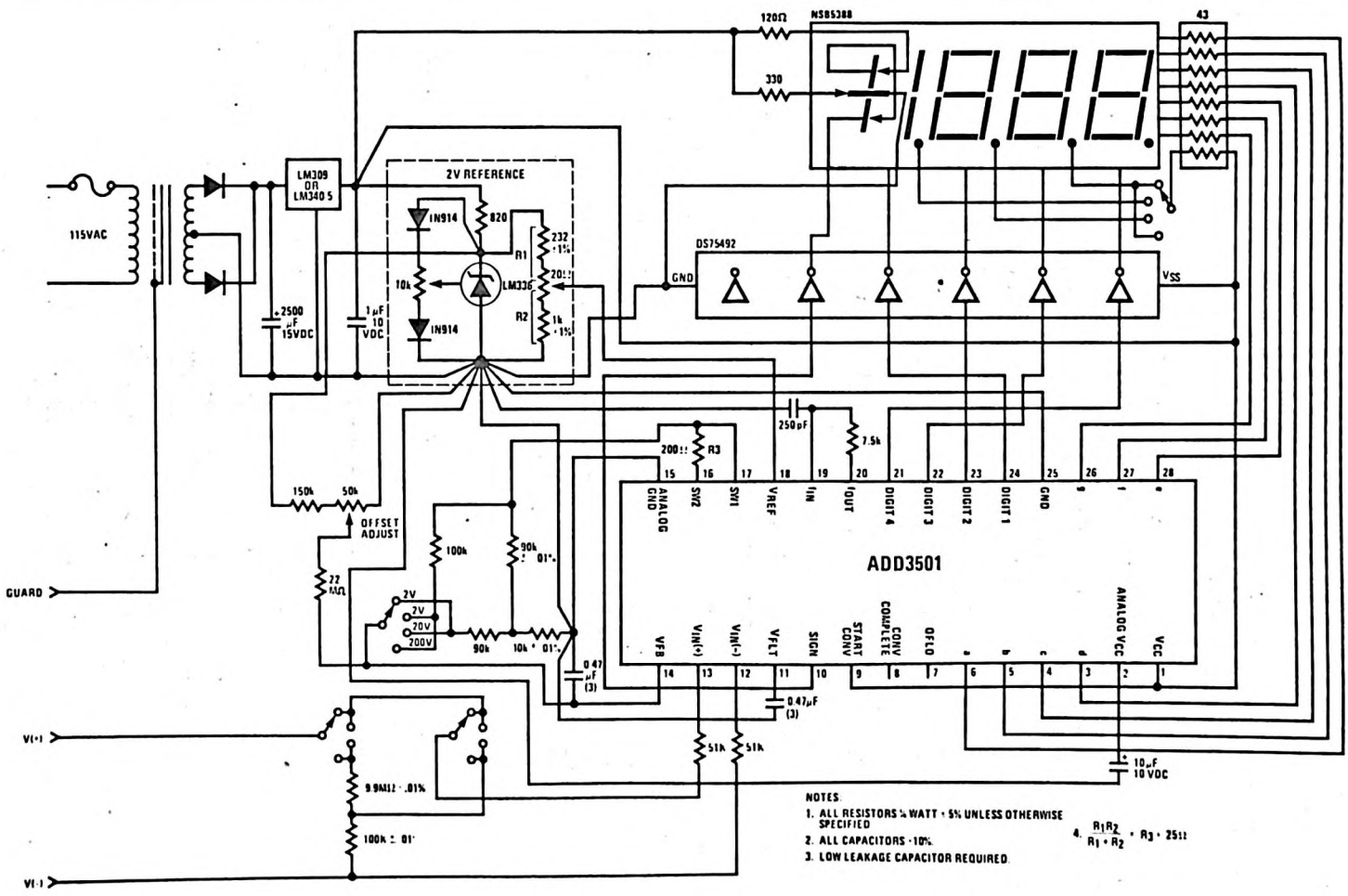


Figure 6. 3½-Digit DVM, Four-Decade, ±0.2 V, ±2 V, ±20 V and ±200 V Full Scale

National Semiconductor

ADD3701 3¾ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5 V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

Features

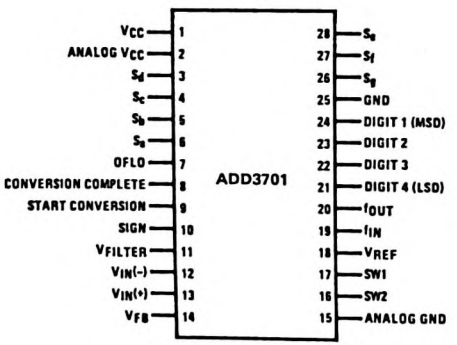
- Operates from single 5 V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram (Top View)

Dual-In-Line Package



Order Number ADD3701CCN
See NS Package N28A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	800mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics ADD3701

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Parameter		Conditions	Min	Typ[2]	Max	Units
$V_{IIN(1)}$	Logical "1" Input Voltage		V_{CC} − 1.5			V
$V_{IIN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OOUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digit Outputs)	I_O = 1.1 mA			0.4	V
$V_{OOUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	I_O = 0.7 mA			0.4	V
$V_{OOUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	I_O = 50 mA @ T_J = 25°C V_{CC}=5V I_O = 30 mA @ T_J = 100°C	V_{CC} − 1.6 V_{CC} − 1.6	V_{CC} − 1.3 V_{CC} − 1.3		V V
$V_{OOUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	I_O = 500 μA (Digit Outputs) I_O = 360 μA (Conv. Complete, +/−, OFLO Outputs)	V_{CC} − 0.4			V
I_{SOURCE}	Output Source Current (Digit Outputs)	V_{OUT} = 1.0 V	2.0			mA
$I_{INN(1)}$	Logical "1" Input Current (Start Conversion)	V_{IN} = 15 V			1.0	μA
$I_{INN(0)}$	Logical "0" Input Current (Start Conversion)	V_{IN} = 0 V	−1.0			μA
I_{CCC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{INN}	Clock Frequency		100		640	kHz
f_{CC}	Conversion Rate			f_{IN}/129,024		conv./sec
f_{MUX}	Digit Mux Rate			f_{IN}/512		Hz
t_{BBLANK}	Inter Digit Blanking Time			1/(32 f_{MUX})		seconds
t_{SSCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for T_A = 25° C.

Note 3: Full scale = 4000 counts; therefore 0.025% of full scale = 1 count and 0.05% of full scale = 2 counts.

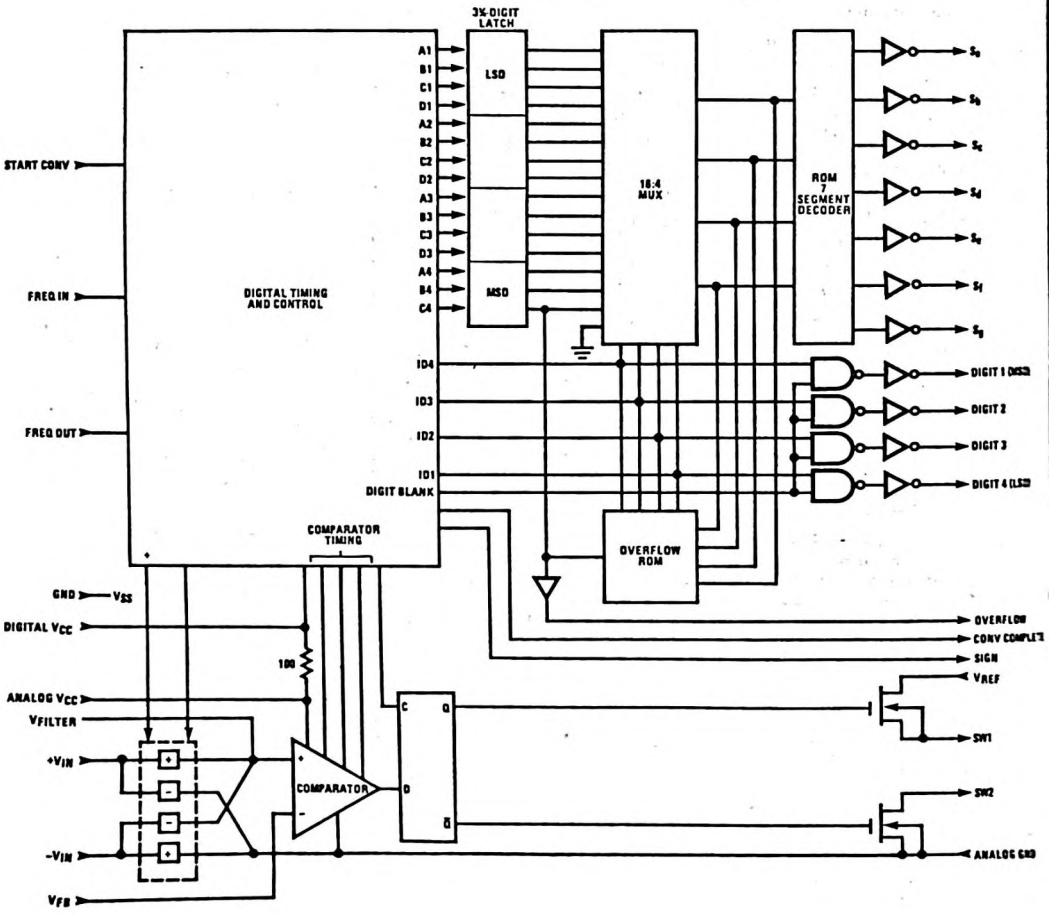
Note 4: For 2.000 Volts full scale, 1 mV = 2 counts.

Electrical Characteristics ADD3701

t_C = 2.5 conversions/second, 0°C ≤ T_A ≤ +70°C, unless otherwise specified.

Parameter	Conditions	Min	Typ[2]	Max	Units
Non-Linearity of Output Reading	V_{IN} = 0–2 V Full Scale V_{IN} = 0–200 mV Full Scale	–0.05	±0.025	+0.05	% full scale (Note 3)
Quantization Error		–1		+0	counts
Offset Error, V_{IN} = 0 V		–0.5	+1.5	+3	mV (Note 3)
Rollover Error		–0		+0	counts
Analog Input Current (V_{IN}+, V_{IN}–)	T_A = 25°C	–5	±1	+5	nA

Block Diagram



ADD3701 3½-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0\,V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0 V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0 V. At this time V_{FB} will start discharging toward 0 V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0 V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\,\frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF}\,(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\,(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\,(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

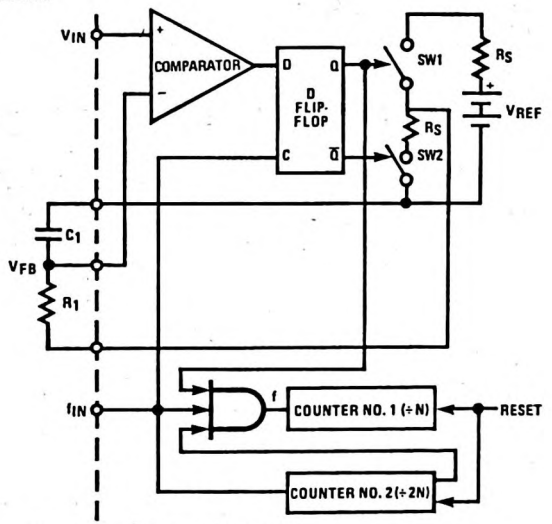
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 129,024 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 128 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3701 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 129,024 x $1/f_{IN}$ and the minimum time is 512 x $1/f_{IN}$.

Timing Waveforms

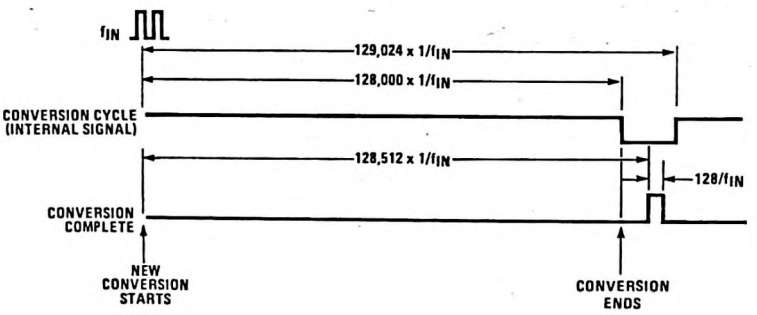


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

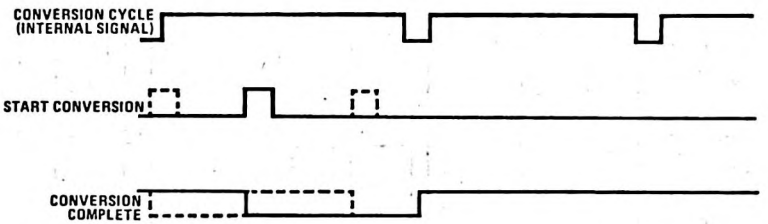


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

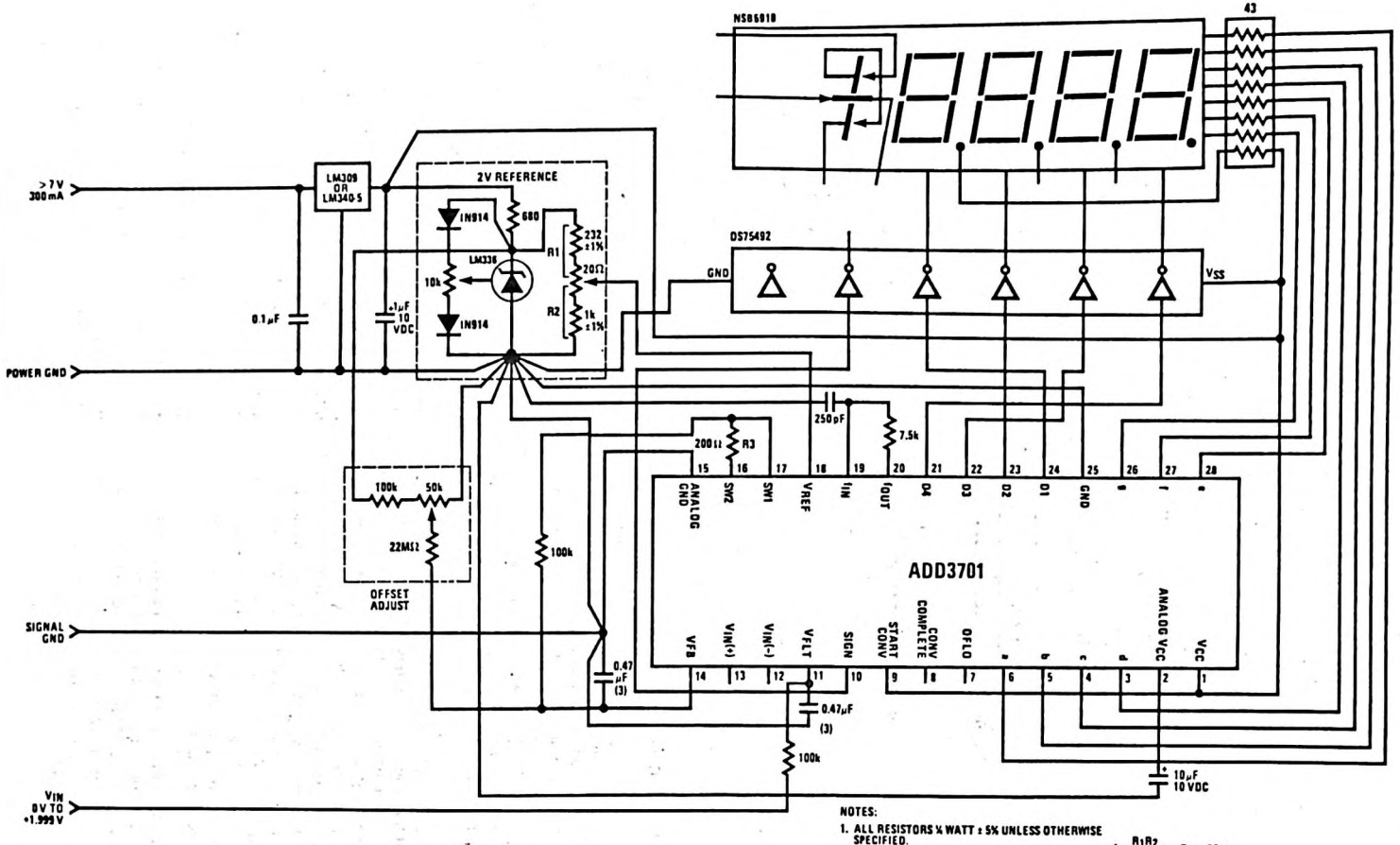
To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators all function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it.

The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 5.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9} A x 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 4. 3½-Digit DPM, +3.999 Count Full Scale

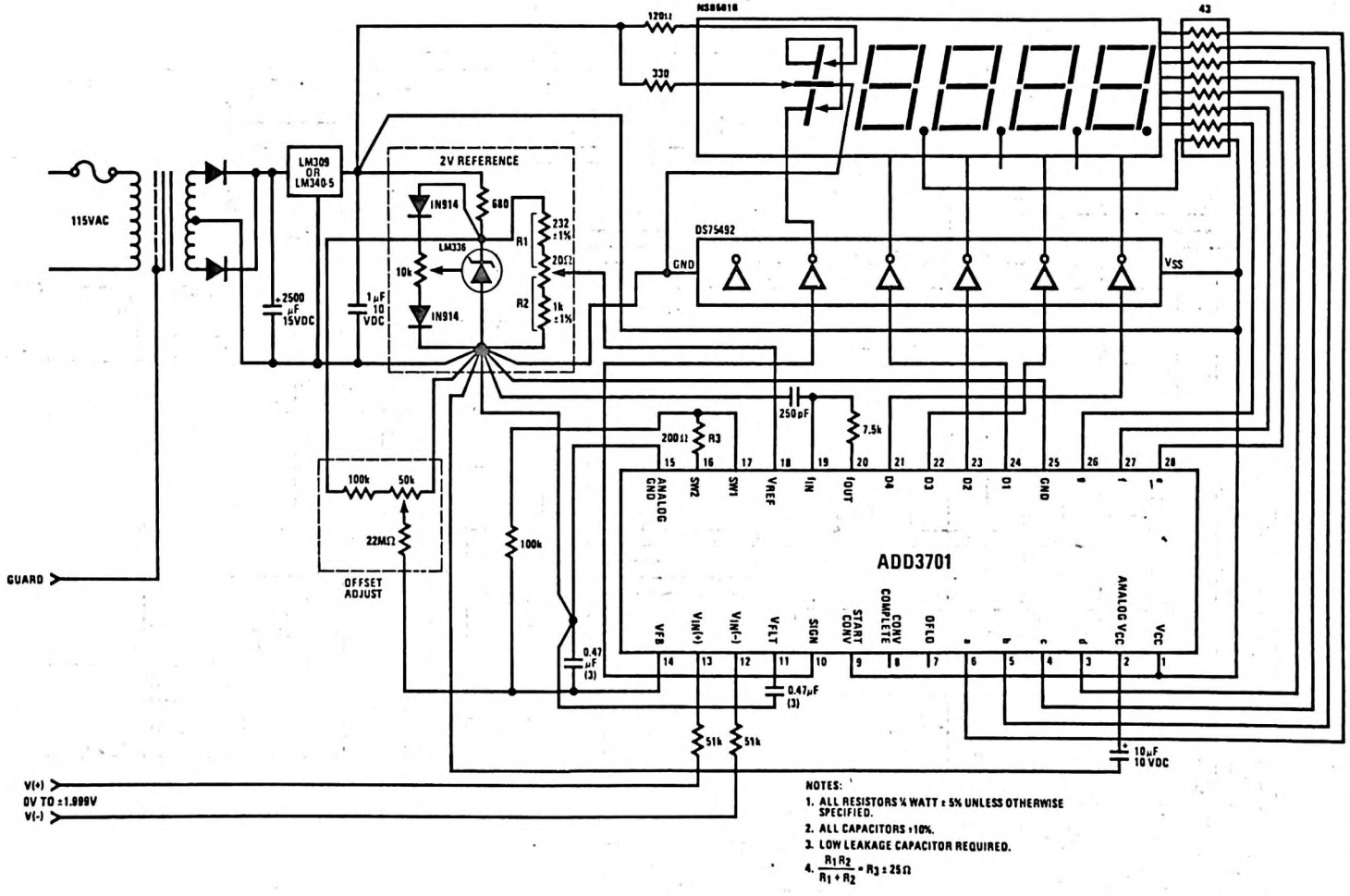


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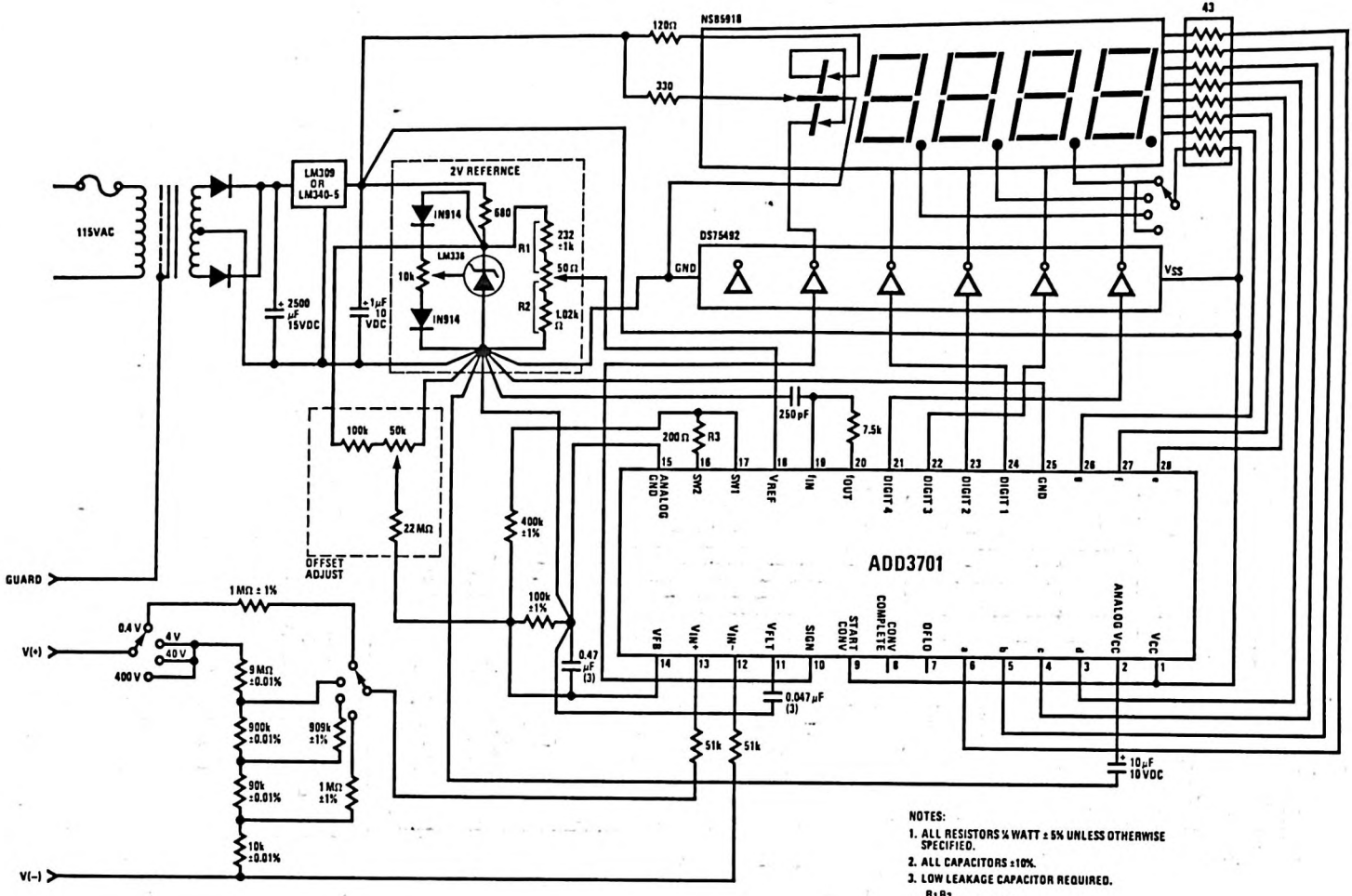
Figure 5. 3½-Digit DPM, ±3.999 Counts Full Scale



NOTES:

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2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$.

Figure 6. 3½-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale

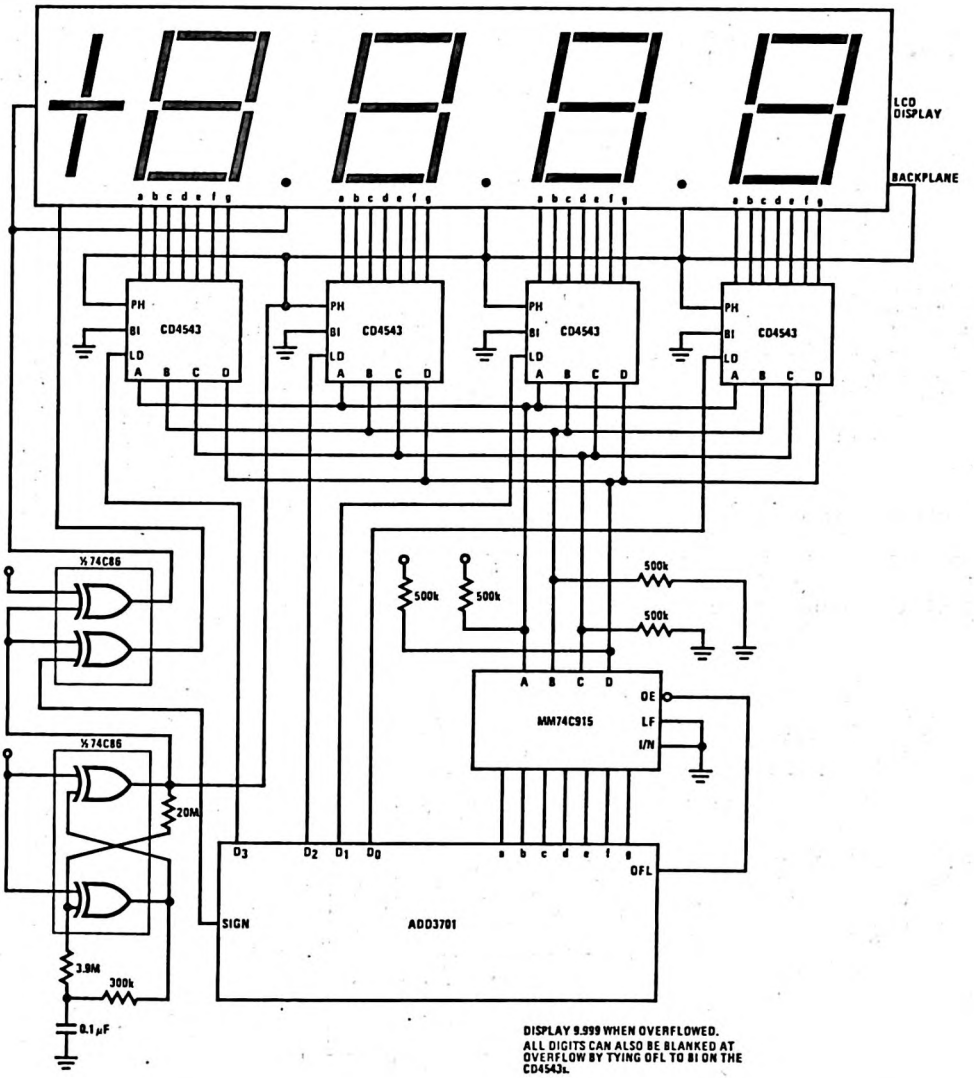
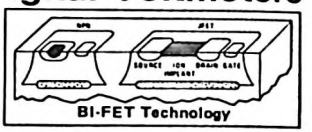


Figure 7. ADD3701 Driving Liquid Crystal Display

National Semiconductor

Digital Voltmeters



LF13300 Integrating A/D Analog Building Block

SEE PAGES 2-57 THRU 2-77 FOR COMPLETE SPECIFICATIONS

General Description

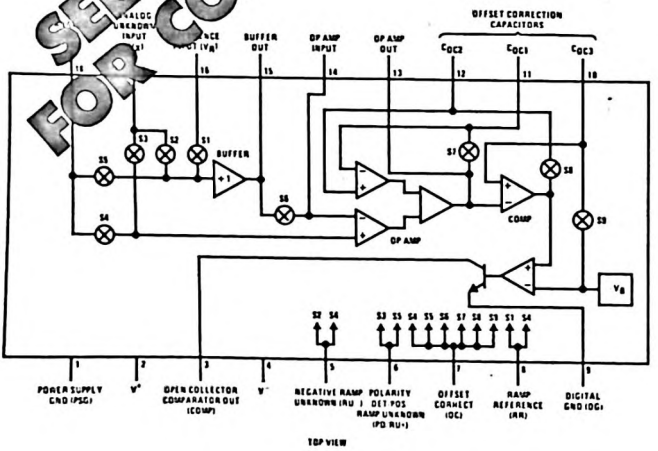
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with either the ADB4511 DPM digital building block or the ADB1200 (MM5863) 12-bit binary building block.

*See ADB1200 (MM5863) data sheet for more information.

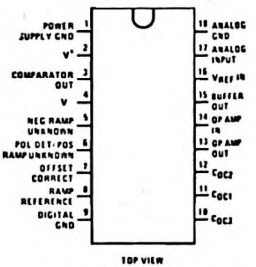
Features

- Rugged JFET inputs blow-out free handling
- High input impedance 10^12Ω typ
- Automatic offset correction
- Analog circuitry can be physically and electrically separated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Easy interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams



Dual-In-Line Package



Order Number LF13300D
See NS Package D18A

Section 6

Voltage References

6

National Semiconductor

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

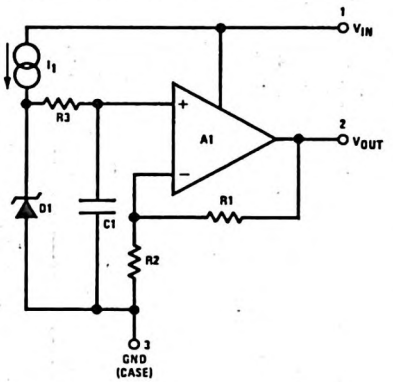
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

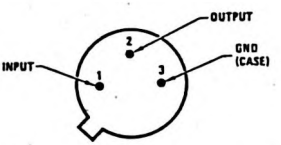
- Accurate output voltage
  - LH0070 — 10V ±0.01%
  - LH0071 — 10.24V ±0.01%
- Single supply operation — 12.5V to 40V
- Low output impedance — 0.1Ω
- Excellent line regulation — 0.1 mV/V
- Low zener noise — 100 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current — 3 mA

Equivalent Schematic



Connection Diagram

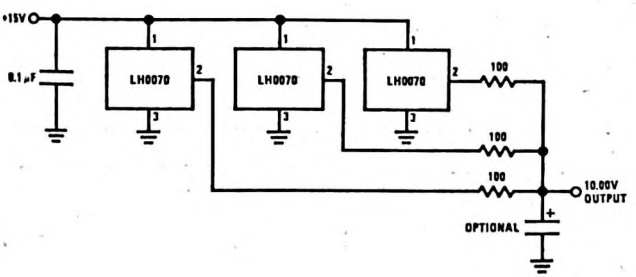
TO-5 Metal Can Package



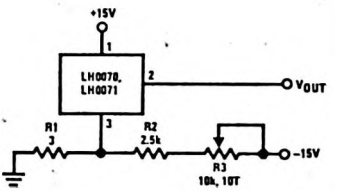
BOTTOM VIEW

Order Number LH0070-0H, LH0071-0H, LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package H03B

Typical Applications



Statistical Voltage Standard



*Note. The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

***Output Voltage Fine Adjustment**

Absolute Maximum Ratings

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	±20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.240		V
Output Accuracy	$T_A = 25°C$				
−0, −1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy					
−0, −1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−0				± 0.2	%
−1			±0.02	± 0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \leq V_{IN} \leq 33V$, $T_C = 25°C$				
−0, −1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range		12.5		40	V
Load Regulation	$0\ mA \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0\ mA$	2	3	5	mA
Change In Quiescent Current	$\Delta V_{IN} = 20V$ From 13V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	1	Ω
Long Term Stability	$T_A = 25°C$, (Note 3)				
−0, −1				±0.2	%/yr
−2				±0.05	%/yr

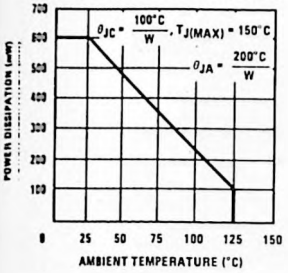
Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

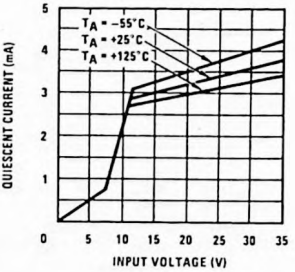
Note 3: This parameter is guaranteed by design and not tested.

Typical Performance Characteristics

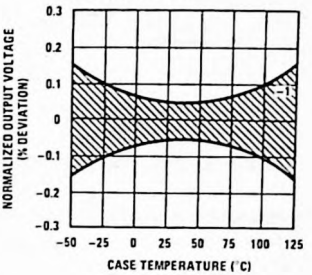
Maximum Power Dissipation



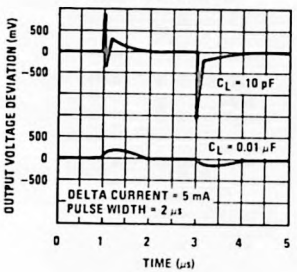
Quiescent Current vs Input Voltage



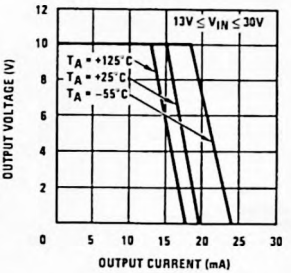
Normalized Output Voltage vs Temperature



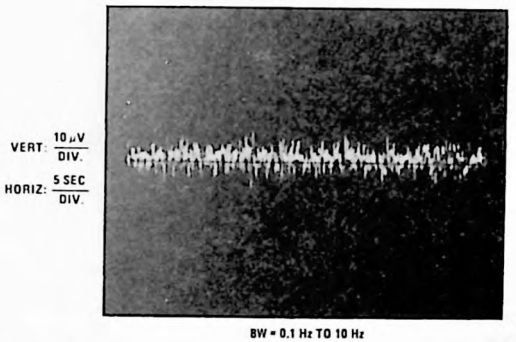
Step Load Response



Output Short Circuit Characteristics

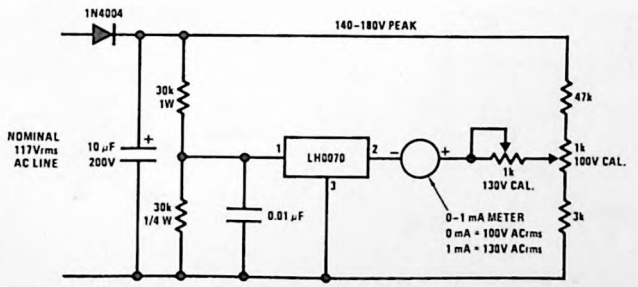


Noise Voltage



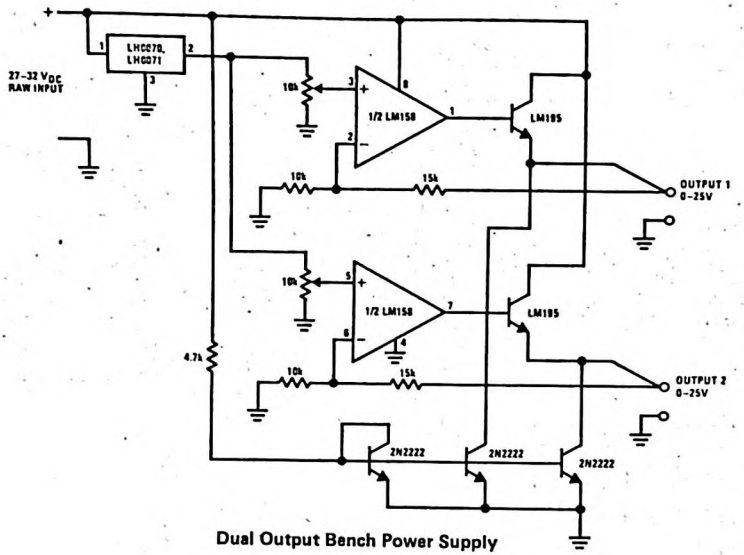
BW = 0.1 Hz TO 10 Hz

Typical Applications (Continued)

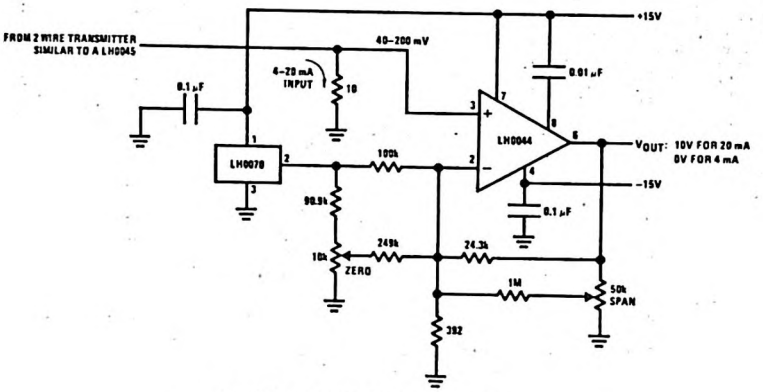


Expanded Scale AC Voltmeter

Typical Applications (Continued)



Dual Output Bench Power Supply



Precision Process Control Interface

National Semiconductor

LM103 Reference Diode**

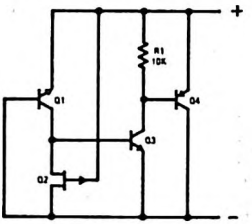
general description

The LM103 is a two-terminal monolithic reference diode electrically equivalent to a breakdown diode. The device makes use of the reverse punch-through of double-diffused transistors, combined with active circuitry, to produce a breakdown characteristic which is ten times sharper than single-junction zener diodes at low voltages. Breakdown voltages from 1.8V to 5.6V are available; and, although the design is optimized for operation between 100 μA and 1 mA, it is completely specified from 10 μA to 10 mA. Noteworthy features of the device are:

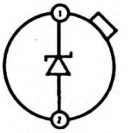
- Exceptionally sharp breakdown
- Low dynamic impedance from 10 μA to 10 mA
- Performance guaranteed over full military temperature range
- Planar, passivated junctions for stable operation
- Low capacitance.

The LM103, packaged in a hermetically sealed, modified TO-46 header is useful in a wide range of circuit applications from level shifting to simple voltage regulation. It can also be employed with operational amplifiers in producing breakpoints to generate nonlinear transfer functions. Finally, its unique characteristics recommend it as a reference element in low voltage power supplies with input voltages down to 4V.

schematic and connection diagrams



Metal Can Package

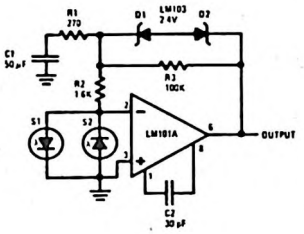


Note: Pin 2 connected to case.
TOP VIEW

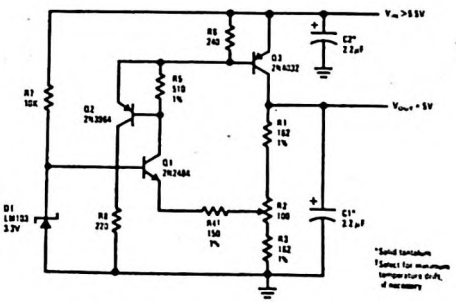
Order Number LM103H
See NS Package H02A

typical applications

Saturating Servo Preamplifier with Rate Feedback



200 mA Positive Regulator



**Covered by U.S. Patent Number 3,571,630

absolute maximum ratings

Power Dissipation (note 1)	250 mW
Reverse Current	20 mA
Forward Current	100 mA
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 60 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Breakdown Voltage Change	$10\,\mu A \leq I_R \leq 100\,\mu A$		60	120	mV
	$100\,\mu A \leq I_R \leq 1$ mA		15	50	mV
	1 mA $\leq I_R \leq 10$ mA		50	150	mV
Reverse Dynamic Impedance (Note 3)	$I_R = 3$ mA		5	25	Ω
	$I_R = 0.3$ mA		15	60	Ω
Reverse Leakage Current	$V_R = V_Z - 0.2V$		2	5	μA
Forward Voltage Drop	$I_F = 10$ mA	0.7	0.8	1.0	V
Peak-to-Peak Broadband Noise Voltage	10 Hz $\leq f \leq 100$ kHz, $I_R = 1$ mA		300		μV
Reverse Breakdown Voltage Change with Current (Note 4)	$10\,\mu A \leq I_R \leq 100\,\mu A$			200	mV
	$100\,\mu A \leq I_R \leq 1$ mA			60	mV
	1 mA $\leq I_R \leq 10$ mA			200	mV
Breakdown Voltage Temperature Coefficient (Note 4)	$100\,\mu A \leq I_R \leq 1$ mA		−5.0		mV/°C

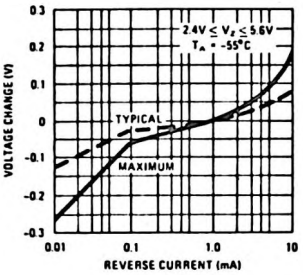
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient (see curve).

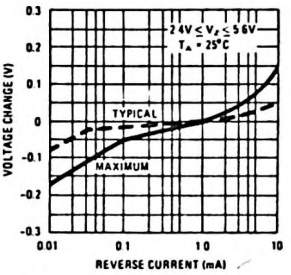
Note 2: These specifications apply for $T_A = 25°C$ and $1.8V < V_Z < 5.6V$ unless stated otherwise. The diode should not be operated with shunt capacitances between 100 pF and 0.01 μF, unless isolated by at least a 300Ω resistor, as it may oscillate at some currents.

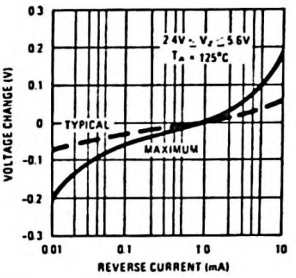
Note 3: Measured with the peak-to peak change of reverse current equal to 10% of the DC reverse current.

Note 4: These specifications apply for $-55°C < T_A < +125°C$.

guaranteed reverse characteristics

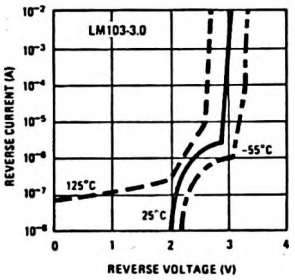




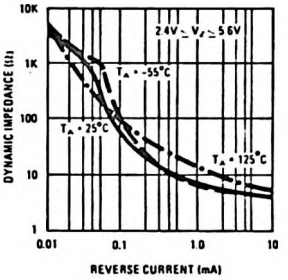


typical performance characteristics

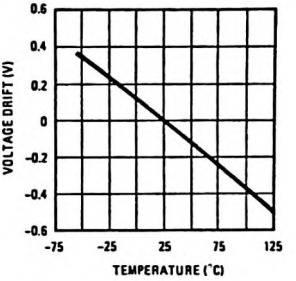
Reverse Characteristics



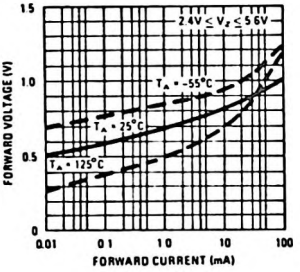
Reverse Dynamic Impedance



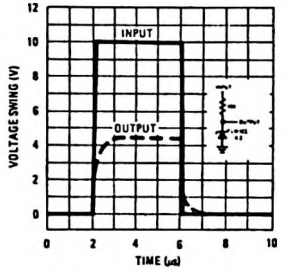
Temperature Drift



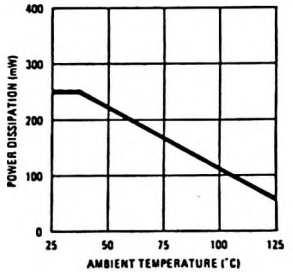
Forward Characteristics



Response Time



Maximum Power Dissipation



BREAKDOWN VOLTAGE*	PART NUMBER
1.8	LM103H-1.8
2.0	LM103H-2.0
2.2	LM103H-2.2
2.4	LM103H-2.4
2.7	LM103H-2.7
3.0	LM103H-3.0
3.3	LM103H-3.3
3.6	LM103H-3.6
3.9	LM103H-3.9
4.3	LM103H-4.3
4.7	LM103H-4.7
5.1	LM103H-5.1
5.6	LM103H-5.6

*Measured at I_R = 1 mA.
Standard tolerance is ±10%.

National Semiconductor

LM113/LM313 Reference Diode

general description

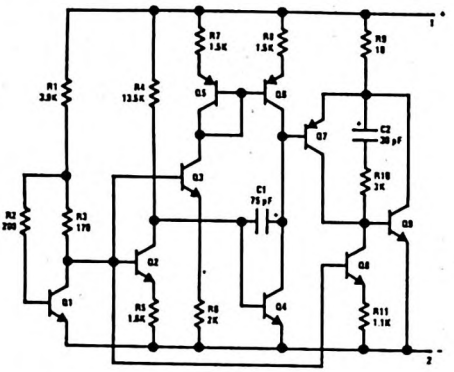
The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances. Outstanding features include:

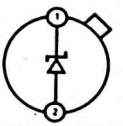
- Low breakdown voltage: 1.220V
- Dynamic impedance of 0.3Ω from 500 μA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5% standard, ±2% and ±1% on special order.

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band-gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

schematic and connection diagrams



Metal Can Package

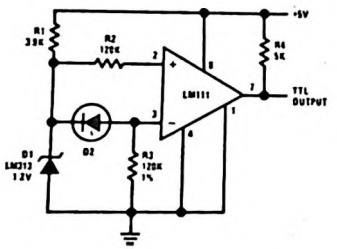


Note: Pin 2 connected to case.
TOP VIEW

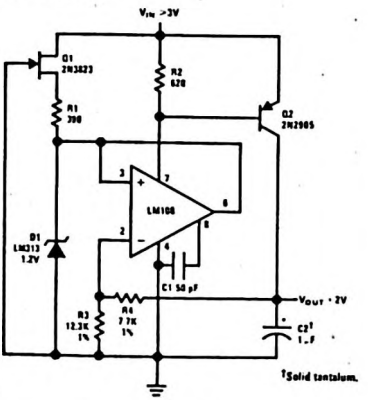
Order Number LM113H or LM313H
See NS Package H02A

typical applications

Level Detector for Photodiode



Low Voltage Regulator



absolute maximum ratings

Power Dissipation (Note 1)	100 mW
Reverse Current	50 mA
Forward Current	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Temperature (T_A)			
LM113	−55	+125	°C
LM313	0	70	°C

electrical characteristics (Note 2)

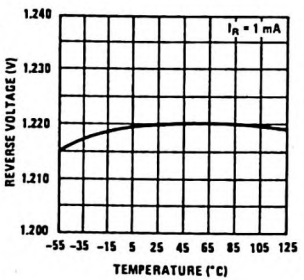
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage					
LM113/LM313	I_R = 1 mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	0.5 mA ≤ I_R ≤ 20 mA		6.0	15	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.2	1.0	Ω
	I_R = 10 mA		0.25	0.8	Ω
Forward Voltage Drop	I_F = 1.0 mA		0.67	1.0	V
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz, I_R = 1 mA		5		μV
Reverse Breakdown Voltage Change with Current	0.5 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}			15	mV
Breakdown Voltage Temperature Coefficient	1.0 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}		0.01		%/°C

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

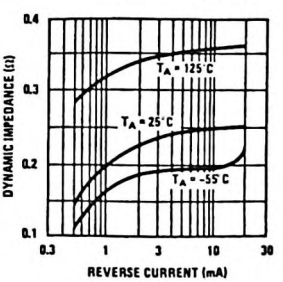
Note 2: These specifications apply for T_A = 25°C, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than 1/4 inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100 Ω resistor, as it may oscillate at some currents.

typical performance characteristics

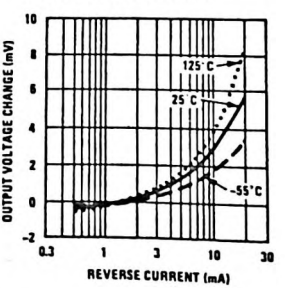
Temperature Drift



Reverse Dynamic Impedance

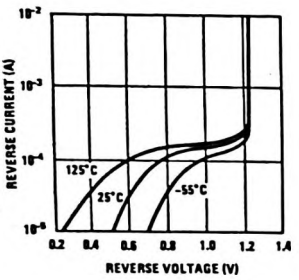


Reverse Characteristics

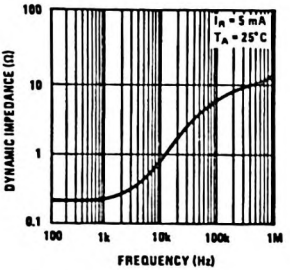


typical performance characteristics (con't)

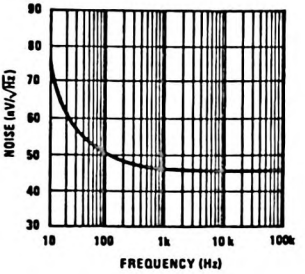
Reverse Characteristics



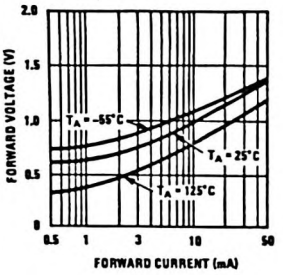
Reverse Dynamic Impedance



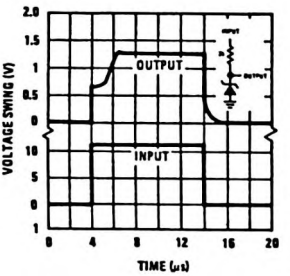
Noise Voltage



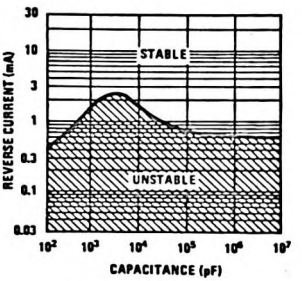
Forward Characteristics



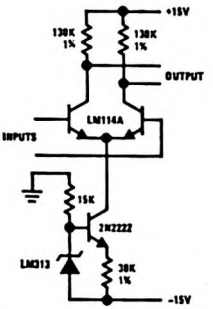
Response Time



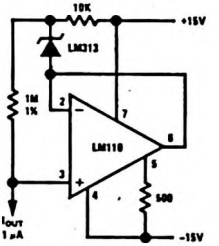
Maximum Shunt Capacitance



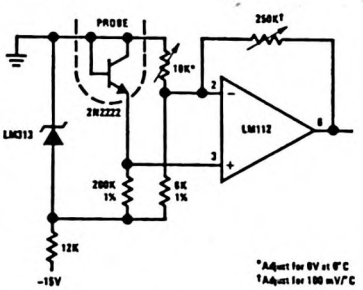
typical applications (con't)



Amplifier Biasing for Constant Gain with Temperature



Constant Current Source



Thermometer

LM129, LM329 Precision Reference

general description

The LM129 and LM329 family are precision multi-current temperature compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shifts in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

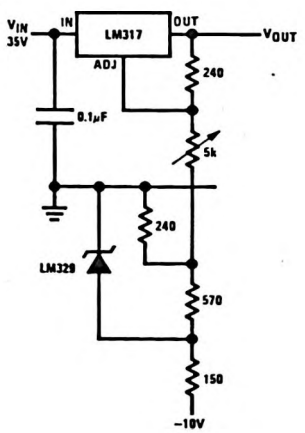
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0—70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

features

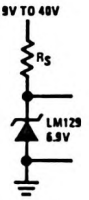
- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

typical applications

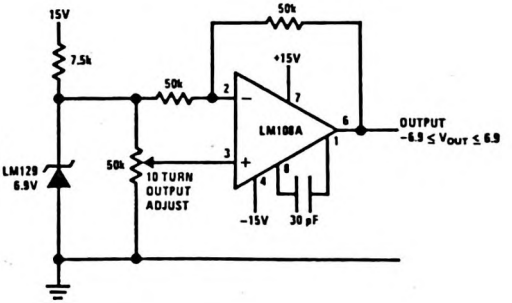
Low Cost 0—25V Regulator



Simple Reference



Adjustable Bipolar Output Reference



absolute maximum ratings

Reverse Breakdown Current	30 mA
Forward Current	2 mA
Operating Temperature Range	
LM129	−55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

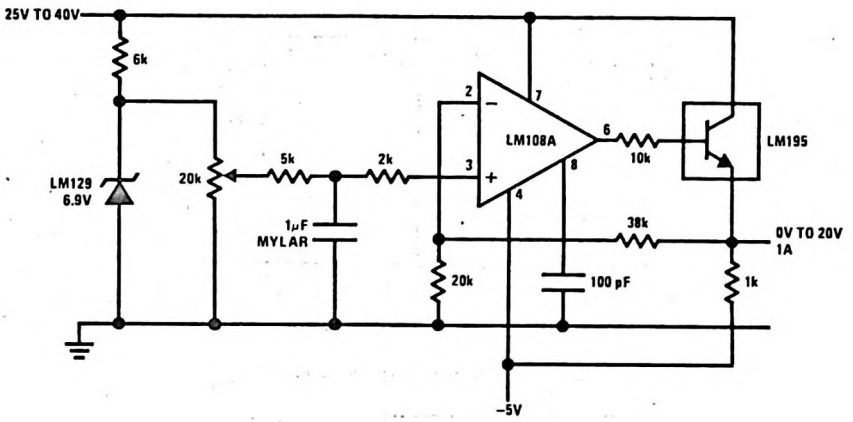
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LM129A, B, C			LM329B, C, D			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \leq F \leq 10\ kHz$		7	20		7	100	μV
Long Term Stability	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A			6	10				ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \leq I_R \leq 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \leq I_R \leq 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \leq I_R \leq 15\ mA$		0.8			1		Ω

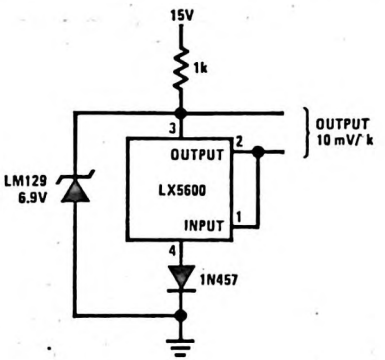
Note 1: These specifications apply for $-55°C \leq T_A \leq +125°C$ for the LM129 and $0°C \leq T_A \leq +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

typical applications (con't)

0V to 20V Power Reference

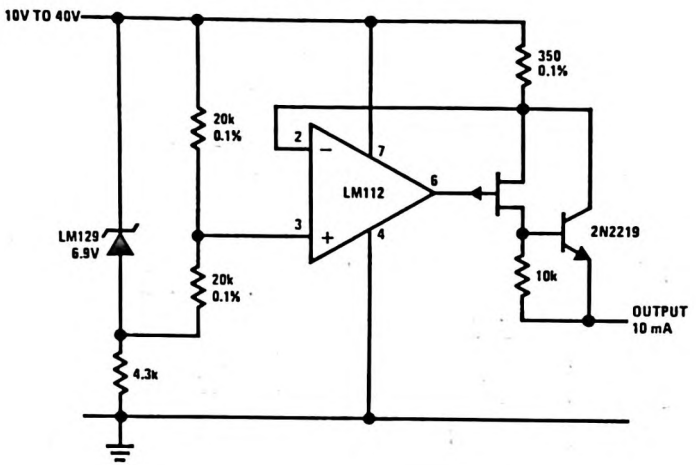


External Reference for Temperature Transducer

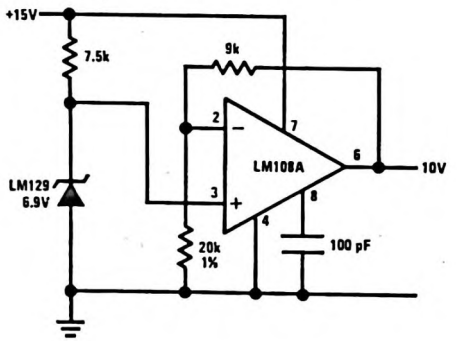


typical applications (con't)

Positive Current Source

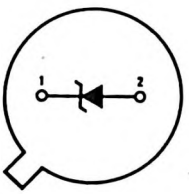


Buffered Reference with Single Supply



connection diagrams

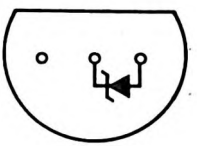
Metal Can Package



BOTTOM VIEW

Order Number LM129AH, LM129BH
LM129CH, LM329BH, LM329CH
or LM329DH
See NS Package H02A

Plastic Package

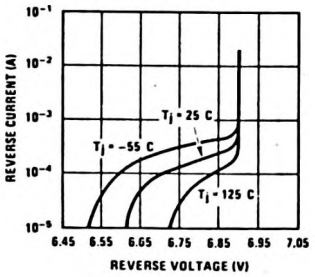


BOTTOM VIEW

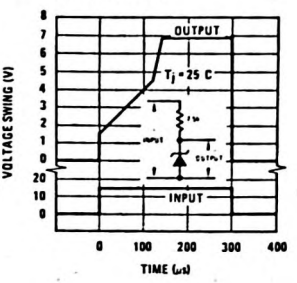
Order Number LM329BZ, LM329CZ
or LM329DZ
See NS Package Z03A

typical performance characteristics

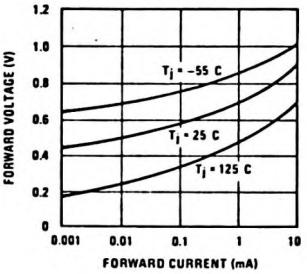
Reverse Characteristics



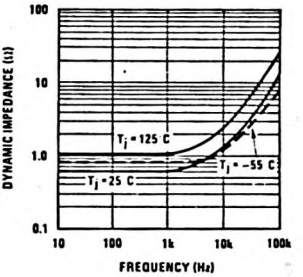
Response Time



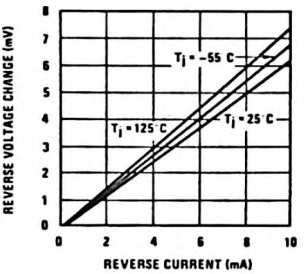
Forward Characteristics



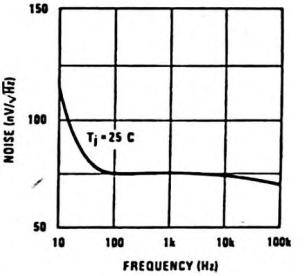
Dynamic Impedance



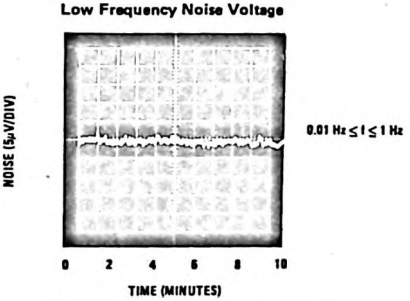
Reverse Voltage Change



Zener Noise Voltage



Low Frequency Noise Voltage



National Semiconductor

LM134/LM234/LM334 3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the new current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

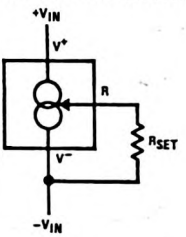
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic and TO-92 plastic packages.

Features

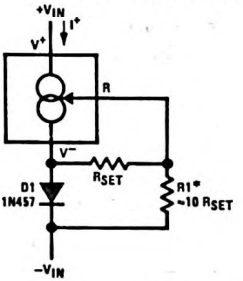
- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Typical Applications

Basic 2-Terminal Current Source

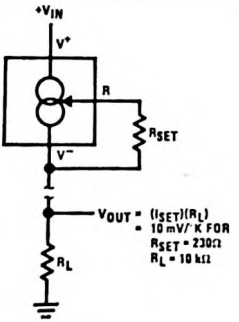


Zero Temperature Coefficient Current Source

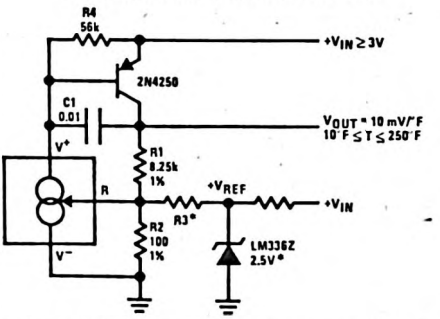


*Select ratio of R1 to R_{SET} to obtain zero drift. $I^+ \approx 2\ I_{SET}$

Terminating Remote Sensor for Voltage Output



Ground Referred Fahrenheit Thermometer



*Select R3 = V_{REF}/583 μA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

Absolute Maximum Ratings

V^+ to V^- Forward Voltage	
LM134/LM234	40V
LM334/LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
SET Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	200 mW
Operating Temperature Range	
LM134/LM134-3/LM134-6	−55°C to +125°C
LM234/LM234-3/LM234-6	−25°C to +100°C
LM334	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM134/LM234			LM334			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$10\,\mu A \le I_{SET} \le 1\,mA$			3			6	%
	$1\,mA < I_{SET} \le 5\,mA$			5			8	%
	$2\,\mu A \le I_{SET} < 10\,\mu A$			5			8	%
Ratio of Set Current to V^- Current	$10\,\mu A \le I_{SET} \le 1\,mA$	14	18	23	14	18	26	
	$1\,mA \le I_{SET} \le 5\,mA$		14			14		
	$2\,\mu A \le I_{SET} \le 10\,\mu A$	14	18	23	14	18	26	
Minimum Operating Voltage	$2\,\mu A \le I_{SET} \le 100\,\mu A$		0.8			0.8		V
	$100\,\mu A < I_{SET} \le 1\,mA$		0.9			0.9		V
	$1\,mA < I_{SET} \le 5\,mA$		1.0			1.0		V
Average Change in Set Current with Input Voltage	$1.5 \le V^+ \le 5V$		0.02	0.05		0.02	0.1	%/V
	$2\,\mu A \le I_{SET} \le 1\,mA$							
	$5V \le V^+ \le 40V$		0.01	0.03		0.01	0.05	%/V
	$1.5V \le V \le 5V$		0.03			0.03		%/V
	$1\,mA < I_{SET} \le 5\,mA$							
	$5V \le V \le 40V$		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	$25\,\mu A \le I_{SET} \le 1\,mA$	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7\,mV/R_{SET}$ (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ $T_j = 25°C$.

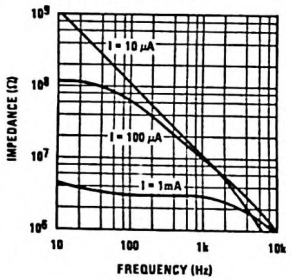
Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o\,(T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Electrical Characteristics (Continued) (Note 1)

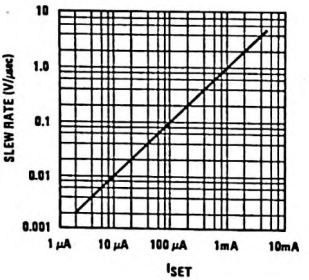
PARAMETER	CONDITIONS	LM134-3, LM234-3			LM134-6, LM234-6			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $T_j = 25°C$			±1			±2	%
Equivalent Temperature Error				±3			±6	°C
Ratio of Set Current to V^- Current	$100\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \leq 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$1.5 \leq V^+ \leq 5V$		0.02	0.05		0.02	0.1	%/V
	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $5V \leq V^+ \leq 30V$		0.01	0.03		0.01	0.05	%/V
Temperature Dependence of Set Current (Note 3) and Equivalent Slope Error	$100\ \mu A \leq I_{SET} \leq 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
				±2			±3	%
Effective Shunt Capacitance			15			15		pF

Typical Performance Characteristics

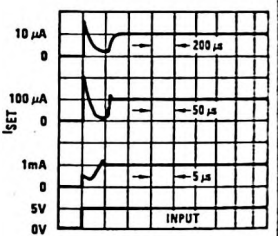
Output Impedance



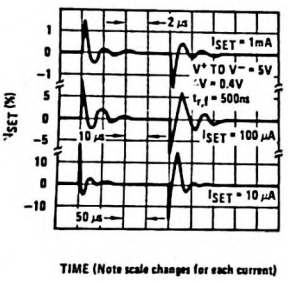
Maximum Slew Rate for Linear Operation



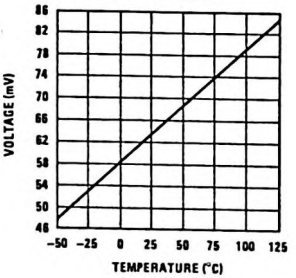
Start-Up



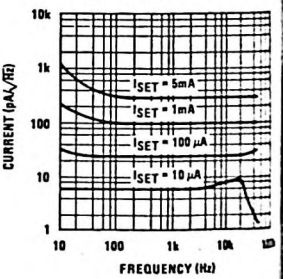
Transient Response



Voltage Across R_{SET}

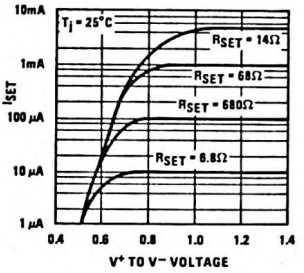


Current Noise

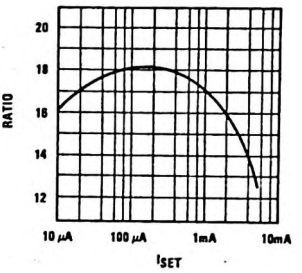


Typical Performance Characteristics (Continued)

Turn-On Voltage



Ratio of I_{SET} to V⁻ Current



Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10 μA, maximum dV/dt is 0.01V/μs; at I_{SET} = 1 mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at I_{SET} = 1 mA will increase junction temperature by ≈ 0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4)(0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

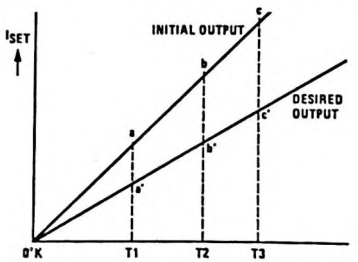
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/^{\circ}K)(T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before

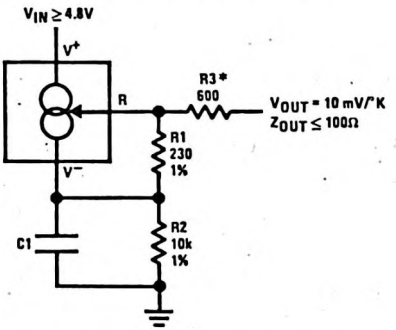
Application Hints (Continued)

trimming. Line a'b'c' is the desired output. A gain trim done at T2 will move the output from b to b' and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

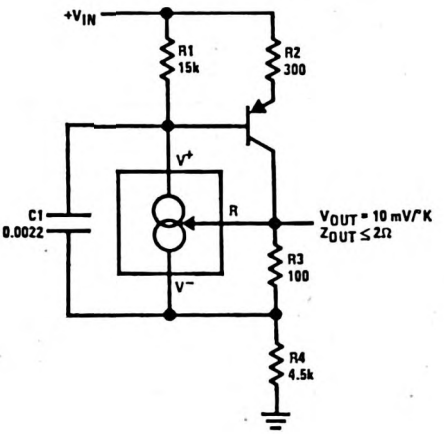
Typical Applications (Continued)

Low Output Impedance Thermometer

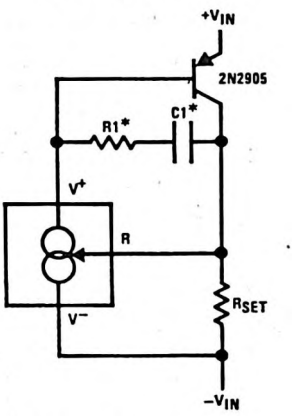


*Output impedance of the LM134 at the "R" pin is approximately $-R_O/16\Omega$, where R_O is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output.

Low Output Impedance Thermometer



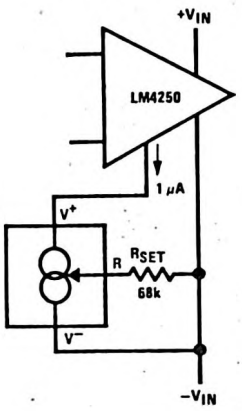
Higher Output Current



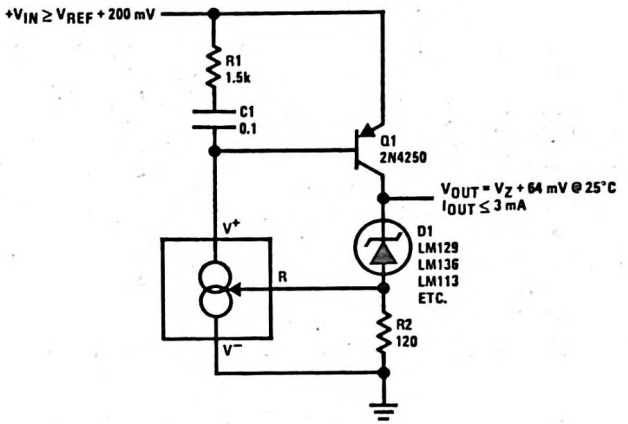
*Select R1 and C1 for optimum stability

Typical Applications (Continued)

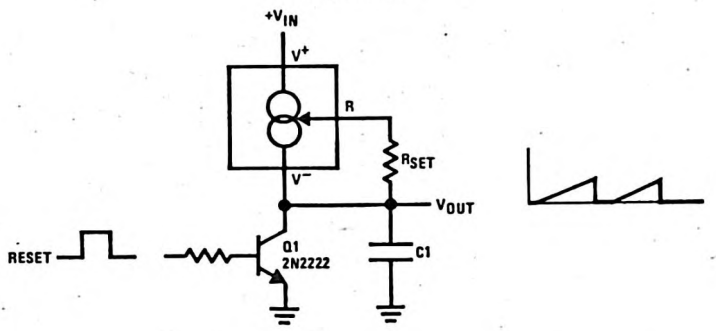
Micropower Bias



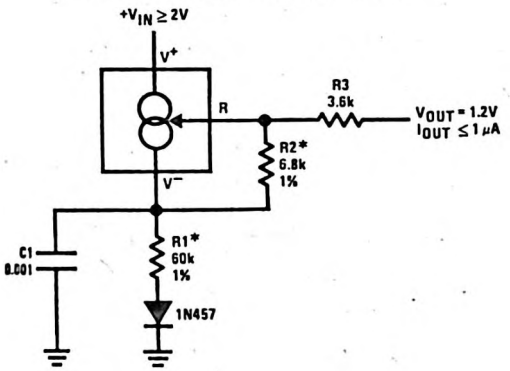
Low Input Voltage Reference Driver



Ramp Generator

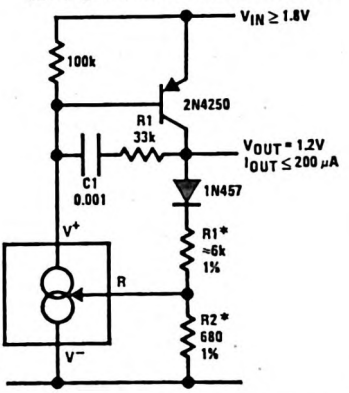


1.2V Reference Operates on 10 μA and 2V



*Select ratio of R1 to R2 to obtain zero temperature drift

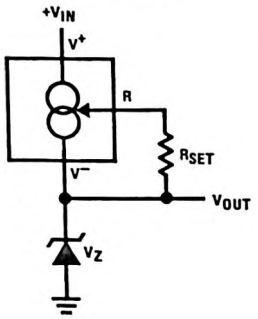
1.2V Regulator with 1.8V Minimum Input



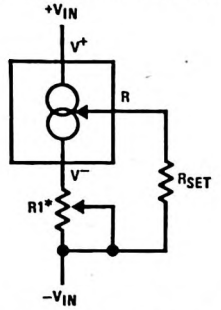
*Select ratio of R1 to R2 for zero temperature drift

Typical Applications (Continued)

Zener Biasing

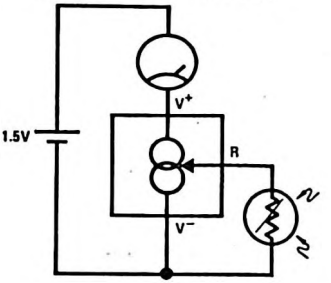


Alternate Trimming Technique

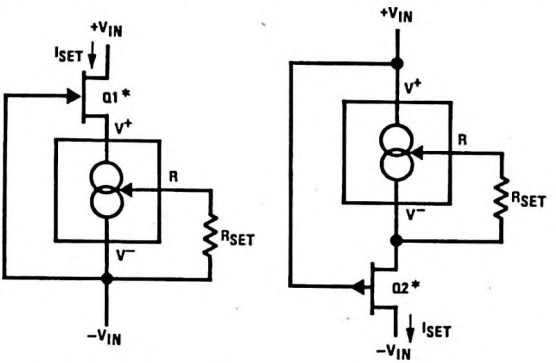


*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

Buffer for Photoconductive Cell

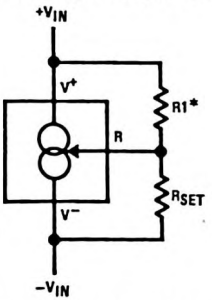


FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



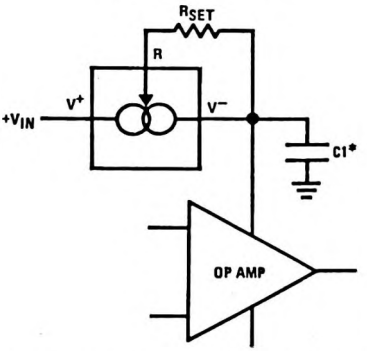
*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_P\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

Generating Negative Output Impedance



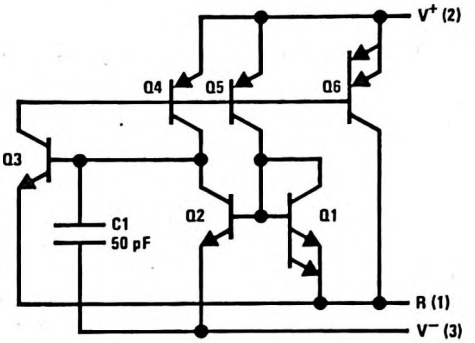
*$Z_{OUT} \approx -16 \cdot R1$ ($R1/V_{IN}$ must not exceed I_{SET})

In-Line Current Limiter

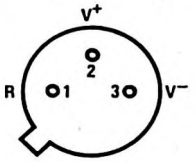


*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Schematic and Connection Diagrams



TO-46
Metal Can Package



BOTTOM VIEW

Pin 3 is electrically connected to case

Order Number LM134H, LM134H-3, LM134H-6, LM234H, LM234H-3, LM234H-6 or LM334H
See NS Package H03H

TO-92
Plastic Package

BOTTOM VIEW

Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Z03A

National Semiconductor

LM136/LM236/LM336 2.5V Reference Diode

General Description

The LM136/LM236 and LM336 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136 allows the reference voltage and temperature coefficient to be trimmed easily.

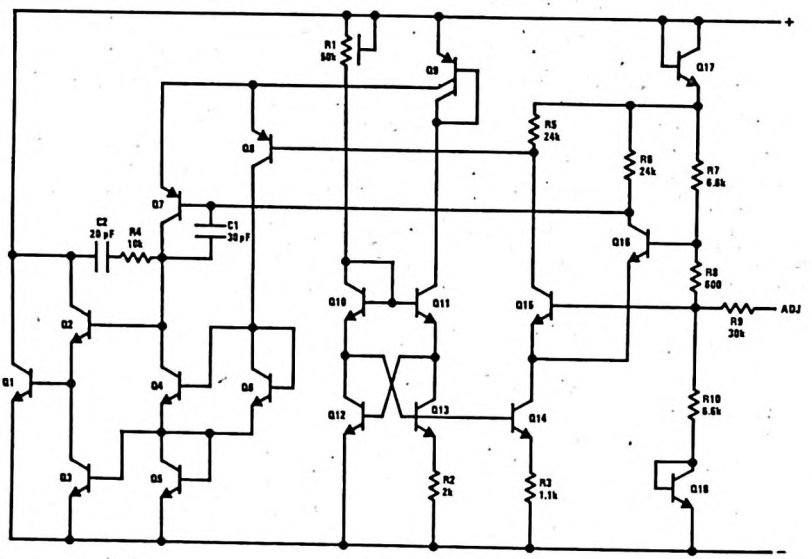
The LM136 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136 is rated for operation over −55°C to +125°C while the LM236 is rated over a −25°C to +85°C temperature range. Both are packaged in a TO-46 package. The LM336 is rated for operation over a 0°C to +70°C temperature range and is available in either a three lead TO-46 package or a TO-92 plastic package.

Features

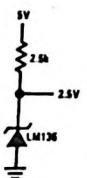
- Low temperature coefficient
- Wide operating current of 300 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package
- 5.0V device also available—LM336–5.0

Schematic Diagram

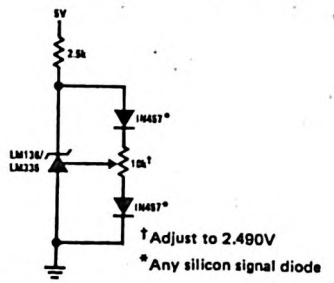


Typical Applications

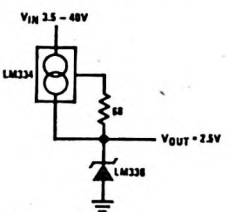
2.5V Reference



2.5V Reference with Minimum Temperature Coefficient



Wide Input Range Reference



Absolute Maximum Ratings

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	−60°C to +150°C
Operating Temperature	
LM136	−55°C to +150°C
LM236	−25°C to +85°C
LM336	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

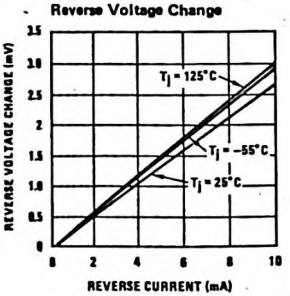
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM136A/LM236A LM136/LM236			LM336B LM336			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136/LM236/LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A/LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25°C$, $400\ \mu A \leq I_R \leq 10$ mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA		0.2	0.6		0.2	1	Ω
Temperature Stability	V_R Adjusted to 2.490V, $I_R = 1$ mA, *(Figure 2)*							
	$0°C \leq T_A \leq 70°C$ (LM336)					1.8	6	mV
	$-25°C \leq T_A \leq +85°C$ (LM236)		3.5	9				mV
	$-55°C \leq T_A \leq +125°C$ (LM136)		12	18				mV
Reverse Breakdown Change With Current	$400\ \mu A \leq I_R \leq 10$ mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA		20			20		ppm

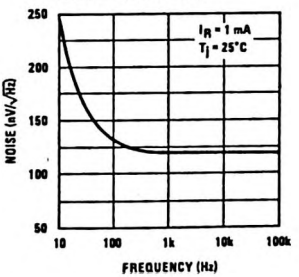
Note 1: Unless otherwise specified, the LM136 is specified from $-55°C \leq T_A \leq +125°C$, the LM236 from $-25°C \leq T_A \leq +85°C$ and the LM336 from $0°C \leq T_A \leq +70°C$. The maximum junction temperature of the LM136 is 150°C, LM236 is 125°C and the LM336 is 100°C. For elevated junction temperature, devices in the TO-46 package should be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Typical Performance Characteristics

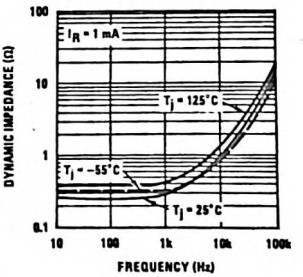
Reverse Voltage Change



Zener Noise Voltage

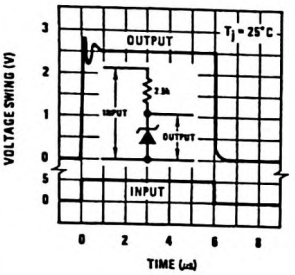


Dynamic Impedance

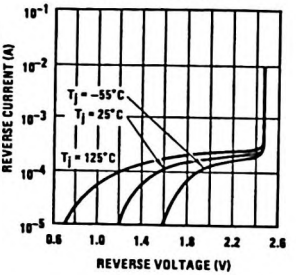


Typical Performance Characteristics (Continued)

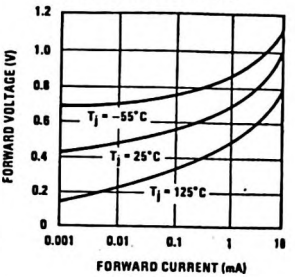
Response Time



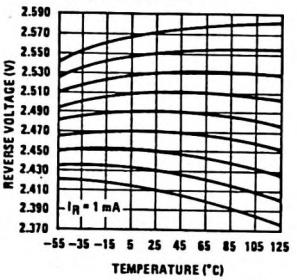
Reverse Characteristics



Forward Characteristics



Temperature Drift



Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

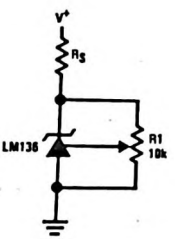


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage

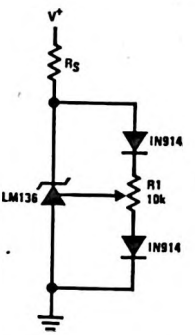
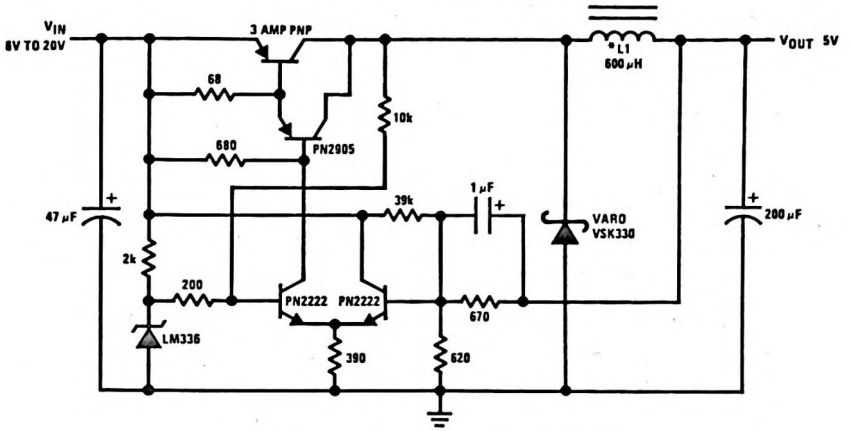


FIGURE 2. Temperature Coefficient Adjustment

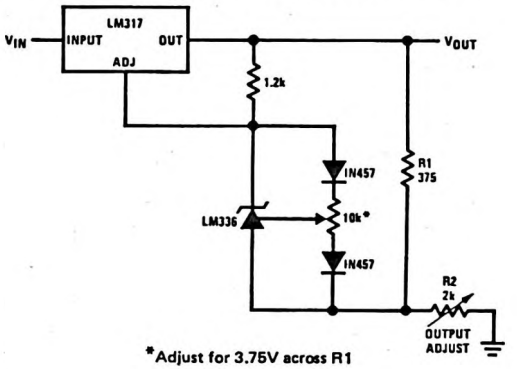
Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator†



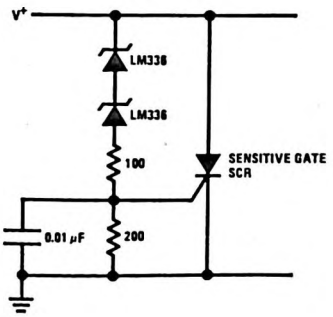
*L1 60 turns #16 wire on Arnold Core A-254168-2
†Efficiency ≈ 80%

Precision Power Regulator with Low Temperature Coefficient

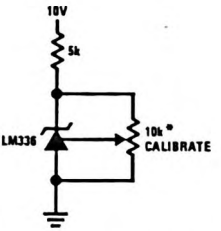


*Adjust for 3.75V across R1

5V Crowbar



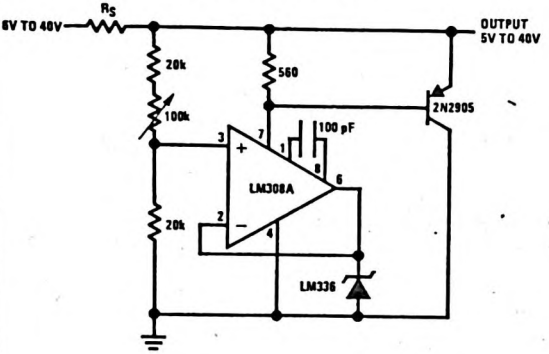
Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage



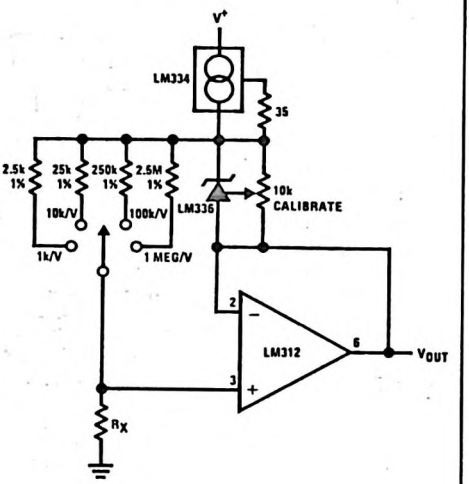
*Does not affect temperature coefficient

Typical Applications (Continued)

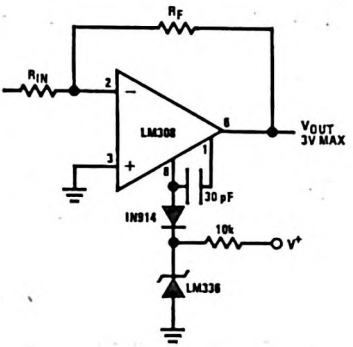
Adjustable Shunt Regulator



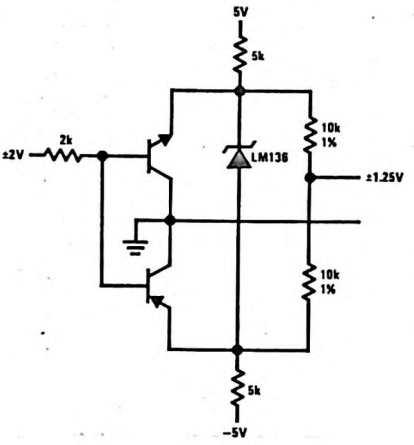
Linear Ohmmeter



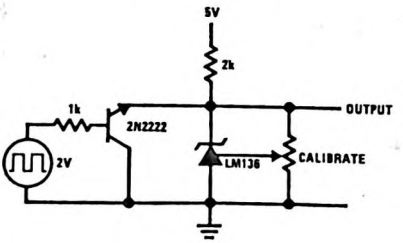
Op Amp with Output Clamped



Bipolar Output Reference

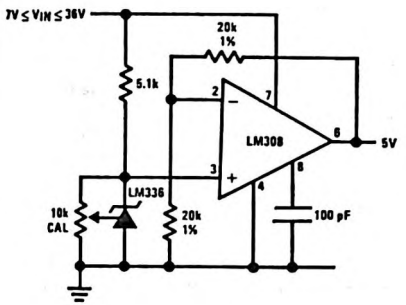


2.5V Square Wave Calibrator

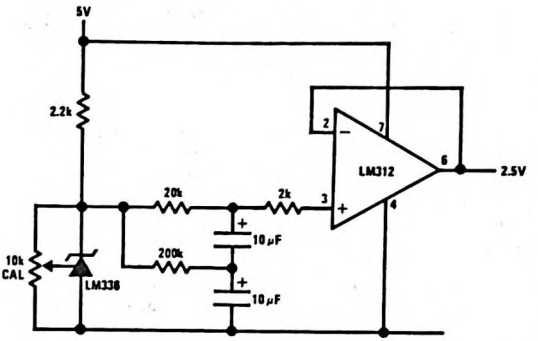


Typical Applications (Continued)

5V Buffered Reference

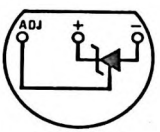


Low Noise Buffered Reference



Connection Diagrams

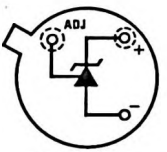
TO-92
Plastic Package



BOTTOM VIEW

Order Number
LM336Z or LM336BZ
See NS Package Z03A

TO-46
Metal Can Package



BOTTOM VIEW

Order Number
LM136H, LM236H, LM336H, LM136AH,
LM236AH or LM336BH
See NS Package H03B

National Semiconductor

LM199/LM299/LM399 Precision Reference

general description

The LM199/LM299/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

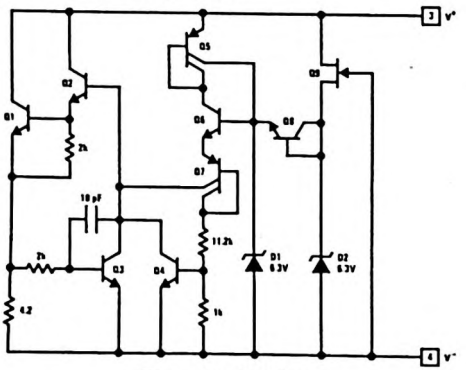
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

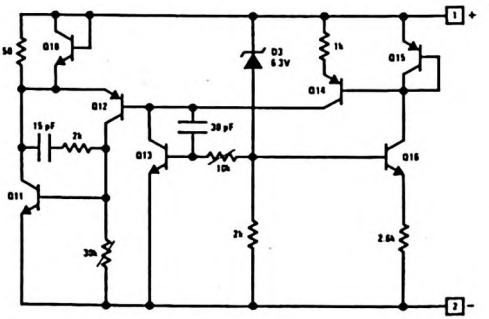
features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm

schematic diagrams



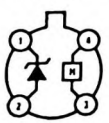
Temperature Stabilizer



Reference

connection diagram

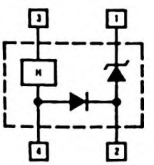
Metal Can Package



TOP VIEW

Order Number LM199H, LM299H or LM399H
See NS Package H04A or H04D

functional block diagram



absolute maximum ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		LM199/LM299			LM399			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \le I \le 10\ mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°C$ $85°C \le T_A \le 125°C$	LM199		0.00003 0.0005	0.0001 0.0015				%/°C %/°C
	$-25°C \le T_A \le 85°C$ $0°C \le T_A \le 70°C$	LM299 LM399		0.00003	0.0001		0.00003	0.0002	%/°C %/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$ $T_A = -55°C$			8.5 22	14 28		8.5	15	mA
Temperature Stabilizer Supply Voltage	(Note 3)		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$, (Note 3)			140	200		140	200	mA

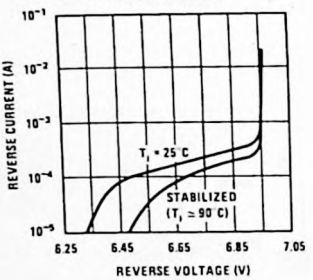
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199; $-25°C \le T_A \le +85°C$ for the LM299 and $0°C \le T_A \le +70°C$ for the LM399.

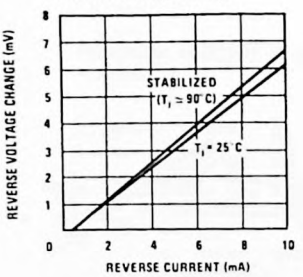
Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

typical performance characteristics

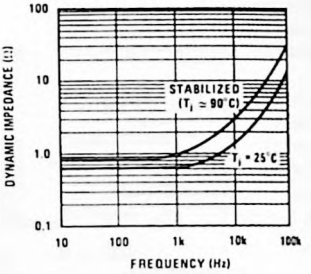
Reverse Characteristics



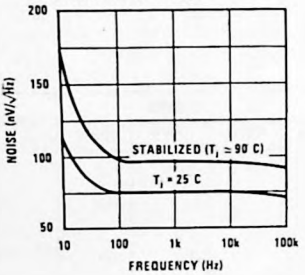
Reverse Voltage Change



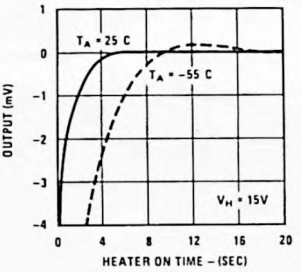
Dynamic Impedance



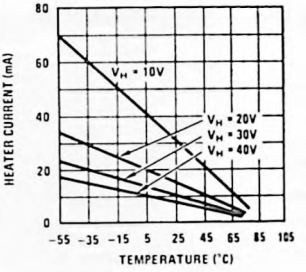
Zener Noise Voltage



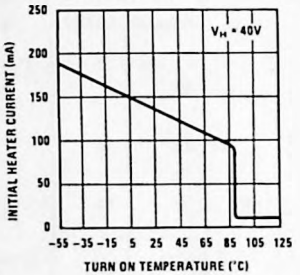
Stabilization Time



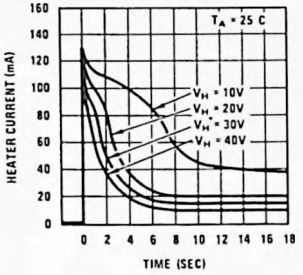
Heater Current



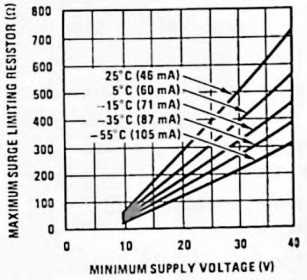
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

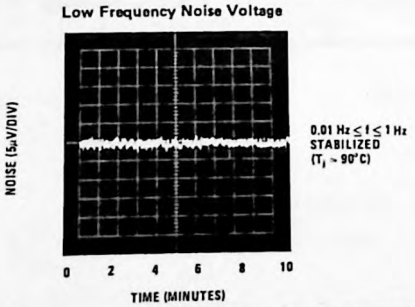


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

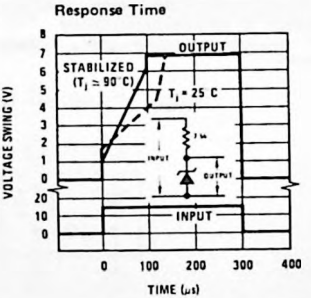


*Heater must be bypassed with a 2 μF or larger tantalum capacitor if maximum value resistors are used. Otherwise, 30% to 50% smaller values must be used. If heater oscillates, resistor value may be too small.

Low Frequency Noise Voltage

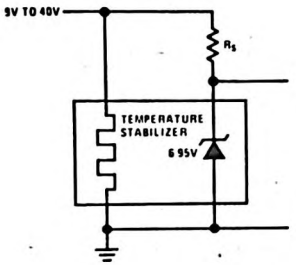


Response Time

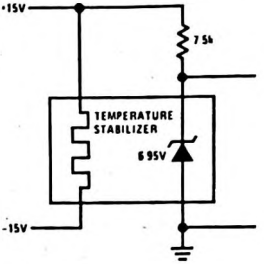


typical applications

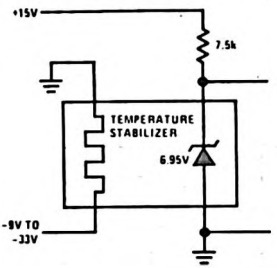
Single Supply Operation



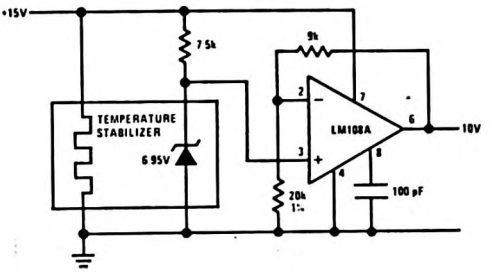
Split Supply Operation



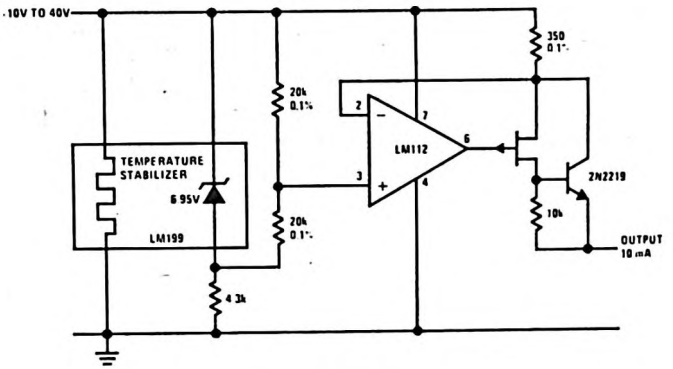
Negative Heater Supply with Positive Reference



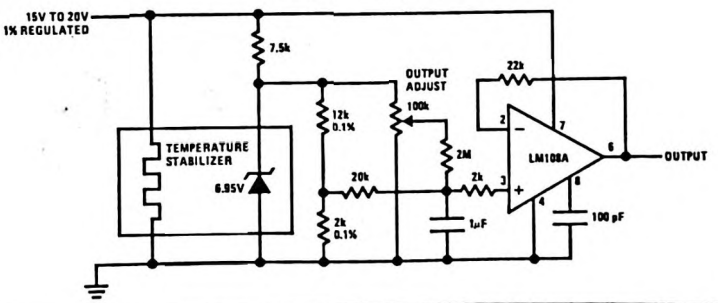
Buffered Reference With Single Supply



Positive Current Source

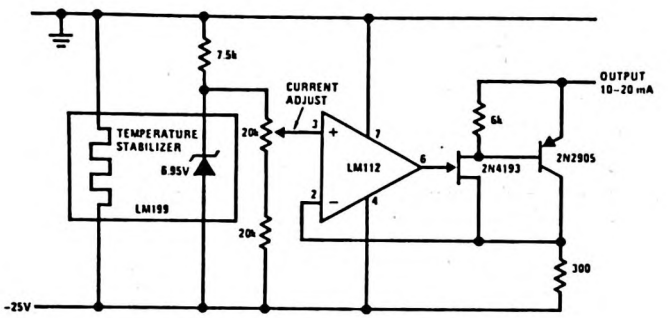


Standard Cell Replacement

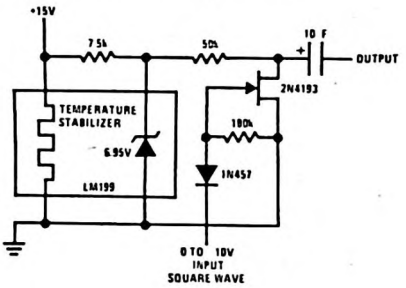


typical applications (con't)

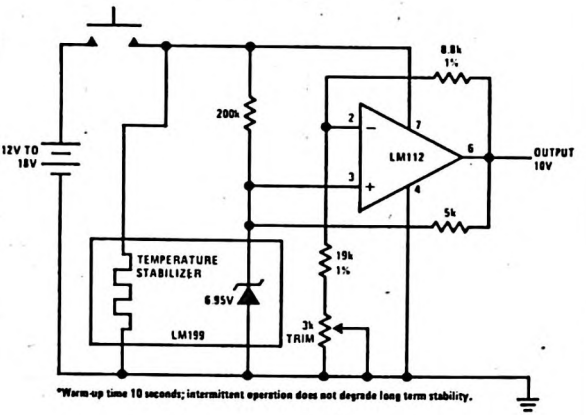
Negative Current Source



Square Wave Voltage Reference

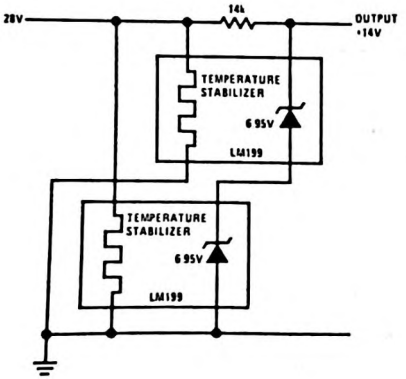


Portable Calibrator*

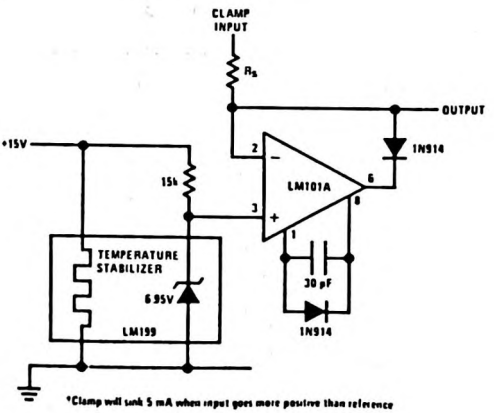


*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

14V Reference



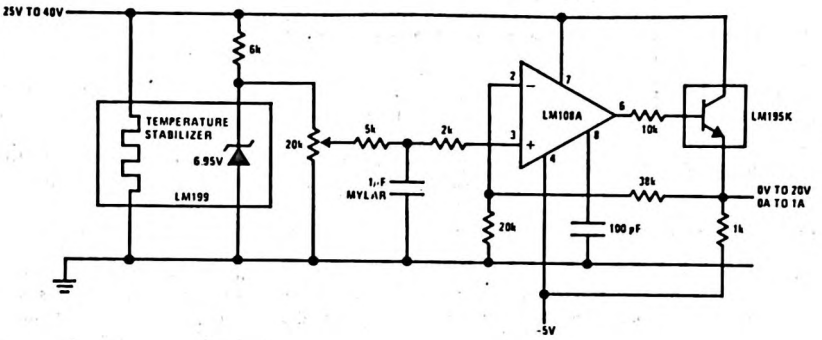
Precision Clamp*



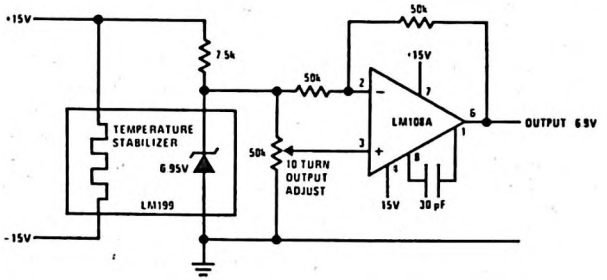
*Clamp will sink 5 mA when input goes more positive than reference

typical applications (con't)

0V to 20V Power Reference



Bipolar Output Reference



National Semiconductor

LM199A/LM299A/LM399A Precision Reference

general description

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299A is rated for operation from −25°C to +85°C and the LM399A is rated from 0°C to +70°C.

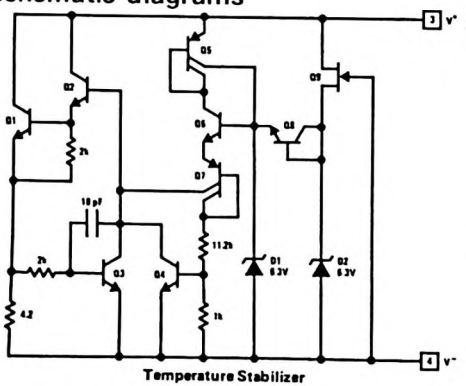
Certified Long Term Stability Devices

All devices are tested for 1000 hours minimum at 25°C ambient temperature with temperature stabilizer operating. All devices shipped with long term data which certifies a maximum drift for the 1000 hours of 20 ppm or 50 ppm.

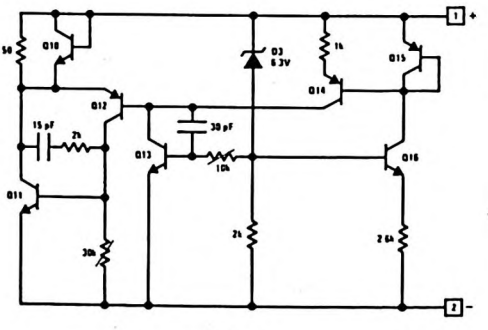
features

- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Certified long term stability available

schematic diagrams



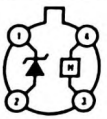
Temperature Stabilizer



Reference

connection diagram

Metal Can Package



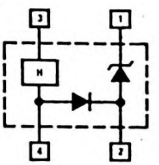
TOP VIEW

Order Number LM199AH, LM299AH or LM399AH
See NS Package H04A or H04D

Certified Long Term Stability Device

CERTIFIED LONG TERM STABILITY ppm MAX	ORDERING NUMBERS
20	LM199AH-20
20	LM299AH-20
50	LM399AH-50

functional block diagram



absolute maximum ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V −0.1V
Operating Temperature Range	
LM199A	−55°C to +125°C
LM299A	−25°C to +85°C
LM399A	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	LM199A, LM299A			LM399A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \le I_R \le 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°C$, LM199A		0.00002	0.00005				%/°C
	$85°C \le T_A \le 125°C$, LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$, LM299A		0.00002	0.0005				%/°C
	$0°C \le T_A \le 70°C$, LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = -55°C$		22	28				
Temperature Stabilizer Supply Voltage (Note 3)		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		Seconds
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$, (Note 3)		140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199A; $-25°C \le T_A \le +85°C$ for the LM299A and $0°C \le T_A \le +70°C$ for the LM399A.

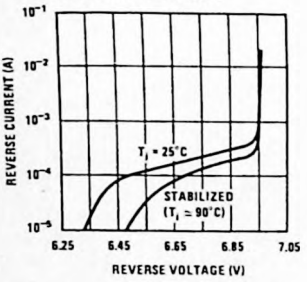
Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

typical applications

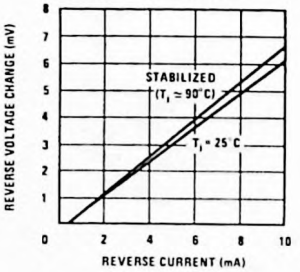
For typical applications, see LM199 data sheet on preceeding pages.

typical performance characteristics

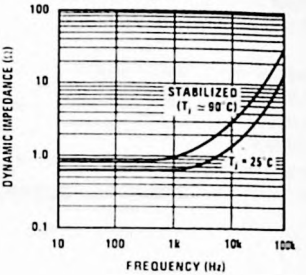
Reverse Characteristics



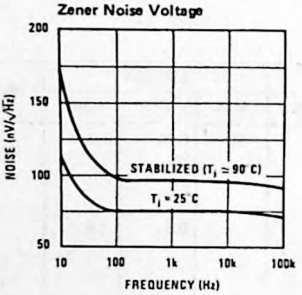
Reverse Voltage Change



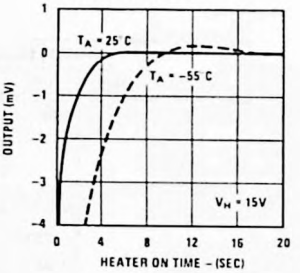
Dynamic Impedance



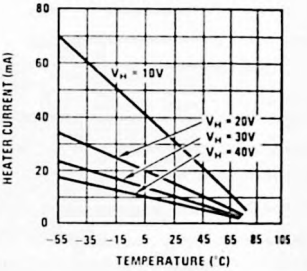
Zener Noise Voltage



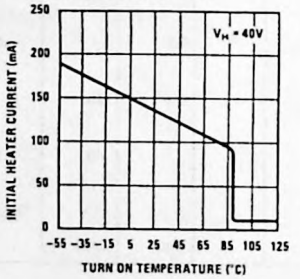
Stabilization Time



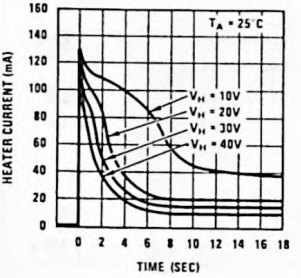
Heater Current



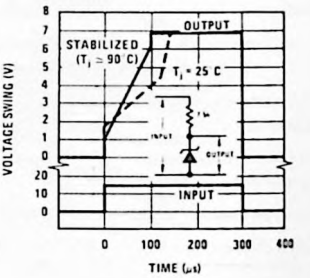
Initial Heater Current



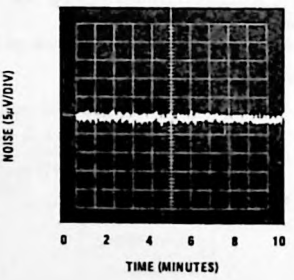
Heater Current



Response Time



Low Frequency Noise Voltage



0.01 Hz ≤ f ≤ 1 Hz
STABILIZED
($T_j \simeq 90°C$)

National Semiconductor

LM3999 Precision Reference

general description

The LM3999 is a precision, temperature-stabilized monolithic zener offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners.

The LM3999 reference is exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM3999 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

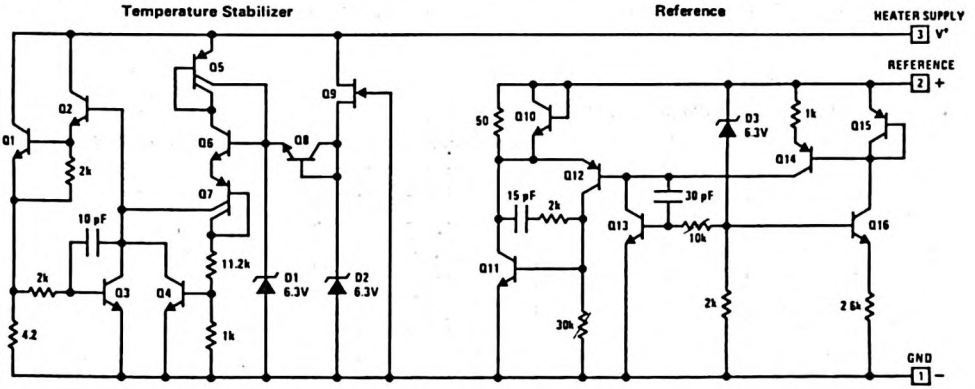
The LM3999 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, precision voltage or current sources or precision power supplies. Further, in many cases, the LM3999 can replace references in existing equipment with a minimum of wiring changes.

The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C.

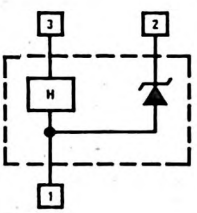
features

- Guaranteed 0.0005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 5%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Low power for stabilization – 400 mW at 25°C
- Long term stability – 20 ppm

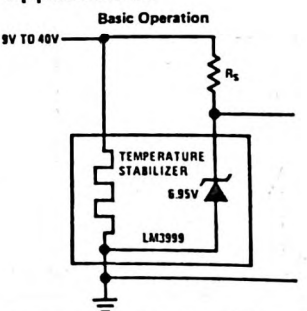
schematic diagram



functional block diagram



typical applications



absolute maximum ratings

Temperature Stabilizer Voltage	36V
Reverse Breakdown Current	20 mA
Forward Current	0.1 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

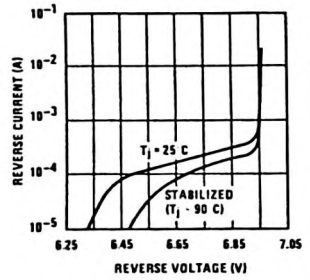
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$0.6\ mA \leq I_R \leq 10\ mA$	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.6\ mA \leq I \leq 10\ mA$		6	20	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	$0°C \leq T_A \leq 70°C$		0.0002	0.0005	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$		7		μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20		ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		5		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$		140	200	mA

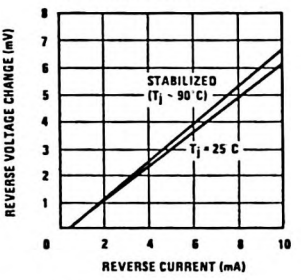
Note 1: These specifications apply for 30V applied to the temperature stabilizer and $0°C \leq T_A \leq +70°C$.

typical performance characteristics

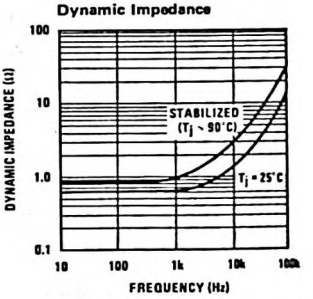
Reverse Characteristics



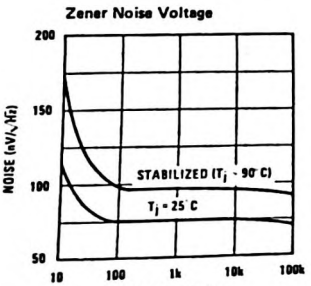
Reverse Voltage Change



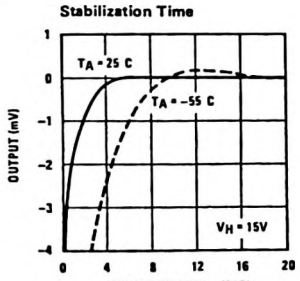
Dynamic Impedance



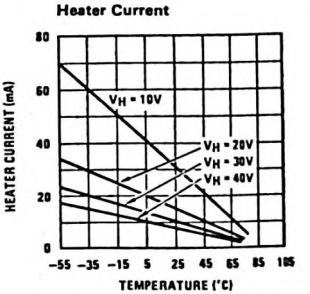
Zener Noise Voltage



Stabilization Time

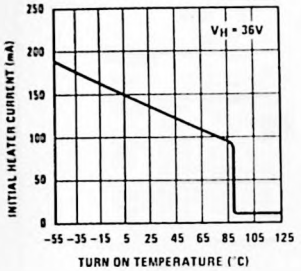


Heater Current

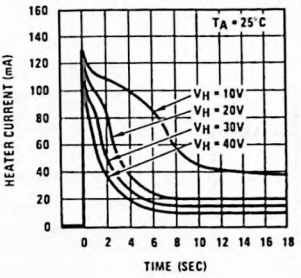


typical performance characteristics (con't)

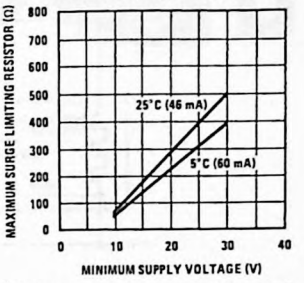
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

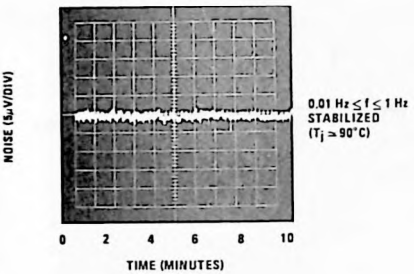


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

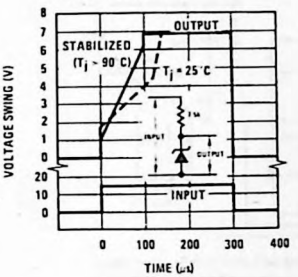


*Heater must be bypassed with a 2 μF tantalum capacitor if maximum value resistors are used. Otherwise 30% to 50% smaller values must be used. If heater voltage oscillates under any condition, temperature is not at control point.

Low Frequency Noise Voltage

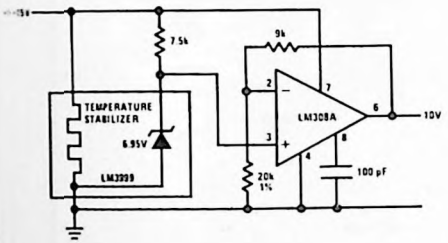


Response Time

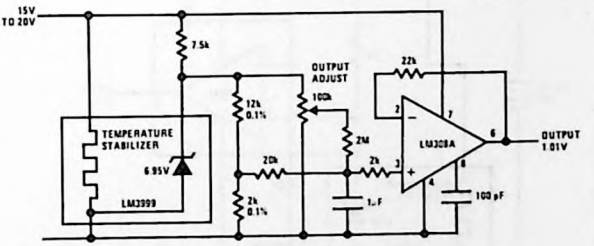


typical applications (con't)

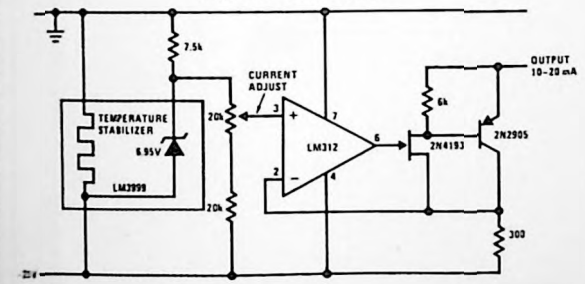
Buffered Reference With Single Supply



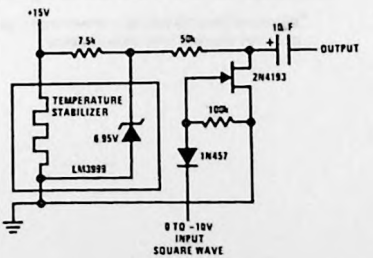
Voltage Reference



Negative Current Source

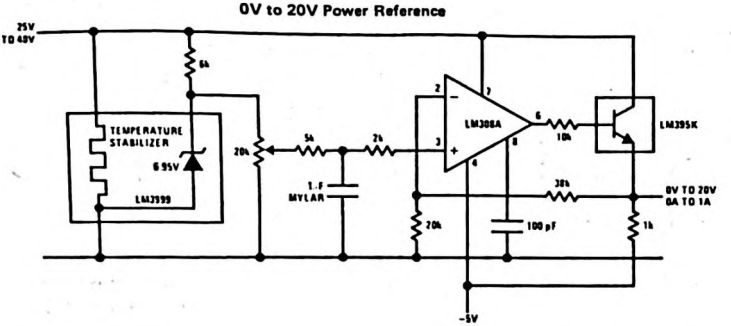


Square Wave Voltage Reference

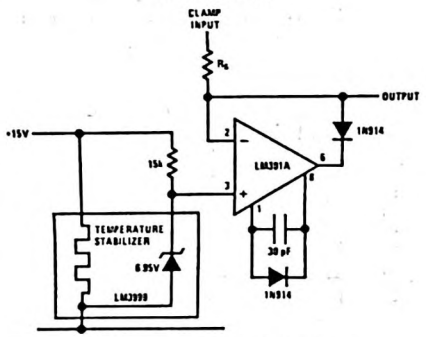


typical applications (con't)

0V to 20V Power Reference

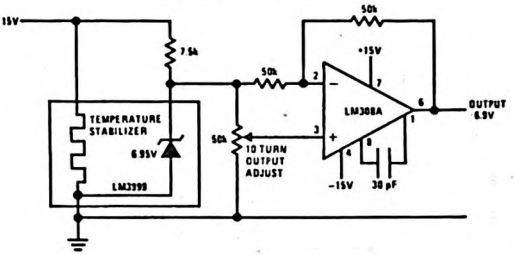


Precision Clamp*

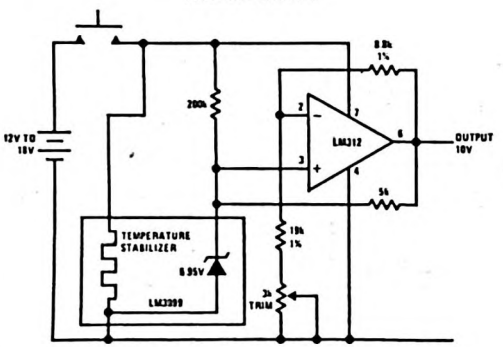


*Clamp will sink 5 mA when input goes more positive than reference.

Bipolar Output Reference



Portable Calibrator*



*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

connection diagram

Plastic Package

BOTTOM VIEW

Order Number LM3999Z
See NS Package Z03A

Section 7

Analog Switches/ Multiplexers

7

National Semiconductor

Analog Switches/Multiplexers

AH0014/AH0014C DPDT TTL/DTL Compatible MOS Analog Switches

AH0015/AH0015C Quad SPST TTL/DTL Compatible MOS Analog Switches

AH0019/AH0019C Dual DPST TTL/DTL Compatible MOS Analog Switches

general description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

features

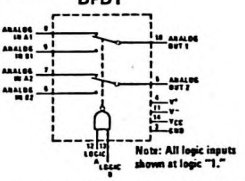
- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications. For information on other National analog switches and analog interface elements, see listing on last page.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

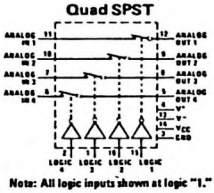
block and connection diagrams

DPDT



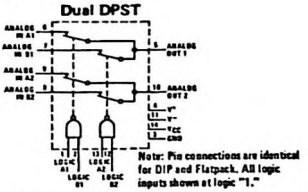
Order Number AH0014D or AH0014CD
See NS Package D14A

Quad SPST



Order Number AH0015D or AH0015CD
See NS Package D14A

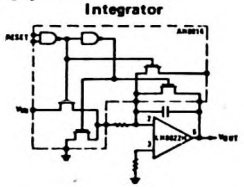
Dual DPST



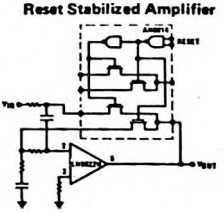
Order Number AH0019D or AH0019CD
See NS Package D14A

typical applications

Integrator



Reset Stabilized Amplifier



*Previously called NH0014/NH0014C and NH0019/NH0019C

absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input — each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input — each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance — each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current — each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current — each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time — t_{OFF}	See test circuit; T_A = 25°C		760	600	ns
Analog Turn-ON Time — t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V, V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

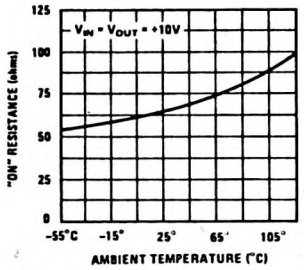
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

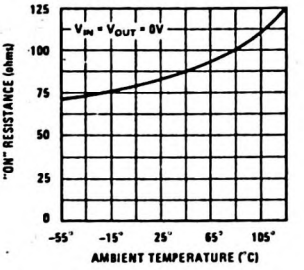
Note 4: All analog switch pins except measurement pin are tied to V^+.

analog switch characteristics (Note 2)

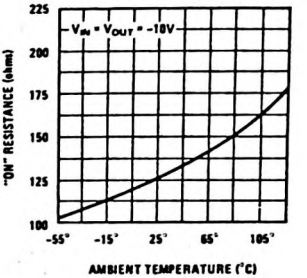
R_{ON} vs Temperature



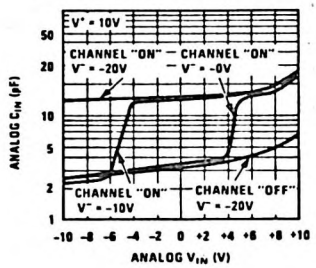
R_{ON} vs Temperature



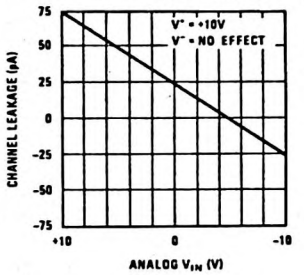
R_{ON} vs Temperature



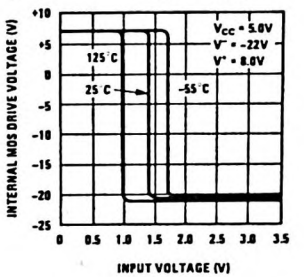
C_{IN} vs V_{IN}



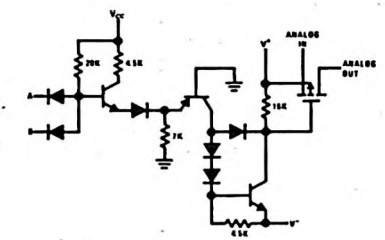
Leakage vs V_{IN} (Channel "OFF")



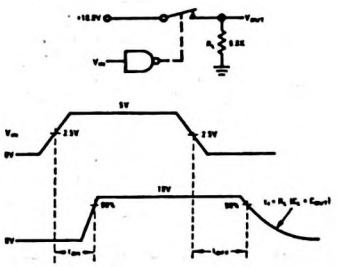
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

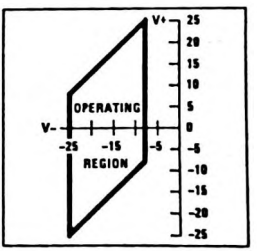


Analog Switching Time Test Circuit



selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between –25V and –8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



National Semiconductor

AH0120/AH0130/AH0140/AH0150/AH0160 Series Analog Switches

general description

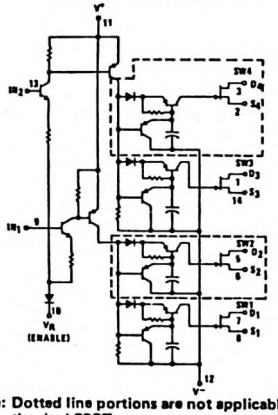
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically 0.4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C

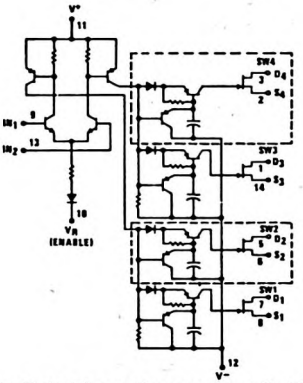
schematic diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

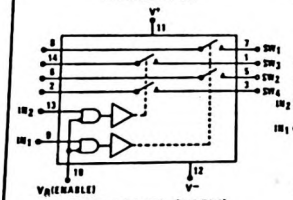


Note: Dotted line portions are not applicable to the SPDT (differential).

Order any of the devices below using the part number with a D or F suffix. See NS Packages D14A or F14A. AH0133C, AH0134C, AH0151C, AH0152C available in N Package also.

logic and connection diagrams

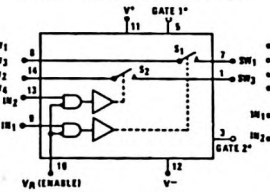
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

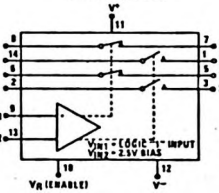
DUAL SPST
* Pinned out in N Package only.



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

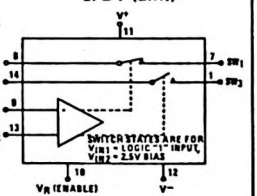
DPDT (diff.)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (diff.)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

absolute maximum ratings

	High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30 mA	30 mA
Power Dissipation		See Curve
Operating Temperature Range AH0100 Series		−55°C to +125°C
AH0100C Series		−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	$V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	T_A = 25°C	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	T_A = 25°C	0.1	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	I^+_{ON}	All Circuits				One Driver ON Note 2	T_A = 25°C	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	I^-_{ON}	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	I^+_{OFF}	All Circuits				V_{IN1} V_{IN2} = 0.8V	T_A = 25°C	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	I^-_{OFF}	All Circuits				V_{IN1} = V_{IN2} 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} = V_{IN2} 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	V_D = 10V, I_D = 1 mA	T_A = 25°C	45	80	Ω
							Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	V_D = 10V, I_D = 1 mA	T_A = 25°C	25	30	Ω
							Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	V_D = 10V, I_F = 1 mA	T_A = 25°C	8	10	Ω
							Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	T_A = 25°C	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	V_{DS} = ±20V	T_A = 25°C	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	V_{DS} = ±20V	T_A = 25°C	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit V_A = ±10V T_A = 25°C		0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit V_A = ±10V T_A = 25°C		0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit V_A = ±10V T_A = 25°C		0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit V_A = ±10V T_A = 25°C		1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for T_A = 25°C.

Note 2: For the DPST and Dual DPST, the ON condition is for V_{IN} = 2.5V; the OFF condition is for V_{IN} = 0.8V. For the differential switches and SW1 and 2 ON, V_{IN2} = 2.5V, V_{IN1} = 3.0V. For SW3 and 4 ON, V_{IN2} = 2.5V, V_{IN1} = 2.0V.

electrical characteristics for "MEDIUM LEVEL" Switches (Note 1)

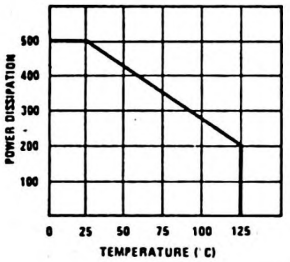
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	I_{INION}	All Circuits				Note 2	$T_A = 25°C$	20	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	I_{INIOFF}	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	µA
							Over Temp. Range		2	µA
Positive Supply Current Switch ON	I^+_{ION}	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	I^-_{ION}	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	I_{RION}	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	I^+_{IOFF}	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	I^-_{IOFF}	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Reference Input (Enable) OFF Current	I_{RIOFF}	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Switch ON Resistance	r_{dsON}	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$, $I_D = 1mA$	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	r_{dsON}	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$, $I_D = 1mA$	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	µA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	µs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	µs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	µs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	µs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

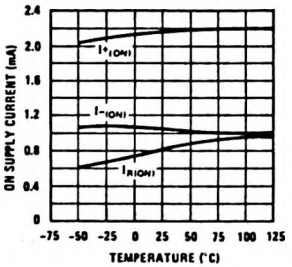
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

typical performance characteristics

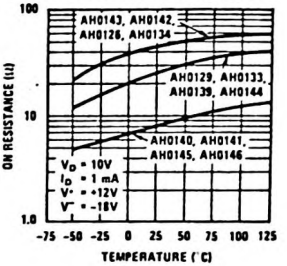
Power Dissipation vs Temperature



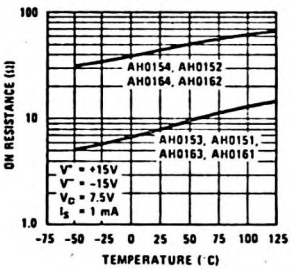
ON Supply Current vs Temperature



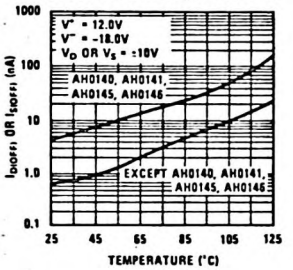
rds(ON) vs Temperature AH0120 thru AH0140 Series



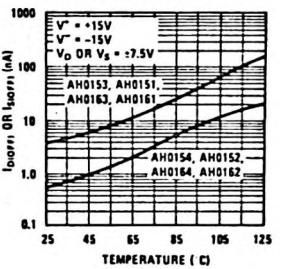
rds(ON) vs Temperature AH0150/AH0160 Series



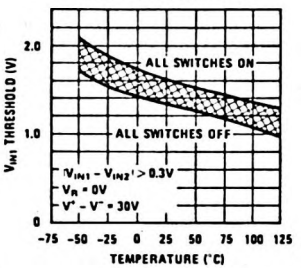
Leakage Current vs Temperature AH0120, AH0130, & AH0140



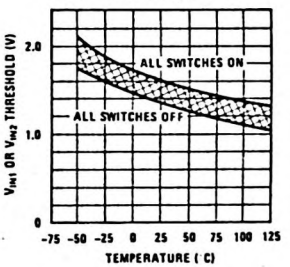
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

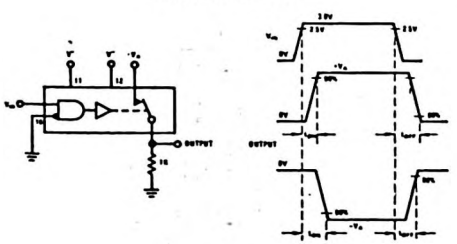


Differential Switch Input Threshold vs Temperature

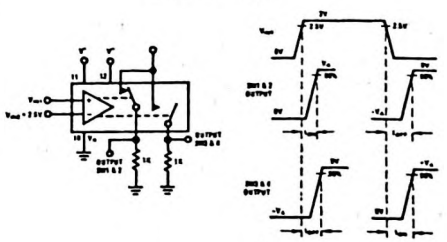


switching time test circuits

Single Ended Input



Differential Input



applications information

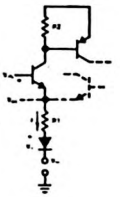
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V+0.7V+0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

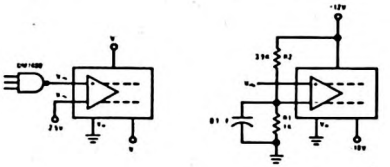
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

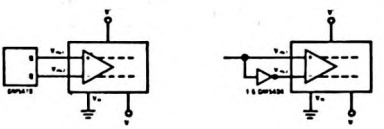
$$|V_{IN1} - V_{IN2}| \geq 0.3V$$

$$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$$

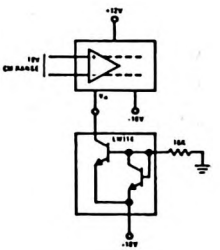
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

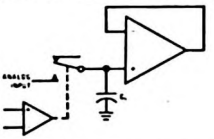
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

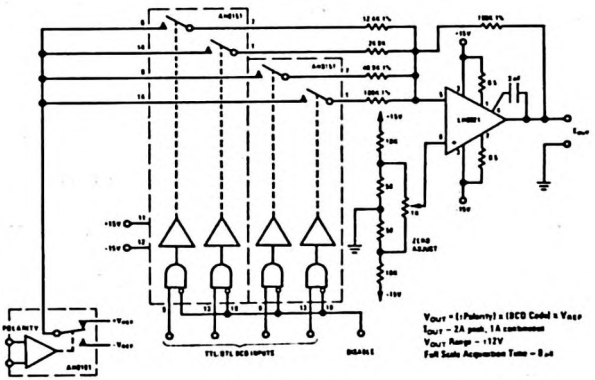
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



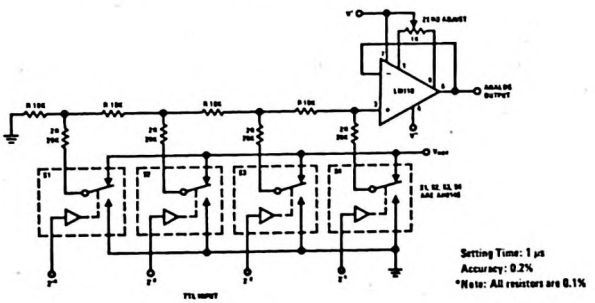
Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

typical applications

Programmable One Amp Power Supply

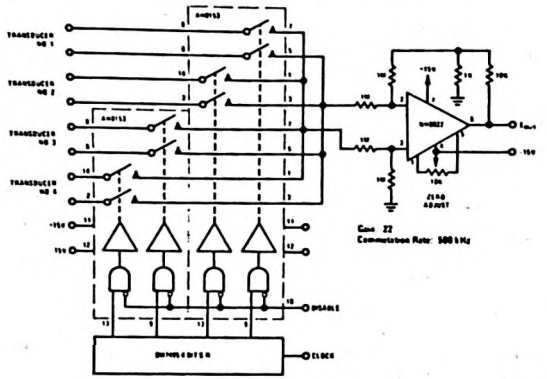


Four to Ten Bit D to A Converter (4 Bits Shown)



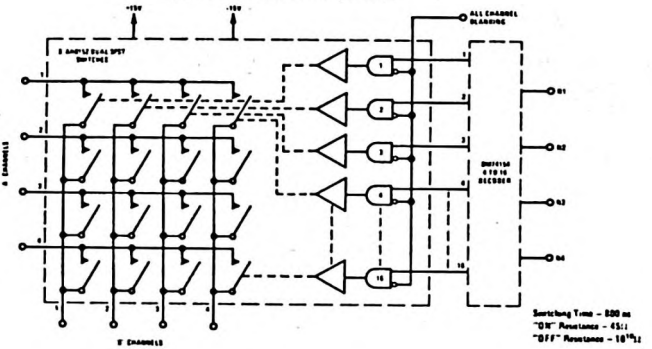
typical applications (con't)

Four Channel Differential Transducer Commutator



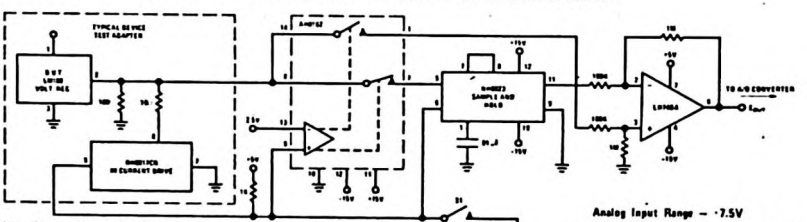
Gain = 22
Commutation Rate: 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – $10^{10}\Omega$

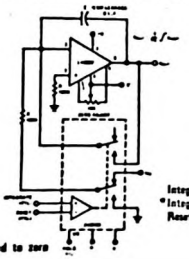
Delta Measurement System for Automatic Linear Circuit Tester



Note: S1 must be open for 50μs min* to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other setup forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

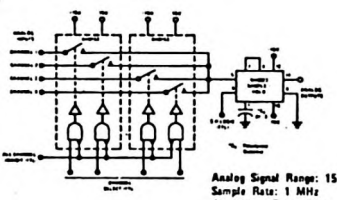
Precision Long Time Constant Integrator with Reset



Integration Interval = 10 sec
*Integration Error = 100μV
Reset Time: 30μs

*Note: V_{OS} adjusted to zero

Four Channel Commutator



Analog Signal Range: $15V_{p-p}$
Sample Rate: 1 MHz
Acquisition Time: 20μs
Drift Rate: 0.5 mV/sec

National Semiconductor

AH2114/AH2114C DPST Analog Switch

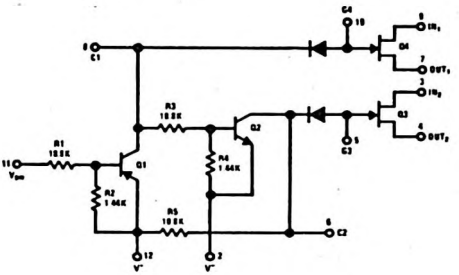
General Description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

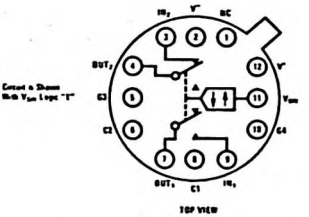
- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 μs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

Schematic and Connection Diagrams

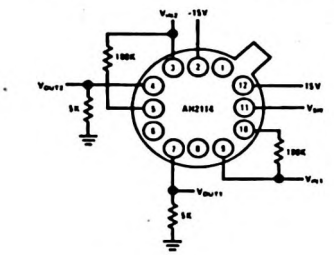


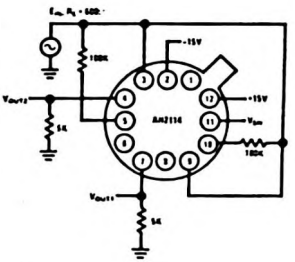
Metal Can Package



Order Number AH2114H or AH2114CH
See NS Package H12C

AC Test Circuit and Waveforms





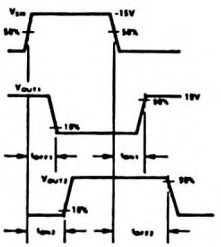


FIGURE 1.

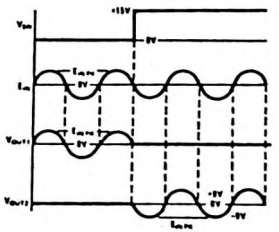


FIGURE 2.

Absolute Maximum Ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	−25V
Vplus−Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1.36W
Operating Temperature Range	
AH2114	−55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1.0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1.0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = −7V, T_A = 25°C		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to −15V, −55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above 25°C.

National Semiconductor

Monolithic N-Channel Junction FET Switches with High Speed Drivers

AM181/AM281, AM182/AM282 dual driver with SPST switches
AM184/AM284, AM185/AM285 dual driver with DPST switches
AM187/AM287, AM188/AM288 single driver with SPDT switches
AM190/AM290, AM191/AM291 dual driver with SPDT switches

General Description

These devices combine N-channel junction FETs and bipolar transistors on a single chip for the first time in a new N-channel Bi-FET process.

This technology provides the industry's only low "ON" resistance, high speed, monolithic N-channel junction FET analog switch. Unique circuit techniques are employed to achieve break-before-make switching action and constant "ON" resistance over the analog voltage range. The switch can block 20V peak-to-peak signals, and because of the driver design, an "OFF" isolation greater than 60 dB is achieved at 10 MHz.

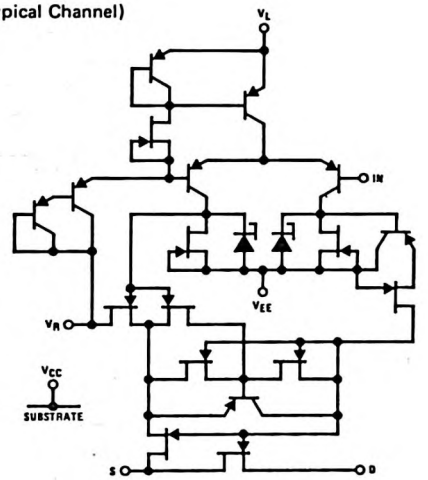
Features

- Interfaces with standard DTL, TTL and CMOS
- Constant "ON" resistance with signals to ±10V
- "ON" resistance match 2 Ω typ
- "OFF" isolation and crosstalk less than −60 dB at 10 MHz (typ)
- t_{ON}/t_{OFF} = 105 ns/95 ns typ
- Break-before-make action

Applications

- A-to-D/D-to-A converters
- Data acquisition
- Signal multiplexers
- Sample and hold
- Video switch

Schematic Diagram (Typical Channel)



Application Hints*

V_{CC} Positive Supply Voltage (V)	V_{EE} Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max− (V)	100 Series V_S Analog Voltage Range (V)	200 Series V_S Analog Signal Range (V)
+15**	−15	+5	Gnd	2.0/0.8	−7.5 to +15	−10 to +15
+10	−20	+5	Gnd	2.0/0.8	−12.5 to +10	−15 to +10
+12	−12	+5	Gnd	2.0/0.8	−4.5 to +12	−7 to +12

*Applications Hints are for design aid only, not guaranteed and not subject to production testing

**Electrical Parameter Chart based on V_{CC} + 15V, V_{EE} = −15V, V_L = 5V, V_R = Gnd

Absolute Maximum Ratings

$V_{CC} - V_{EE}$	36V
$V_{CC} - V_D$	33V
$V_D - V_{EE}$	33V
$V_D - V_S$	±22V
$V_L - V_{EE}$	36V
$V_L - V_{IN}$	8V
$V_L - V_R$	8V
$V_{IN} - V_R$	8V
$V_R - V_{EE}$	27V
$V_R - V_{IN}$	2V
Current (Any Terminal)	30 mA

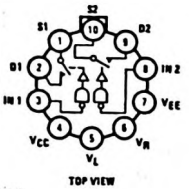
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation*	
Metal Can**	450 m
14-Pin DIP***	825 m
16-Pin DIP****	900 m

* All leads soldered to PC board
** Derate 6 mW/°C above 75°C
*** Derate 11 mW/°C above 75°C
**** Derate 12 mW/°C above 75°C

Connection Diagrams

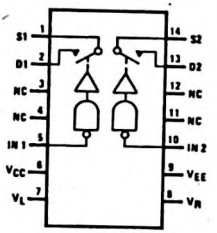
AM181/AM281, AM182/AM282▲

Metal Can Package
See NS Package H10A
Order by Part Number
Followed by H Suffix



TOP VIEW

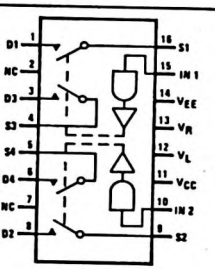
Switch states are for logical "1" input



TOP VIEW

Dual-In-Line Package
See NS Package D14A
Order by Part Number
Followed by D Suffix

AM184/AM284, AM185/AM285▲



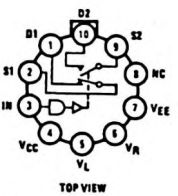
TOP VIEW

Dual-In-Line Package
See NS Package D16A
Order by Part Number
Followed by D Suffix

Switch states are for logical "0" input

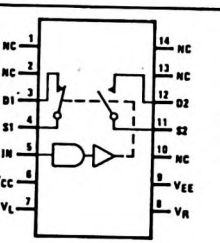
AM187/AM287, AM188/AM288▲

Metal Can Package
See NS Package H10A
Order by Part Number
Followed by H Suffix



TOP VIEW

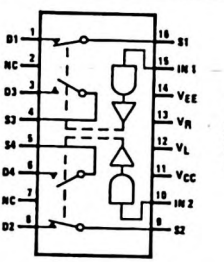
Switch states are for logical "1" input



TOP VIEW

Dual-In-Line Package
See NS Package D14A
Order by Part Number
Followed by D Suffix

AM190/AM290, AM191/AM291▲



TOP VIEW

Dual-In-Line Package
See NS Package D16A
Order by Part Number
Followed by D Suffix

Switch states are for logical "1" input

▲Consult local sales representative or factory for information concerning the 14-pin flat package

Electrical Characteristics AM181/AM281, AM182/AM282

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM181 −55°C	AM181 25°C	AM181 125°C	AM281 −20°C	AM281 25°C	AM281 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)}$ + $I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 0.8V	V_D = V_S = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM182 −55°C	AM182 25°C	AM182 125°C	AM282 −20°C	AM282 25°C	AM282 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V	V_D = −10V	75	75	100	100	100	150	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)}$ + $I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 0.8V	V_D = V_S = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM181, AM182 −55°C	AM181, AM182 25°C	AM181, AM182 125°C	AM281, AM282 −20°C	AM281, AM282 25°C	AM281, AM282 85°C	UNITS
$C_{S(OFF)}$	Source "OFF" Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain "OFF" Capacitance		V_D = −5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)}$ + $C_{S(ON)}$	Channel "ON" Capacitance		V_D = V_S = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	Both V_{IN} = 0, All Channels "ON"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	Both V_{IN} = 5V, All Channels "OFF"			0.1			0.1		
I_{EE}	Negative Supply Current				−5			−5		
I_A	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM184/AM284, AM185/AM285

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM184 −55°C	AM184 25°C	AM184 125°C	AM284 −20°C	AM284 25°C	AM284 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10 mA, V_{IN} = 2V	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 0.8V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V	V_D = V_S = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM185 −55°C	AM185 25°C	AM185 125°C	AM285 −20°C	AM285 25°C	AM285 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10V, V_{IN} = 2V	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 0.8V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V	V_D = V_S = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM184, AM185 −55°C	AM184, AM185 25°C	AM184, AM185 125°C	AM284, AM285 −20°C	AM284, AM285 25°C	AM284, AM285 85°C	UNITS
$C_{S(OFF)}$	Source OFF Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain OFF Capacitance		V_D = −5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance		V_D = V_S = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	Both V_{IN} = 5V, All Channels "ON"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−4			−4		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	Both V_{IN} = 0, All Channels "OFF"			0.1			0.1		
I_{EE}	Negative Supply Current				−5.5			−5.5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM187/AM287, AM188/AM288

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM187 −55°C	AM187 25°C	AM187 125°C	AM287 −20°C	AM287 25°C	AM287 85°C	UNITS
$r_{DS(ON)}$	Drain Source "ON" Resistance	I_S = −10 mA, V_{IN} = 2V, Ch. 1 "ON", V_{IN} = 0.8V, Ch. 2 "ON"	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V, Ch. 2 "OFF" V_{IN} = 0.8V, Ch. 1 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)}$ + $I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 2V, Ch. 1 "ON" V_{IN} = 0.8V, Ch. 2 "ON"	V_D = V_S = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM188 −55°C	AM188 25°C	AM188 125°C	AM288 −20°C	AM288 25°C	AM288 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V, Ch. 2 "ON", V_{IN} = 2V, Ch. 1 "ON"	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 0.8V, Ch. 1 "OFF" V_{IN} = 2V, Ch. 2 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)}$ + $I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 2V, Ch. 1 "ON" V_{IN} = 0.8V, Ch. 2 "ON"	V_D = V_S = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM187, AM188 −55°C	AM187, AM188 25°C	AM187, AM188 125°C	AM287, AM288 −20°C	AM287, AM288 25°C	AM287, AM288 85°C	UNITS
$C_{S(OFF)}$	Source "OFF" Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain "OFF" Capacitance		V_D = 5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)}$ + $C_{S(ON)}$	Channel "ON" Capacitance		V_D = V_S = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	V_{IN} = 0, Ch. 2 "ON", Ch. 1 "OFF"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−3			−3		
I_L	Logic Supply Current				3.2			3.2		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	V_{IN} = 5V, Ch. 2 "OFF", Ch. 1 "ON"			0.1			0.1		
I_{EE}	Negative Supply Current				−3			−3		
I_L	Logic Supply Current				3.2			3.2		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM190/AM290, AM191/AM291

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM190 −55°C	AM190 25°C	AM190 125°C	AM290 −20°C	AM290 25°C	AM290 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10 mA, V_{IN} = 2V, Ch. 1 and 2 "ON", V_{IN} = 0.8V, Ch. 3 and 4 "ON"	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 2V, Ch. 3 and 4 "OFF" V_{IN} = 0.8V, Ch. 1 and 2 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V, Ch. 1 and 2 "ON" V_{IN} = 0.8V, Ch. 3 and 4 "ON"	V_D = V_S = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn OFF Time				130			150		

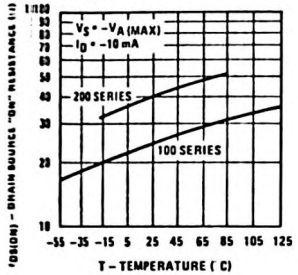
PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM191 −55°C	AM191 25°C	AM191 125°C	AM291 −20°C	AM291 25°C	AM291 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10 mA, V_{IN} = 0.8V, Ch. 3 and 4 "ON", V_{IN} = 2V, Ch. 1 and 2 "ON"	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 0.8V, Ch. 1 and 2 "OFF" V_{IN} = 2V, Ch 3 and 4 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 0.8V, Ch. 3 and 4 "ON" V_{IN} = 2V, Ch. 1 and 2 "ON"	V_D = V_S = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM190, AM191 −55°C	AM190, AM191 25°C	AM190, AM191 125°C	AM290, AM291 −20°C	AM290, AM291 25°C	AM290, AM291 85°C	UNITS
$C_{S(OFF)}$	Source OFF Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain OFF Capacitance		V_D = 5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance		V_D = V_S = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	V_{IN} = 0, Ch. 3 and 4 "ON", Ch. 1 and 2 "OFF"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	V_{IN} = 5V, Ch. 3 and 4 "OFF", Ch. 1 and 2 "ON"			0.1			0.1		
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

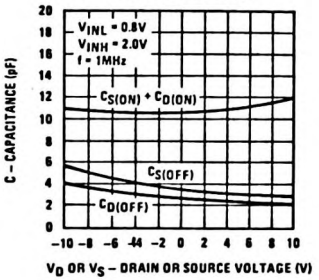
Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Typical Performance Characteristics V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0 unless otherwise noted.

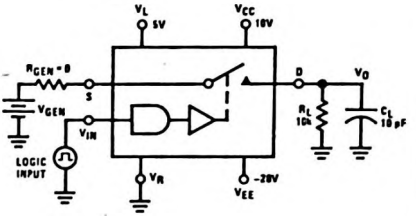
$r_{DS(ON)}$ vs V_D and Temperature



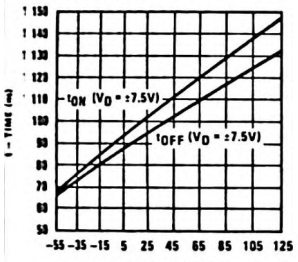
Capacitance vs V_D or V_S



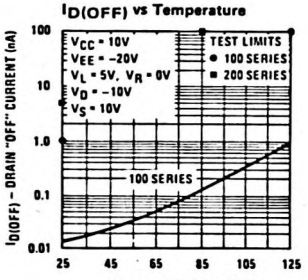
Typical delay, rise, fall, settling times, and switching transients in this circuit.



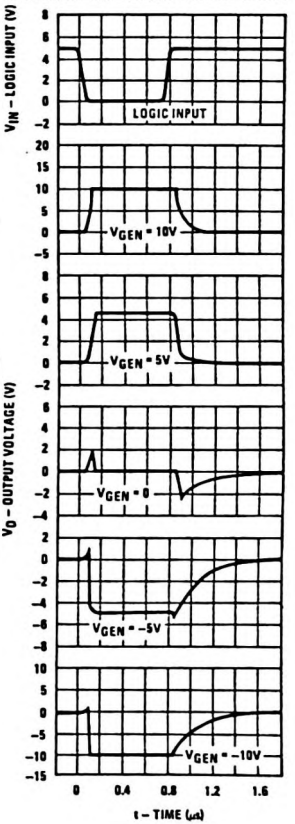
Switching Time vs V_D and Temperature



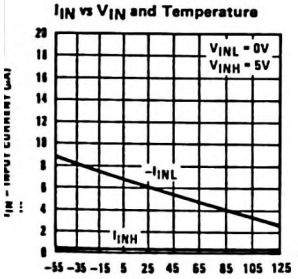
$I_{D(OFF)}$ vs Temperature



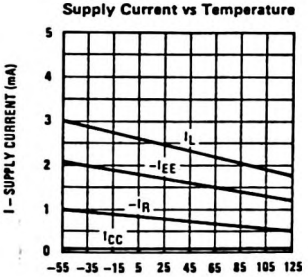
If R_{GEN}, R_L or C_L is increased there will be proportional increases in rise and/or fall RC times.



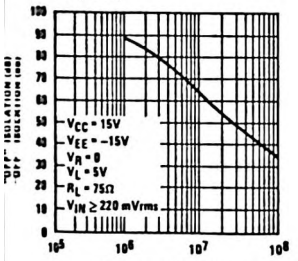
I_{IN} vs V_{IN} and Temperature



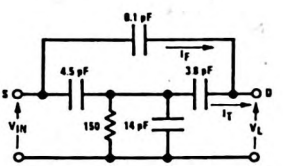
Supply Current vs Temperature



"OFF" Isolation vs Frequency

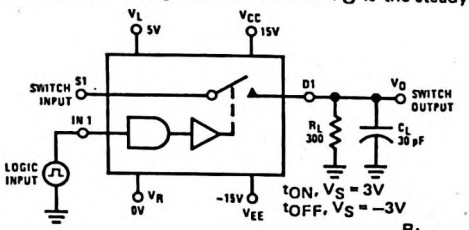


Equivalent "OFF" Circuit



Switching Time Test Circuit

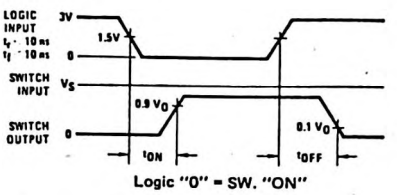
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch "ON". Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



t_{ON}, V_S = 3V
t_{OFF}, V_S = −3V

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

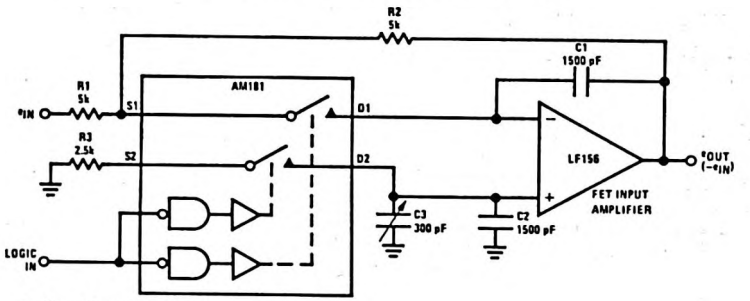
(Repeat test for IN2 and S2)



Logic "0" = SW. "ON"

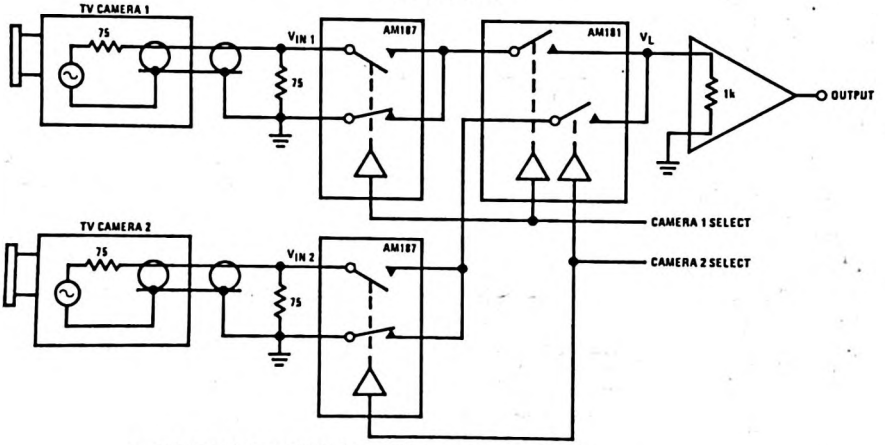
Typical Applications

Low Drift-Compensated Sample and Hold



- Input impedance 5 kΩ
- Slew rate limiting and 3 dB point: 20V swing: 3.2K C; 5V swing: 12K C; small signal: 21K C
- Droop rate @ 25°C 0.5 nV per μs
- Sample to hold offset adjustable to zero
- Acquisition time—98 μs
- Aperture time—80 ns
- Aperture uncertainty—2 ns

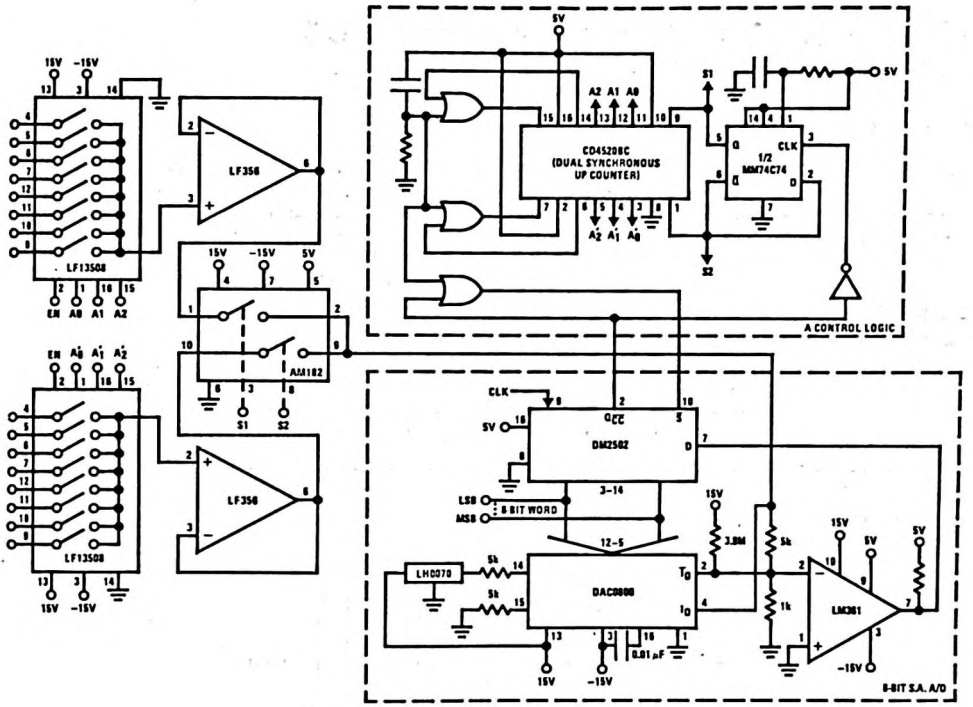
Video Switch with Very High "OFF" Isolation
(f = dc to 10 MHz)



- 116 dB isolation at 10 MHz, "OFF" camera to "ON" camera
- 98 dB isolation at 10 MHz, load from each camera when both cameras are "OFF"
- < 1 dB on insertion loss

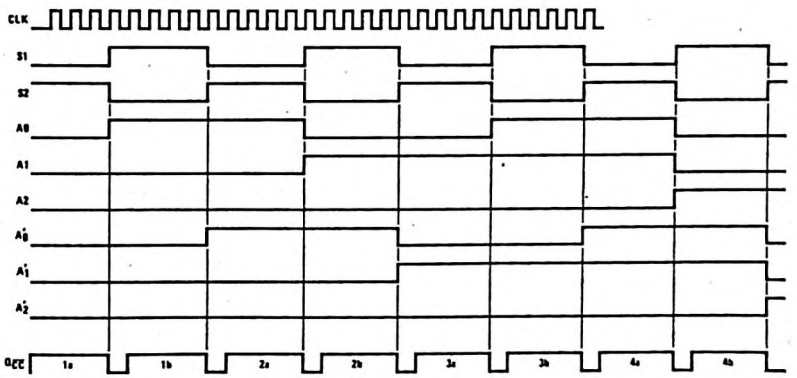
Typical Applications (Continued)

A 16-Channel Data Acquisition Unit with Second Level Multiplexing



- Maximum A/D clock frequency: 4.5 MHz
- Maximum throughput rate: 31.25k samples/sec
- Minimum switch "ON" time for the 2-channel MUX: $t_{ON(min)} \leq 1/4.5$ MHz
- Maximum input signal bandwidth 15.6 kHz
- Maximum input signal variation during conversion for 8-bit accuracy and 10V full scale: $\Delta V_{IN}/\Delta T = 19.5\ mV/\mu s$

Timing Diagram



National Semiconductor

AM2009/AM2009C, MM4504/MM5504 6-Channel MOS Multiplex Switches

General Description

The AM2009/AM2009C/MM4504/MM5504 are six channel multiplex switches constructed on a single silicon chip using low threshold P-channel MOS process. The gate of each MOS device is protected by a diode circuit.

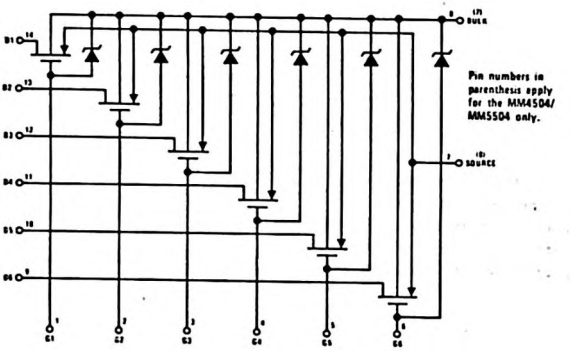
The AM2009/AM2009C/MM4504/MM5504 are designed for applications such as time division multiplexing of analog or digital signals. Switching speeds are primarly determined by conditions external to the device such as signal source impedance, capacitive loading and the total number of channels used in parallel.

The AM2009/MM4504 are specified for operation over the -55°C to +125°C military temperature range. The AM2009C/MM5504 are specified for operation over the -25°C to +85°C temperature range.

Features

- Typical low "on" resistance 150Ω
- Typical low "off" leakage 100 pA
- Typical large analog voltage range ±10V
- Zero inherent offset voltage
- Normally off with zero gate voltage

Schematic Diagrams

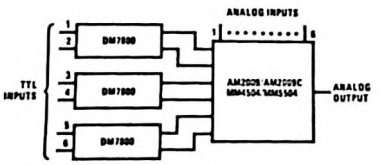


Order Number
AM2009F or AM2009CF
MM4504F or MM5540F
See NS Package F14A

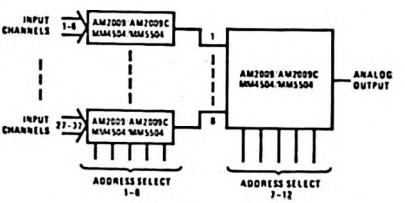
Order Number
AM2009D or AM2009CD
MM4504D or MM5504D
See NS Package D14A

Order Number AM2009CN
or MM4504CN
See NS Package N14A

Typical Applications



TTL Compatible 6 Channel MUX



32 Channel MUX

Absolute Maximum Ratings (V_{BULK} = 0V)

Voltage on Any Source or Drain	−30V	Total Power Dissipation (at T_A = 25°C)	900 mW
Voltage on Any Gate	−35V	Power Dissipation — each gate circuit	150 mW
Positive Voltage on Any Pin	+0.3V	Operating Temperature Range AM2009	−55°C to +125°C
Source or Drain Current	50 mA	AM2009C	−25°C to +85°C
Gate Current (forward direction of zener clamp)	0.1 mA	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Threshold Voltage	$V_{GS} = V_{DS}$, $I_{DS} = -1\ \mu A$	−1.0		−3.0	V
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		150	250	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		500	1250	Ω
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$			325	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$			1500	Ω
Gate Leakage	$V_{GS} = -20V$, Note 2 $V_{GS} = -20V$, Note 2, $T_A = 25°C$		 100	1.0	μA pA
Input Leakage	$V_{DS} = -20V$, Note 2 $V_{DS} = -20V$, Note 2, $T_A = 25°C$		 100	1.0	μA pA
Output Leakage	$V_{SD} = -20V$, Note 2 $V_{SD} = -20V$, Note 2, $T_A = 25°C$		 500	3.0	μA pA
Gate-Bulk Breakdown Voltage	$I_{GB} = -10\ \mu A$, Note 2	−35			V
Source-Drain Breakdown Voltage	$I_{SD} = -10\ \mu A$, $V_{GD} = 0$, Note 2	−30			V
Drain-Source Breakdown Voltage	$I_{DS} = -10\ \mu A$, $V_{GS} = 0$, Note 2	−30			V
Transconductance			4000		mhos
Gate Capacitance	Note 3, f = 1 MHz		4.7	8	pF
Input Capacitance	Note 3, f = 1 MHz		4.6	8	pF
Output Capacitance	Note 3, f = 1 MHz		16	20	pF

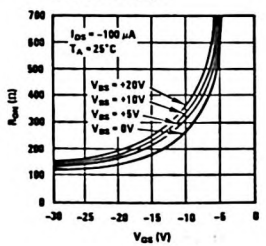
Note 1: Ratings apply over the specified temperature range and V_{BULK} = 0, unless otherwise specified.

Note 2: All other pins grounded.

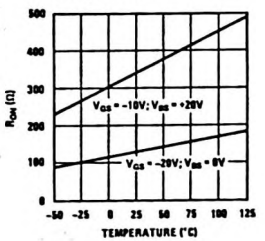
Note 3: Capacitance measured on dual-in-line package between pin under measurement to all other pins. Capacitances are guaranteed by design.

Typical Performance Characteristics

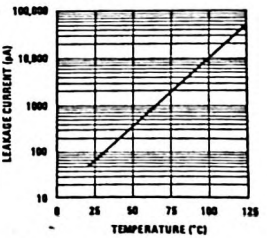
"ON" Resistance vs Gate-to-Source Voltage



"ON" Resistance vs T Temperature



Input Leakage Current vs Temperature



National Semiconductor

AM3705/AM3705C 8-Channel MOS Analog Multiplexer

General Description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

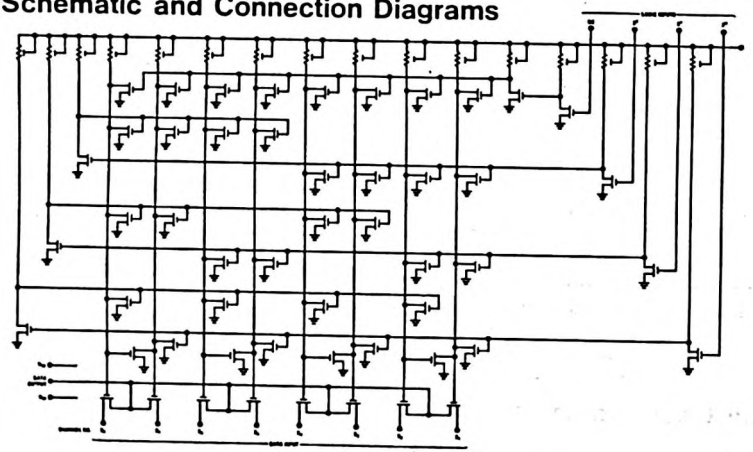
Important design features include:

- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

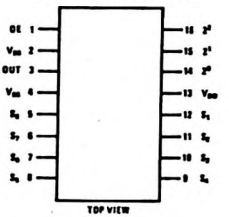
The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

The AM3705 is specified for operation over the −55°C to +125°C military temperature range. The AM3705C is specified for operation over the −25°C to +85°C temperature range.

Schematic and Connection Diagrams



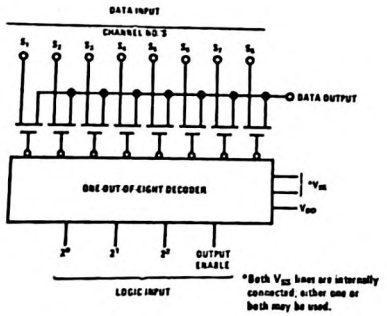
Dual-In-Line Package



Order Number AM3705D or AM3705CD
See NS Package D16A

Order Number AM3705F or AM3705CF
See NS Package F16A

Block Diagram (MIL-STD-806B)



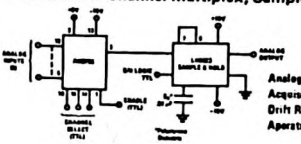
*Both V_{EE} lines are internally connected, either one or both may be used.

Truth Table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

Typical Application

Buffered 8-Channel Multiplex, Sample and Hold



Analog Signal Range — ±5V
Acquisition Time — 25 μs
Drift Rate — 0.5 mV/sec
Aperture Time — 250 ns

Absolute Maximum Ratings

Positive Voltage on Any Pin (Note 1)		+0.3V
Negative Voltage on Any Pin (Note 1)		−35V
Source to Drain Current		±30 mA
Logic Input Current		±0.1 mA
Power Dissipation (Note 2)		500 mW
Operating Temperature Range	AM3705	−55°C to +125°C
	AM3705C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\,\mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\,\mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\,\mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$; $I_{OUT} = 100\,\mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\,\mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\,\mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-	Switching Time Test Circuit		600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

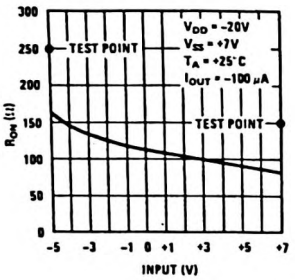
Note 1: All voltages referenced to V_{SS}.

Note 2: Ratings applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

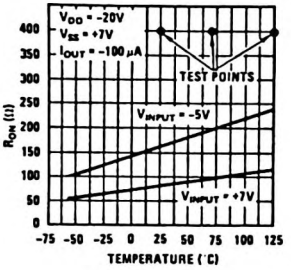
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

Typical Performance Characteristics

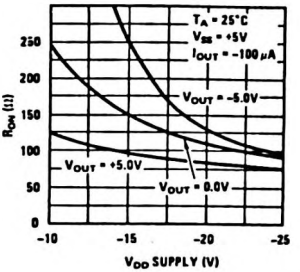
ON Resistance vs Analog Input Voltage



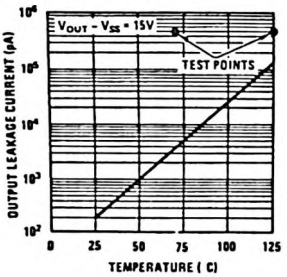
ON Resistance vs Ambient Temperature



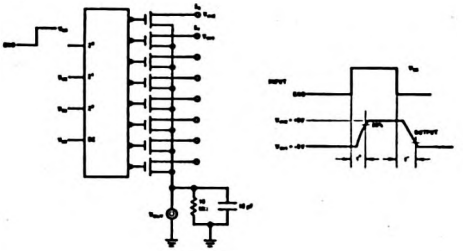
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

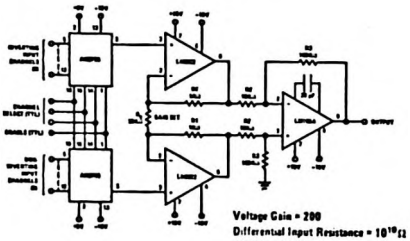


Switching Time Test Circuit



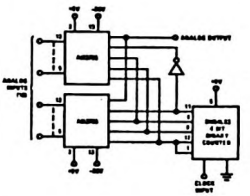
Typical Applications (Continued)

Differential Input MUX

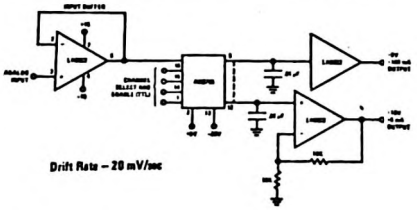


Voltage Gain = 200
Differential Input Resistance = 10^{10} Ω
CMRR = 100 dB
Input Current = 0.5 nA

16-Channel Commutator

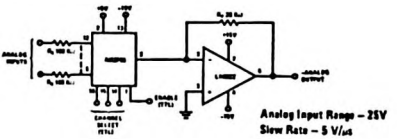


8-Channel Demultiplexer with Sample and Hold



Drift Rate – 20 mV/sec

Wide Input Range Analog Switch



Analog Input Range – 25V
Slew Rate – 5 V/µs

National Semiconductor

AM9709/AM97C09/AH5009 Series Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches designed to economically fulfill a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

The AM97C09 series is specifically intended to be driven from CMOS providing the best performance at lowest cost.

Applications

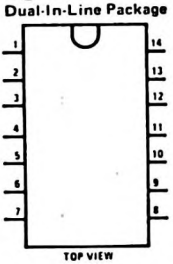
- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

Interfaces with standard TTL and CMOS	
On-resistance match	2 ohms
Low "ON" resistance	100 ohms
Very low leakage	50 pA
Large analog signal range	±10V peak
High switching speed	150 ns
Excellent isolation between channels	80 dB at 1 kHz

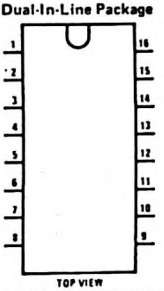
Connection Diagrams

Dual-In-Line Package



Order Number AM9709CN, AM9710CN, AM97C09CN, AM97C10CN, AH5009CN, AH5010CN, AH5013CN or AH5014CN
See NS Package N14A

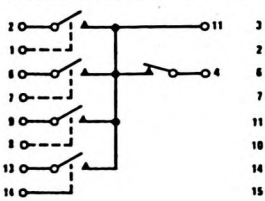
Dual-In-Line Package



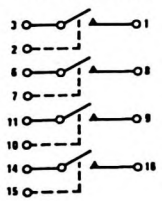
Order Number AM9711CN, AM9712CN, AM97C09CN, AM97C10CN, AH5011CN, AH5012CN, AH5015CN or AH5016CN
See NS Package N16A

Functional and Schematic Diagrams (Additional type on other pages)

MUX Switches (4-Channel Version Shown)

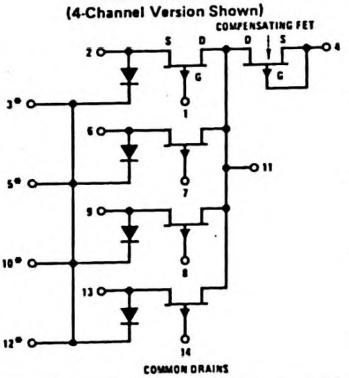


SPST Switches (Quad Version Shown)

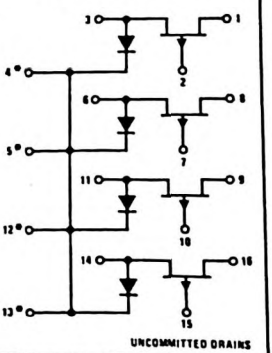


*Note: All diode cathodes are internally connected to the substrate.

MUX Switches (4-Channel Version Shown)



SPST Switches (Quad Version Shown)



Absolute Maximum Ratings

Input Voltage	
AM9709–12CN, AH5009–24CN	30V
AM97C09–12CN	25V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

AM9709, AM97C09, AH5009 (Notes 1 and 2)

PARAMETER		CONDITIONS	5V TTL AM9710CN AM9712CN		5V TTL AH5010–16 (EVEN SERIES)		5V–10V CMOS AM97C10CN AM9712CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V	0.01	0.2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 4.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.08	1	0.08	1	0.08	1	nA
		T_A = 85°C		200		200		200	nA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.13	5		1000	0.13	5	nA
		T_A = 85°C		10		10		10	μA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.1	10		100	0.10	10	nA
		T_A = 85°C		20		100		20	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0.35V, I_S = 2 mA	90	150	90	150			Ω
		T_A = +85°C		240		240			Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					90	150	Ω
		T_A = 85°C						240	Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	4	20		50	4	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Note 1: Test conditions 25°C unless otherwise noted.
Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

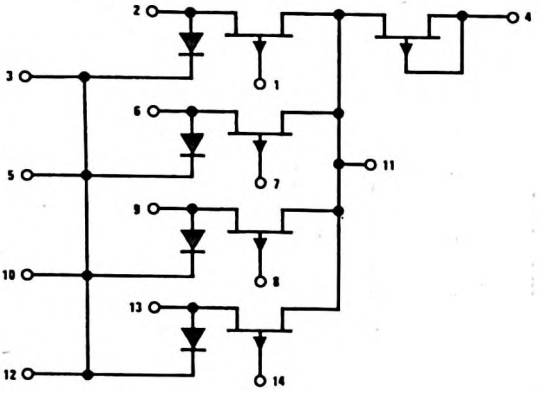
Electrical Characteristics (Continued)

	PARAMETER	CONDITIONS	15V TTL AM9709CN AM9711CN		15V TTL AH5009–15 (ODD SERIES)		10–15V CMOS AM97C09CN AM97C11CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{S(X)}$	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
$I_{S(X)}$	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 9.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 10.3V	0.01	2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.04	0.5	0.04	0.5	0.04	0.5	nA
		T_A = 85°C		100		100		100	nA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.07	2		2	0.07	2	nA
		T_A = 85°C		1		2		1	μA
$I_{D(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.05	5		100	0.05	5	nA
		T_A = 85°C		2		20		2	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					60	100	Ω
		T_A = 85°C						160	Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 1.5V, I_S = 2 mA	60	100	60	100			Ω
		T_A = 85°C		160		160			Ω
$V_{D(DIODE)}$	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	2	10		50	2	10	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Schematic Diagrams and Pin Connections

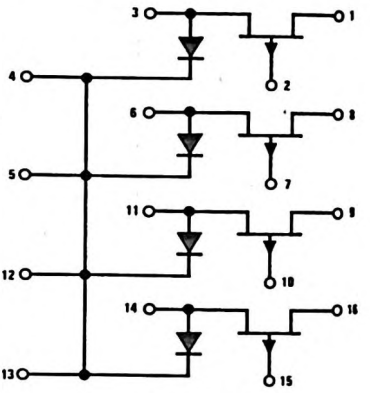
Four Channel

AM97C09CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C10CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9709CN, AH5009CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9710CN, AH5010CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

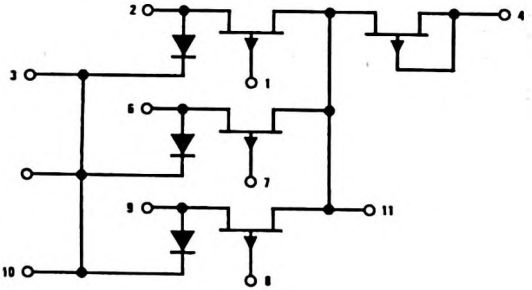
AM97C11CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C12CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9711CN, AH5011CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9712CN, AH5012CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



16-Pin DIP

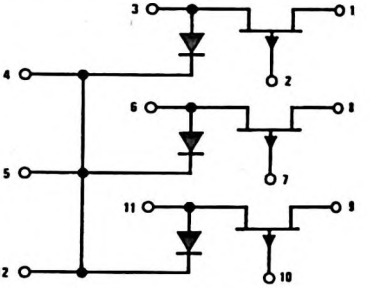
Three-Channel

AH5013CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5014CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

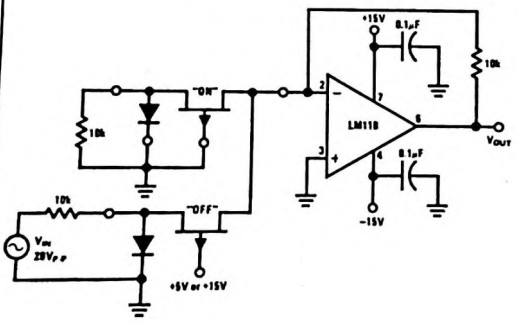
AH5015CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5016CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



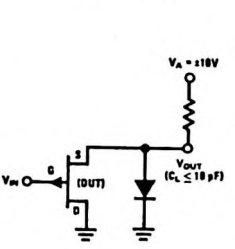
16-Pin DIP

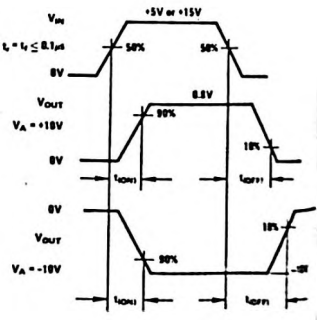
Test Circuits and Switching Time Waveforms

Cross Talk Test Circuit



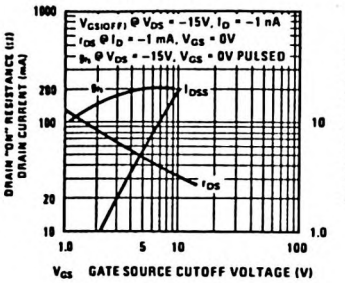
ac Test Circuit



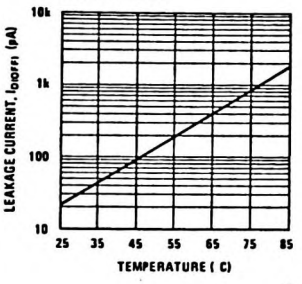


Typical Performance Characteristics

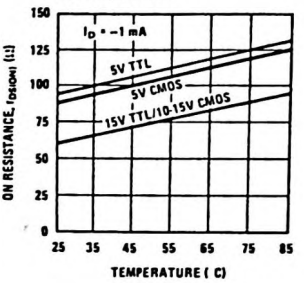
Parameter Interaction



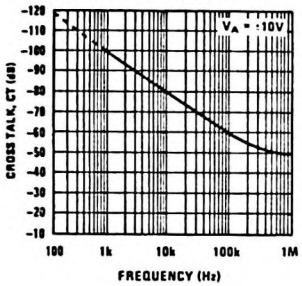
Leakage Current, $I_{D(OFF)}$ vs Temperature



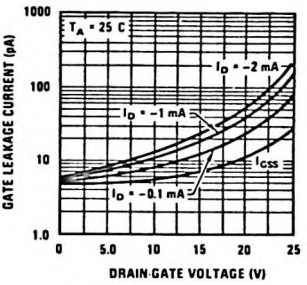
On Resistance, $r_{DS(ON)}$ vs Temperature



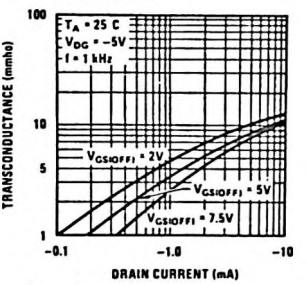
Cross Talk, CT vs Frequency



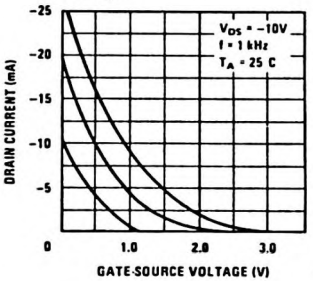
Leakage Current vs Drain-Gate Voltage



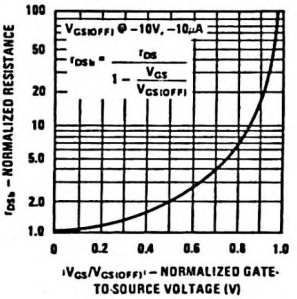
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



Applications Information

Theory of Operation

The AM/AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AM9710), 5V–10V CMOS (AM97C10), open collector 15V TTL (AM9709), and 10–15V CMOS (AM97C09).

Two basic switch configurations are available: multiple independent switches (N by SPST) and multiple pole switches used for multiplexing (NPST-MUX). The MUX versions such as the AM9709 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1.*

Applications Information (Continued)

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AM/AH series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is worse.

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

≅ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, I_S ≅ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AM9710. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\, A_D}{(N)\, I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)}$ ≤ 10 nA at 85°C for the AM9709, $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

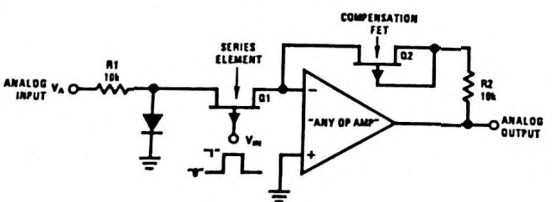


FIGURE 1. Use of Compensation FET

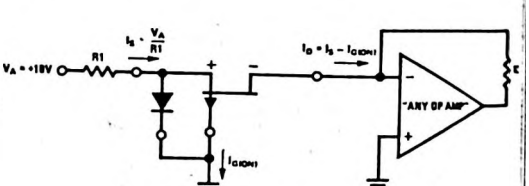


FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

TTL Compatibility

Two input logic drive versions of AM/AH series are available: the even numbered part types are specified to be driven from standard 5V-TTL logic and the odd numbered types from 15V open collector TTL.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AM9710, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5*. In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} and the expense of power dissipation in the low state.

CMOS Compatibility

The cost effective AM97C09 series of switches is optimized for CMOS drive without resistor pull-up. The AM97C10's and AM97C12's are specified for 5V–10V operation while the AM97C09's and AM97C11's are specified for 10V–15V operation.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6*.

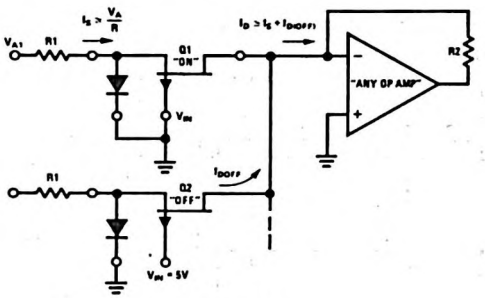


FIGURE 3.

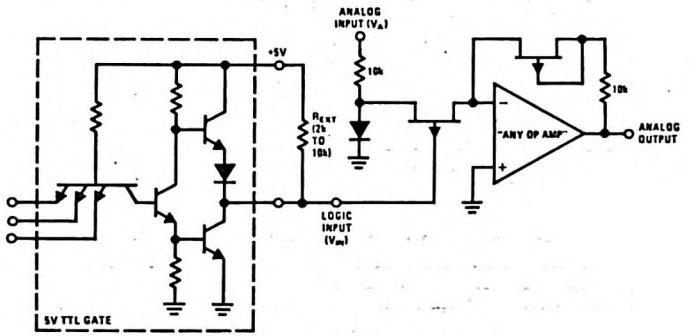


FIGURE 4. Interfacing with +5V TTL

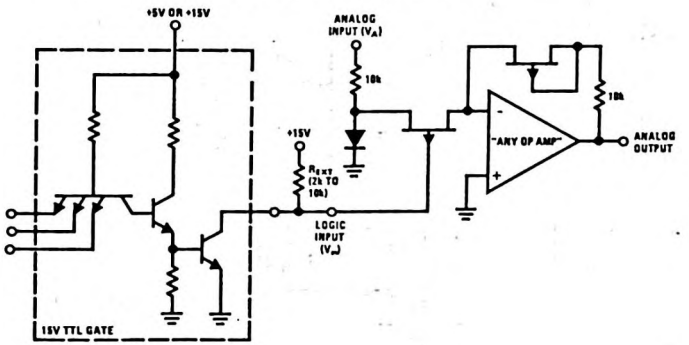


FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

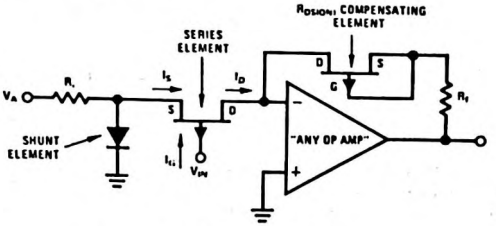
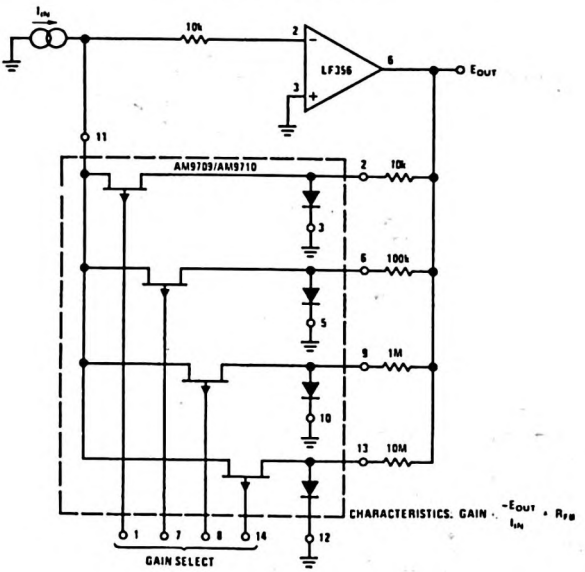


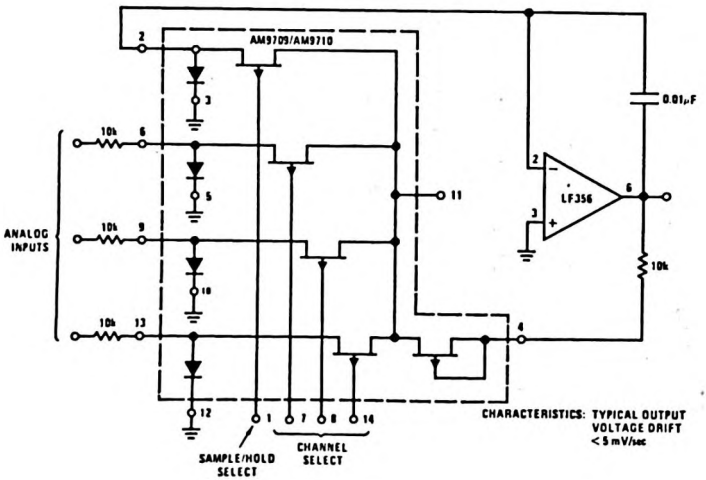
FIGURE 6. Definition of Terms

Typical Applications

Gain Programmable Amplifier

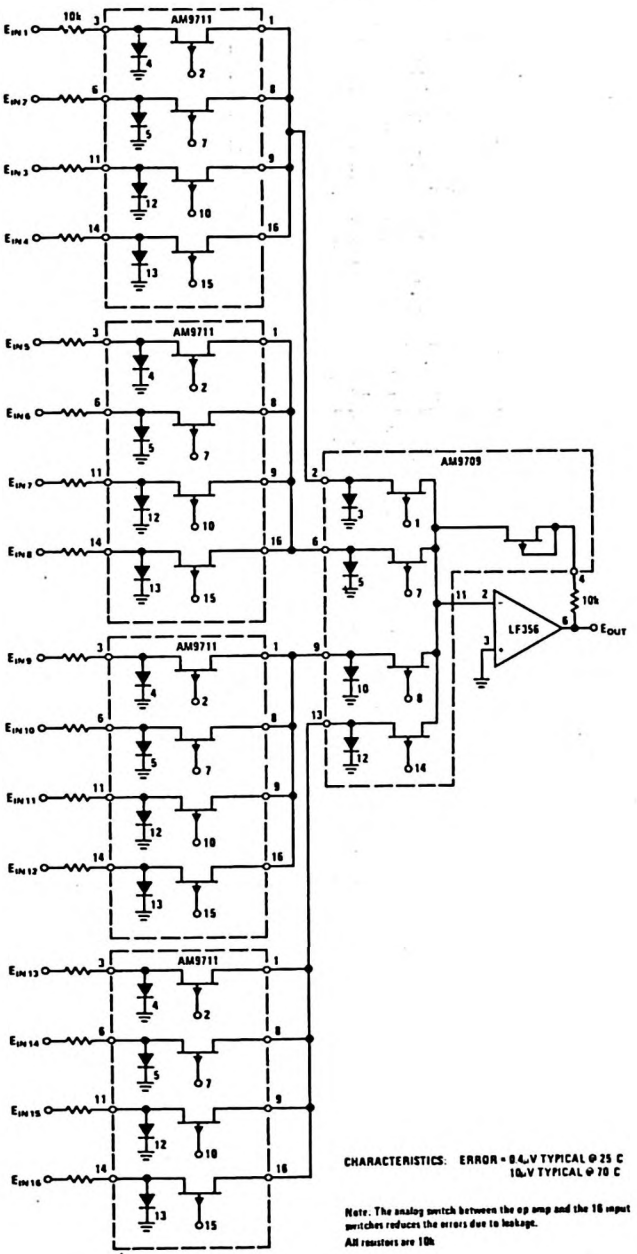


3-Channel Multiplexer with Sample and Hold



Typical Applications (Continued)

16-Channel Multiplexer



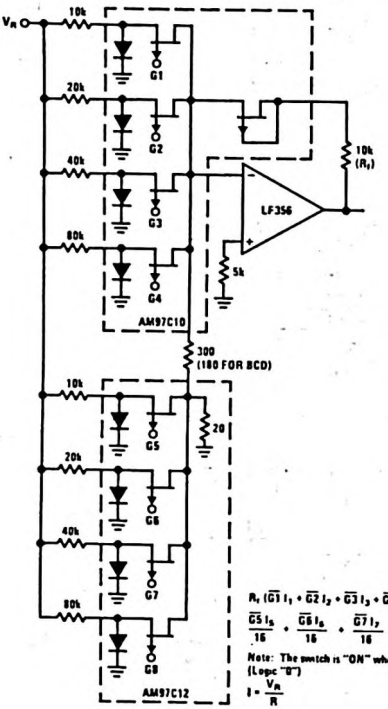
CHARACTERISTICS: ERROR = 0.4 V TYPICAL @ 25 C
1.0 V TYPICAL @ 70 C

Note. The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k

Typical Applications (Continued)

8-Bit Binary (BCD) Multiplying D/A Converter



National Semiconductor

CD4016M/CD4016C Quad Bilateral Switch

general description

The CD4016M/CD4016C is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

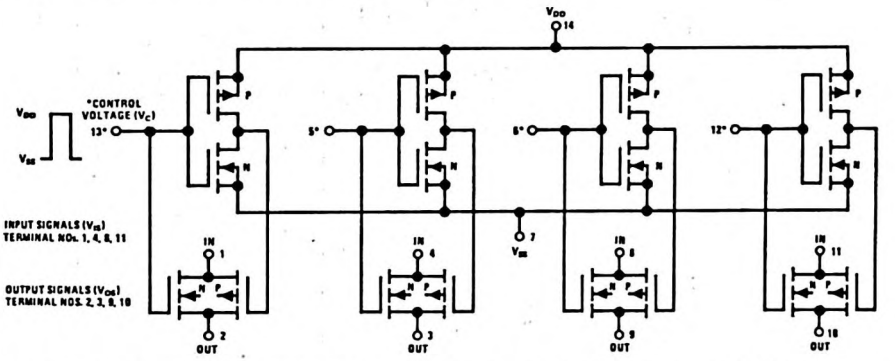
features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ.
■ Wide range of digital and analog levels	±7.5 V_{PEAK}
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS} = 15V$
■ Matched switch characteristics	$\Delta R_{ON} = 40\Omega$ typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ $f_{is} = 10$ kHz $R_L = 10k$
■ High degree of linearity	.5% distortion typ. @ $f_{is} = 1$ kHz
■ Extremely low leakage	$V_{is} = 5\ V_{p-p}$ $V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$
■ Transmits frequencies up to 10 MHz	

applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

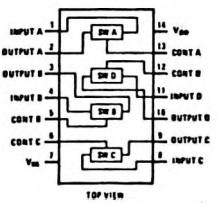
schematic and connection diagrams



Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{in} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}



Order Number CD4016MD or CD4016CD
See NS Package D14A

Order Number CD4016MF or CD4016CF
See NS Package F14A

Order Number CD4016MJ or CD4016CJ
See NS Package J14A

Order Number CD4016MN or CD4016CN
See NS Package N14A

Order Number CD4016MW or CD4016CW
See NS Package W14A

absolute maximum ratings

Voltage at Any Pin (Note 1) V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD4016M −55°C to +125°C
CD4016C −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500mW
Lead Temperature (Soldering, 10 seconds) 300°C
Operating V_{DD} Range V_{SS} + 3V to V_{SS} + 15V

electrical characteristics CD4016M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −55°C MIN	LIMITS −55°C TYP	LIMITS −55°C MAX	LIMITS 25°C MIN	LIMITS 25°C TYP	LIMITS 25°C MAX	LIMITS 125°C MIN	LIMITS 125°C TYP	LIMITS 125°C MAX	UNITS
Quiescent Dissipation per Package	P_T	TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_a 1, 4, 8, 11 ≤ +10; V_{os} 2, 3, 9, 10 ≤ +10			5		0.1	5			300	μW
All Switches "ON"		TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 +10; $V_a = V_{os}$ 1-4, 8-11 < +10			5		0.1	5			300	μW
Threshold Voltage N Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_a) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_a: +7.5V		120	360		200	400		300	600	Ω
		+7.5V, −7.5V, −7.5V		120	360		200	400		300	600	Ω
		±0.25V		130	775		280	850		470	1230	
		+5V		130	600		250	660		400	960	
		+5V, −5V, −5V		130	600		250	660		400	960	Ω
		±0.25V		325	1870		580	2000		900	2600	
		+15V		120	360		200	400		300	600	
		+15V, 0V, +0.25V		120	360		200	400		300	600	Ω
		9.3V		150	775		300	850		490	1230	
		+10V		130	600		250	660		400	960	
		+10V, 0V, +0.25V		130	600		250	660		400	960	Ω
		5.6V		300	1870		560	2000		880	2600	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, −7.5V, ±7.5V					10					Ω
		+5V, −5V, +5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_a = 1 kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage–Switch "OFF" (Effective "OFF" Resistance)		V_{DD} +7.5V, $V_C - V_{SS}$ −7.5V, V_a +7.5V / −7.5V					±100 / ±100					pA
		V_{DD} +5V, $V_C - V_{SS}$ −5V, V_a +5V / −5V					(Note 2)	125		(Note 2)	125	nA
Frequency Response–Switch "ON" (Sine Wave Input)		$V_C = V_{DD} = +5V$, $V_{SS} = -5V$; R_L = 1 kΩ; V_a = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_a} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		$V_{DD} = +5V$, $V_C = V_{SS} = -5V$; $20 \log_{10} \frac{V_{os}}{V_a} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		R_L = 1 kΩ; $V_a(A)$ = 5V(p-p); $V_C(A) = V_{DD} = +5V$, $V_C(B) = V_{SS} = -5V$; $20 \log_{10} \frac{V_{os}(B)}{V_a(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					pF
Output	C_{OS}						4					
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V$, V_{SS} = GND, C_L = 15 pF; V_a = 10V (square wave); $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_a < V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C < V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave); R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_r = t_f$ = 20 ns; V_a < 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave); $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. **Note 2:** ±10 x 10^{-3}. **Note 3:** Symmetrical about 0V.

electrical characteristics CD4016C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −40°C MIN	LIMITS −40°C TYP	LIMITS −40°C MAX	LIMITS 25°C MIN	LIMITS 25°C TYP	LIMITS 25°C MAX	LIMITS 85°C MIN	LIMITS 85°C TYP	LIMITS 85°C MAX	UNITS
Quiescent Dissipation per Package	P_T	TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_{in} 1, 4, 8, 11 ≤ +10; V_{os} 2, 3, 9, 10 ≤ +10										
All Switches "OFF"					5		0.1	5			80	μW
All Switches "ON"		TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 +10; $V_{in} = V_{os}$ 1-4, 8-11 ≤ +10										
					5		0.1	5			80	μW
Threshold Voltage N-Channel	$V_{TH}N$	$I_{DS} = 10\ \mu A$, $V_{DD} = 5V$, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	$I_{DS} = 10\ \mu A$, $V_{DD} = 5V$, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{in}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	$R_L = 10k\Omega$; $V_C = V_{DD}$, V_{SS}, V_{in}: +7.5V, −7.5V, ±0.25V		130	370		200	400		260	520	Ω
		+5V, −5V, ±0.25V		150	610		250	660		340	840	Ω
		+15V, 0V, +0.25V		130	370		200	400		260	520	Ω
		+10V, 0V, +0.25V		150	610		250	660		340	2380	Ω
		+7.5V, −7.5V, ±7.5V					10					Ω
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+5V, −5V, ±5V					15					Ω
Sine Wave Response (Distortion)		$R_L = 10\ k\Omega$, $f_{in} = 1$ kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		V_{DD} / $V_C = V_{SS}$ / V_{in}: +7.5V / −7.5V / +7.5V / −7.5V					±100					pA
		+5V / −5V / +5V / −5V					±100 (Note 2) 125 (Note 2)					nA
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD} = +5V$, $V_{SS} = -5V$; $R_L = 1\ k\Omega$, $V_{in} = 5V(p\text{-}p)$; $20\ \text{Log}_{10} \frac{V_{os}}{V_{in}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		$V_{DD} = +5V$, $V_C = V_{SS} = -5V$; $20\ \text{Log}_{10} \frac{V_{os}}{V_{in}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		$R_L = 1\ k\Omega$, $V_{in}(A) = 5V(p\text{-}p)$; $V_C(A) = V_{DD} = +5V$, $V_C(B) = V_{SS} = -5V$; $20\ \text{Log}_{10} \frac{V_{os}(B)}{V_{in}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	$V_{DD} = +5V$, $V_C = V_{SS} = -5V$					4					pF
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V$, $V_{SS} = GND$, $C_L = 15$ pF; $V_{in} = 10V$ (square wave); $t_r = t_f = 20$ ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{in} < V_{DD}$; $V_{DD} - V_{SS} = 15V$, 10V, 5V; $I_{IS} = 10\ \mu A$				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS} = 10V$; $V_C \lesssim V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS} = 10V$, $V_C = 10V$ (square wave), $R_L = 10\ k\Omega$					50					mV
Turn "ON" Propagation Delay	$t_{PHL}C$	$t_{rc} = t_{fc} = 20$ ns, $V_{in} < 10V$, $C_L = 15$ pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} 10V, $V_{SS} = GND$, $R_L = 1\ k\Omega$, $C_L = 15$ pF, $V_C = 10V$ (square wave), $t_r = t_f = 20$ ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. Note 2: $\pm 10 \times 10^{-3}$. Note 3: Symmetrical about 0V.

typical ON resistance characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{in} (V)	VALUE (Ω)	V_{in} (V)	VALUE (Ω)	V_{in} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: R_{ON} = 0Ω.

National Semiconductor

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer

CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer

CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

general description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15 Vp-p can be achieved by digital signal amplitudes of 3-15 V. For example, if V_{DD} = 5 V, V_{SS} = 0 V and V_{EE} = −5 V, analog signals from −5 V to +5 V can be controlled by digital inputs of 0-5 V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF."

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

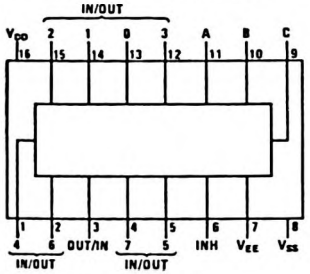
CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

features

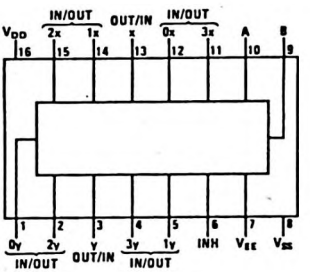
- Wide range of digital and analog signal levels: digital 3-15 V, analog to 15 Vp-p
- Low "ON" resistance: 80 Ω (typ) over entire 15 Vp-p signal-input range for $V_{DD} - V_{EE}$ = 15 V
- High "OFF" resistance: channel leakage of ±10 pA (typ) at $V_{DD} - V_{EE}$ = 10 V
- Logic level conversion for digital addressing signals of 3-15 V ($V_{DD} - V_{SS}$ = 3-15 V) to switch analog signals to 15 Vp-p ($V_{DD} - V_{EE}$ = 15 V)
- Matched switch characteristics: ΔR_{ON} = 5 Ω (typ) for $V_{DD} - V_{EE}$ = 15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ) at $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10 V
- Binary address decoding on chip

connection diagrams



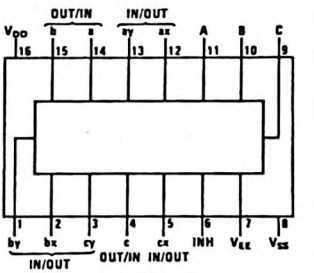
TOP VIEW

Order Number CD4051BMD or CD4051BCD
See NS Package D16A
Order Number CD4051BMF or CD4051BCF
See NS Package F16A
Order Number CD4051BMJ or CD4051BCJ
See NS Package J16A



TOP VIEW

Order Number CD4052BMD or CD4052BCD
See NS Package D16A
Order Number CD4052BMJ or CD4052BCJ
See NS Package J16A
Order Number CD4052BMN or CD4052BCN
See NS Package N16A
Order Number CD4052BMW or CD4052BCW
See NS Package W16A



TOP VIEW

Order Number CD4053BMD or CD4053BCD
See NS Package D16A
Order Number CD4053BMF or CD4053BCF
See NS Package F16A
Order Number CD4053BMJ or CD4053BCJ
See NS Package J16A
Order Number CD4053BMW or CD4053BCW
See NS Package W16A

absolute maximum rating

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD} + 0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

recommended operating conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0 V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

dc electrical characteristics (Note 2)

	Parameter	Conditions		−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+125°C Max	+125°C Min	+125°C Max	Units
I_{DD}	Quiescent Device Current	V_{DD} = 5V			5			5		150	μA
		V_{DD} = 10V			10			20		600	μA
		V_{DD} = 15V			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V		2000		270	2500		3500	Ω
			V_{DD} = 5V V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V		310		120	400		580	Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V		220		80	280		400	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V				10				Ω
			V_{DD} = 5V, V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V				10				Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5V, V_{EE} = −7.5V O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		V_{DD} = 7.5V, V_{EE} = −7.5V, O/I = 0V,	CD4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1kΩ to V_{SS} I_{IS} < 2μA on all OFF channels V_{IS} = V_{DD} thru 1kΩ									
		V_{DD} = 5V			1.5			1.5		1.5	V
		V_{DD} = 10V			3.0			3.0		3.0	V
		V_{DD} = 15V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15V, V_{EE} = 0V V_{IN} = 0V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{EE} = 0V V_{IN} = 15V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

dc electrical characteristics (con't) (Note 2)

	Parameter	Conditions		−40°C		+25°C		+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DDD}	Quiescent Device Current	V_{DD} = 5V			20			20		150	μA
		V_{DD} = 10V			40			40		300	μA
		V_{DD} = 15V			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{OON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V		2100		270	2500		3200	Ω
			V_{DD} = 5V, V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V		330		120	400		520	Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V		230		80	280		360	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V				10				Ω
			V_{DD} = 5V V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V				10				Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5V, V_{EE} = −7.5V O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V V_{DD} = 7.5V, V_{EE} = −7.5V, O/I = 0V	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{ILL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1 kΩ to V_{SS} I_{IS} < 2μA on all OFF Channels V_{IS} = V_{DD} thru 1kΩ									
		V_{DD} = 5V			1.5			1.5		1.5	V
		V_{DD} = 10V			3.0			3.0		3.0	V
		V_{DD} = 15V			4.0			4.0		4.0	V
V_{IHH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15V, V_{EE} = 0V V_{IN} = 0V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{EE} = 0V V_{IN} = 15V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

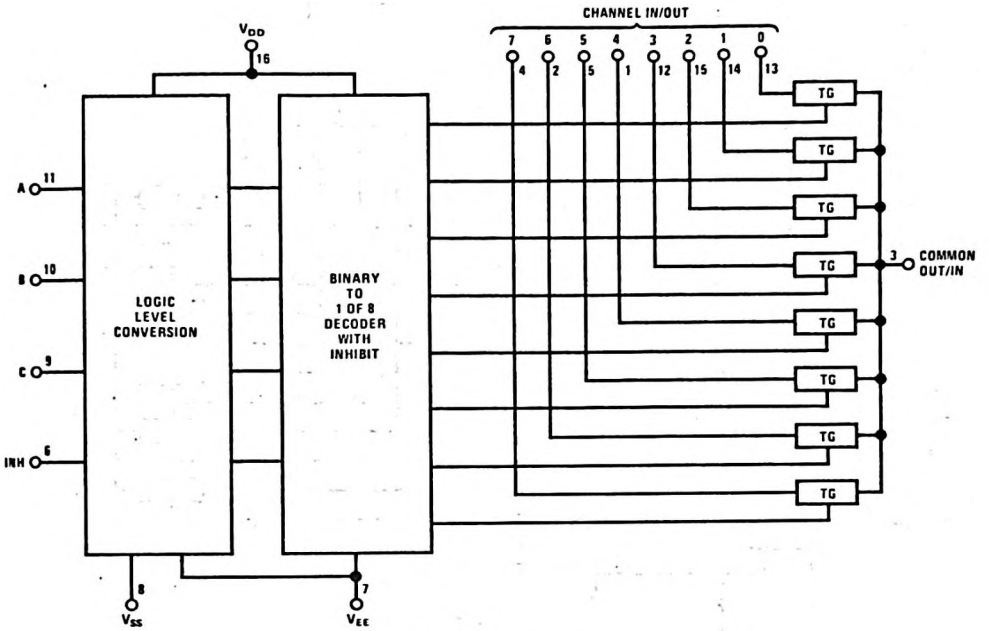
ac electrical characteristics

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

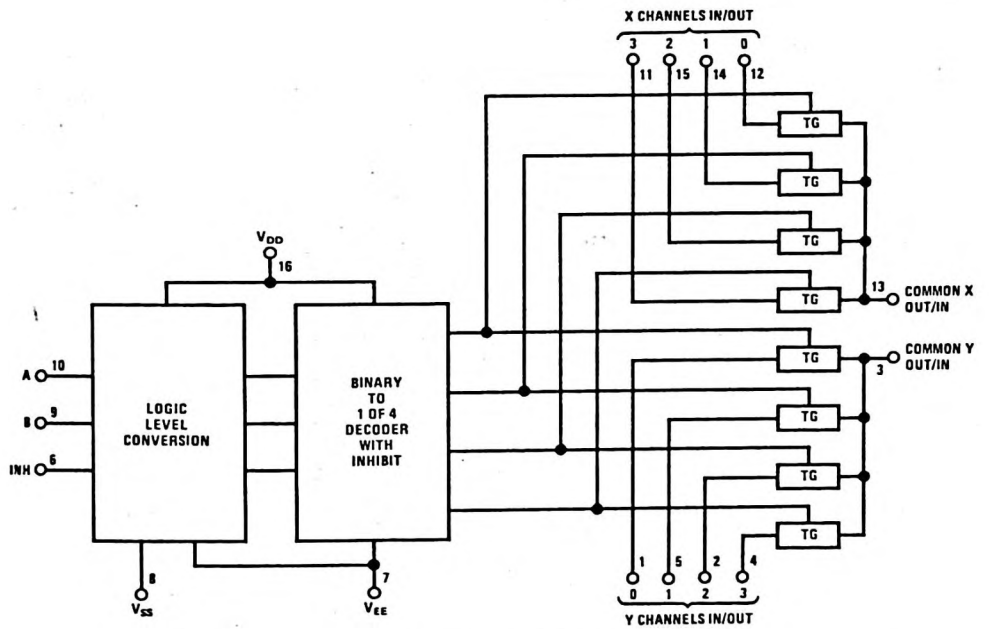
Parameter		Conditions	V_{pp}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		600 225 160	1200 450 320	ns ns ns
t_{PHZ} t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance Control Input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20\log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL}, t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		25 15 10	65 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

block diagrams

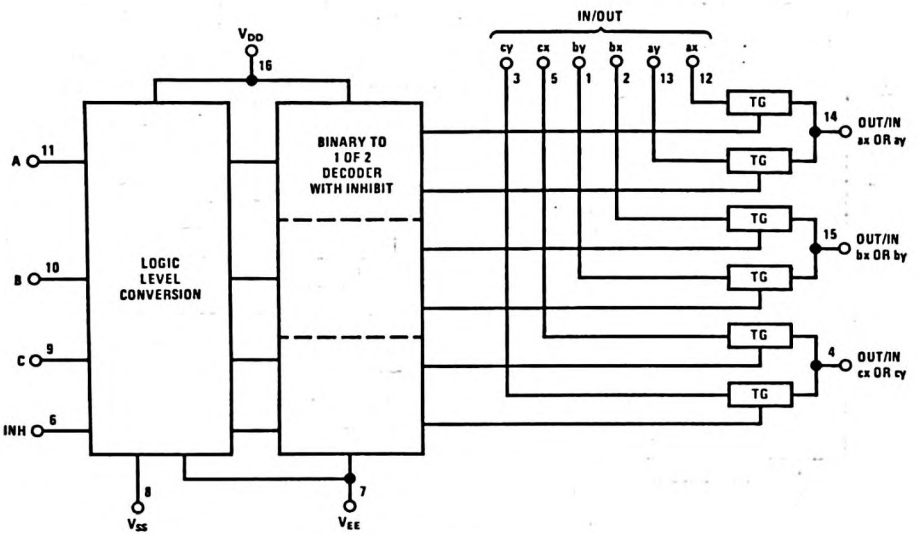


CD4051BM/CD4051BC



CD4052BM/CD4052BC

block diagram (cont)

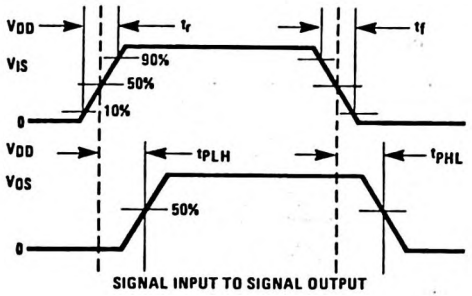


CD4053BM/CD4053BC

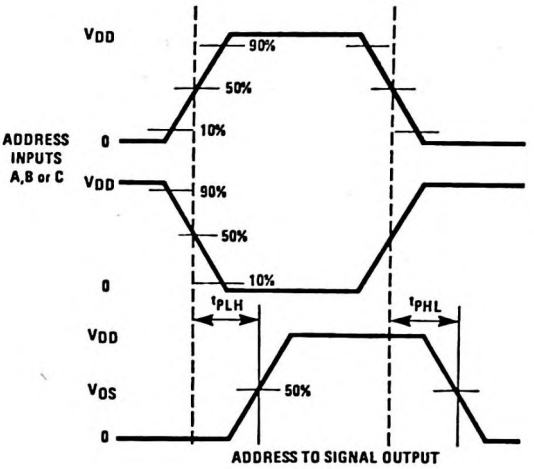
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don't Care condition.

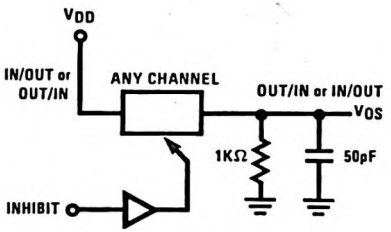
switching time waveforms

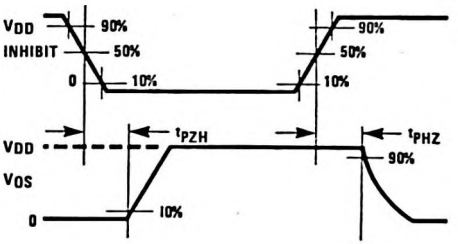


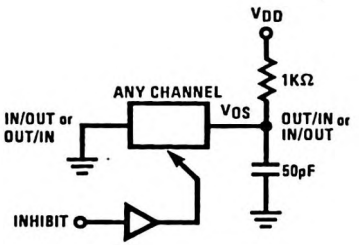
SIGNAL INPUT TO SIGNAL OUTPUT

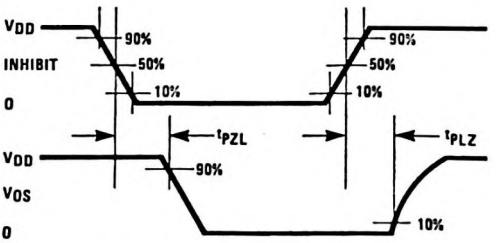


ADDRESS TO SIGNAL OUTPUT







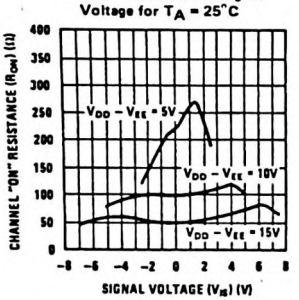


special considerations

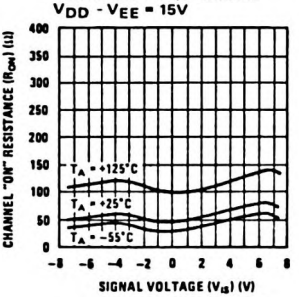
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6 V at $T_A \leq 25°C$, or 0.4 V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

typical performance characteristics

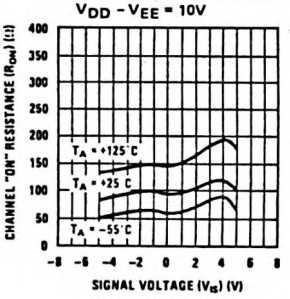
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



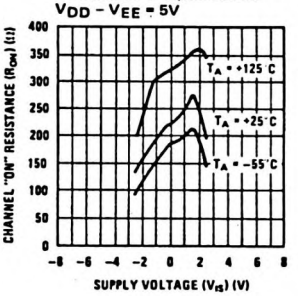
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

general description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

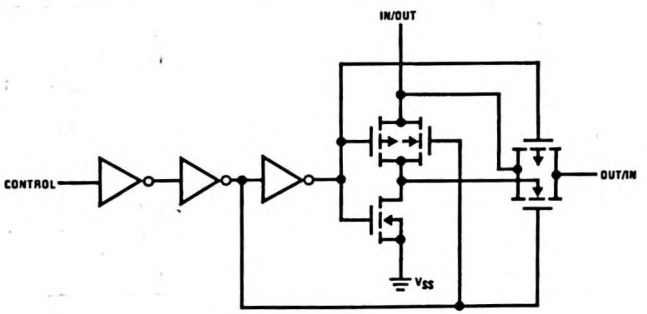
features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω typ
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity — < 0.4% distortion typ @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω typ
- Low crosstalk between switches — −50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz typ

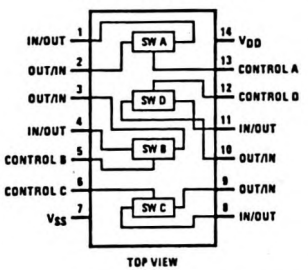
applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

schematic and connection diagrams



Dual-In-Line Package



Order Number CD4066BMD or CD4066BCD
See NS Package D14A

Order Number CD4066BMF or CD4066BCF
See NS Package F14A

Order Number CD4066BMJ or CD4066BCJ
See NS Package J14A

Order Number CD4066BMN or CD4066BCN
See NS Package N14A

Order Number CD4066BMW or CD4066BCW
See NS Package W14A

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

dc electrical characteristics CD4066BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
	V_{DD} = 10V		0.5		0.01	0.5		15	μA
	V_{DD} = 15V		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 5V		2000		270	2500		3500	Ω
	V_{DD} = 10V		400		120	500		550	Ω
	V_{DD} = 15V		220		80	280		320	Ω
ΔR_{ON} Δ "ON" Resistance Between any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 10V				10				Ω
	V_{DD} = 15V				5				Ω
I_{IS} Input or Output Leakage Switch "OFF"	V_C = 0		±50		±0.1	±50		±500	nA
	V_{IS} = 15V and 0V,								
	V_{OS} = 0V and 15V								
Control Inputs									
V_{ILC} Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD}								
	V_{OS} = V_{DD} and V_{SS}								
	I_{IS} = ±10μA								
	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC} High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN} Input Current	V_{DD} − V_{SS} = 15V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
	$V_{DD} \geq V_{IS} \geq V_{SS}$								
	$V_{DD} \geq V_C \geq V_{SS}$								

dc electrical characteristics CD4066BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
	V_{DD} = 10V		2.0		0.01	2.0		15	μA
	V_{DD} = 15V		4.0		0.01	4.0		30	μA

dc electrical characteristics (Continued) CD4066BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$								
	$V_C = V_{DD}$, V_{SS} to V_{DD}								
	$V_{DD} = 5V$		2000		270	2500		3200	Ω
	$V_{DD} = 10V$		450		120	500		520	Ω
	$V_{DD} = 15V$		250		80	280		300	Ω
ΔR_{ON} Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$								
	$V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
	$V_{DD} = 10V$				10				Ω
	$V_{DD} = 15V$				5				Ω
I_{IS} Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
Control Inputs									
V_{ILC} Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD}								
	$V_{OS} = V_{DD}$ and V_{SS}								
	$I_{IS} = \pm 10\mu A$								
	$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC} High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN} Input Current	$V_{DD} - V_{SS} = 15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
	$V_{DD} \geq V_{IS} \geq V_{SS}$								
	$V_{DD} \geq V_C \geq V_{SS}$								

ac electrical characteristics $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50$ pF, *(Figure 1)*				
		$R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$		0.4		%
		$R_L = 10\ k\Omega$, $V_{IS} = 5\ V_{p-p}$, $f = 1$ kHz, *(Figure 4)*				
	Frequency Response–Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$,		40		MHz
		$R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$,				
		$20\ \text{Log}_{10}\ V_{OS}/V_{OS}(1kHz)$–dB, *(Figure 4)*				

ac electrical characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\,k\Omega$, $V_{IS} = 5V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switch (Frequency at −50 dB)	$V_{DD} = V_{C(1)} = 5V$; $V_{SS} = V_{C(2)} = -5V$, $R_L = 1\,k\Omega$, $V_{IS(A)} = 5V_{p-p}$, 20 Log_{10} $V_{OS(2)}/V_{IS(1)} = -50$ dB, *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\,k\Omega$ $R_{IN} = 1\,k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$pF *(Figure 6)*		150		mV_{p-p}
	Maximum Control Input	$R_L = 1\,k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = \frac{1}{2}V_{OS(1kHz)}$				
		$V_{DD} = 5V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{is}	Signal Input Capacitance			8		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8		pF
C_{ios}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}:
a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OS} = standard B series I_{OL}

ac test circuits and switching time waveforms

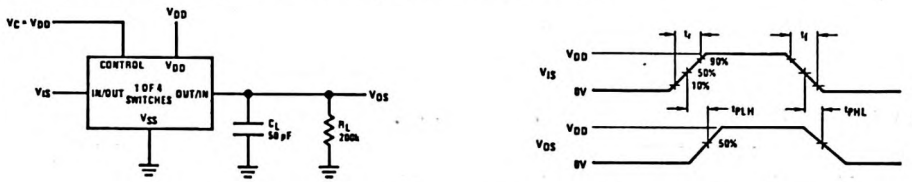


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

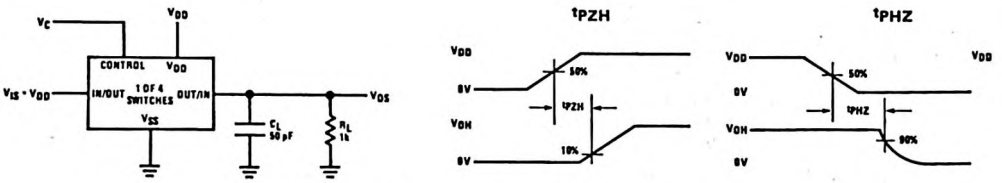


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

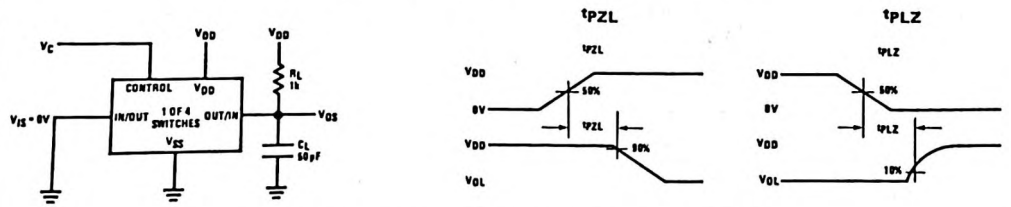


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

ac test circuits and switching time waveforms (Continued)

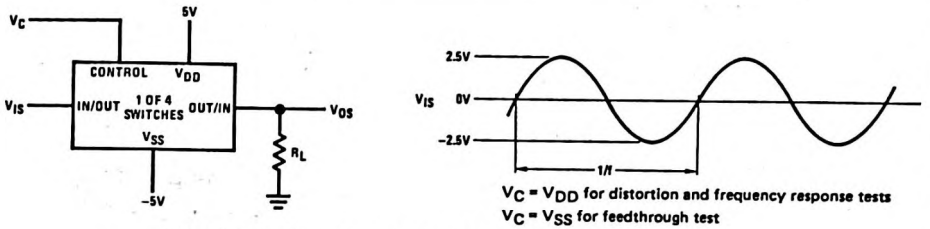


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

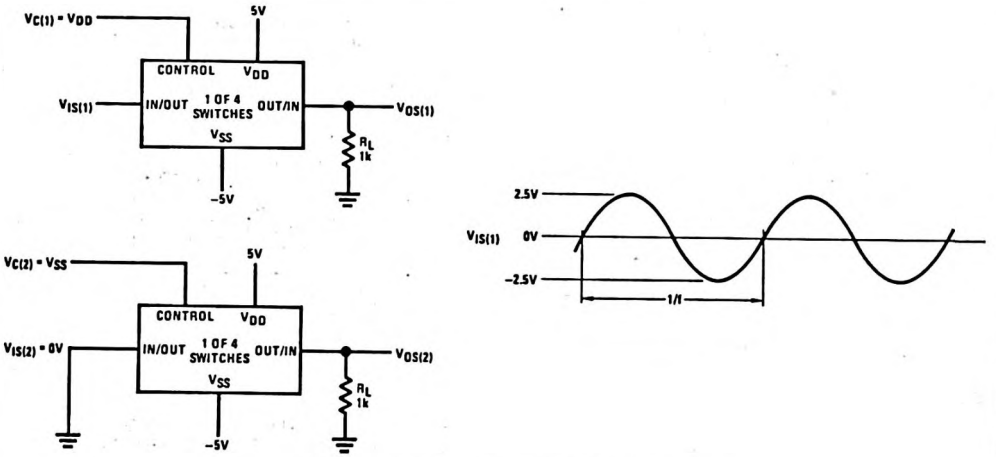


FIGURE 5. Crosstalk Between Any Two Switches

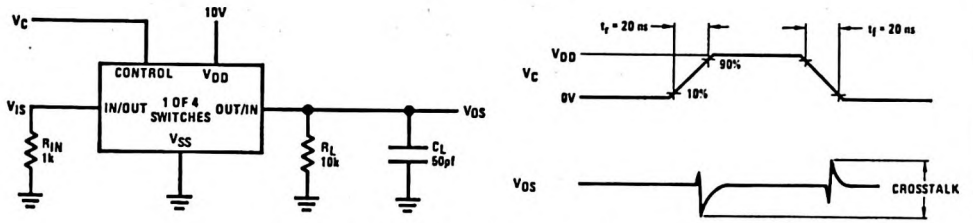


FIGURE 6. Crosstalk: Control Input to Signal Output

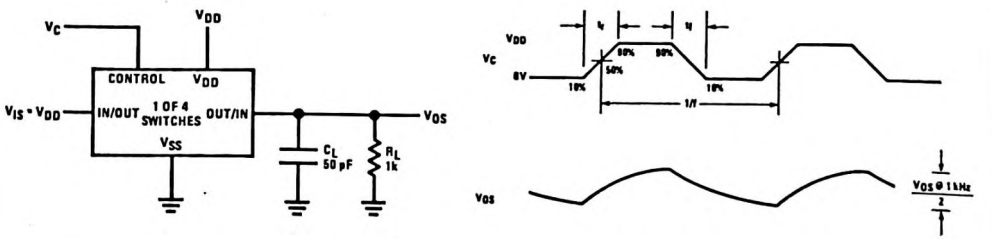
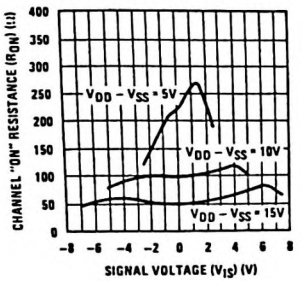


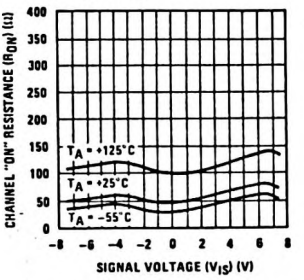
FIGURE 7. Maximum Control Input Frequency

typical performance characteristics

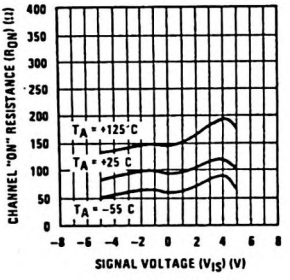
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



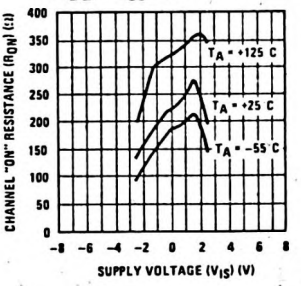
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



special considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

National Semiconductor

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

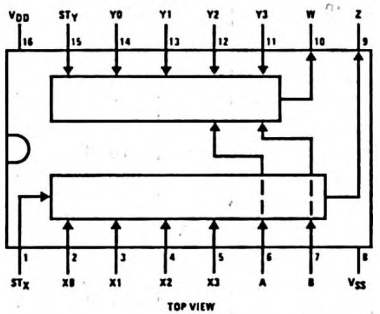
The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single binary to 1-of-8 decoder applications.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low quiescent power dissipation — 0.005 μW/package typical @ 5 V_{DC}
- 10 MHz frequency operation (typical)
- Data paths are bidirectional
- Linear ON resistance (120Ω typical @ 15V)
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

Connection Diagram

Dual-In-Line Package



TOP VIEW

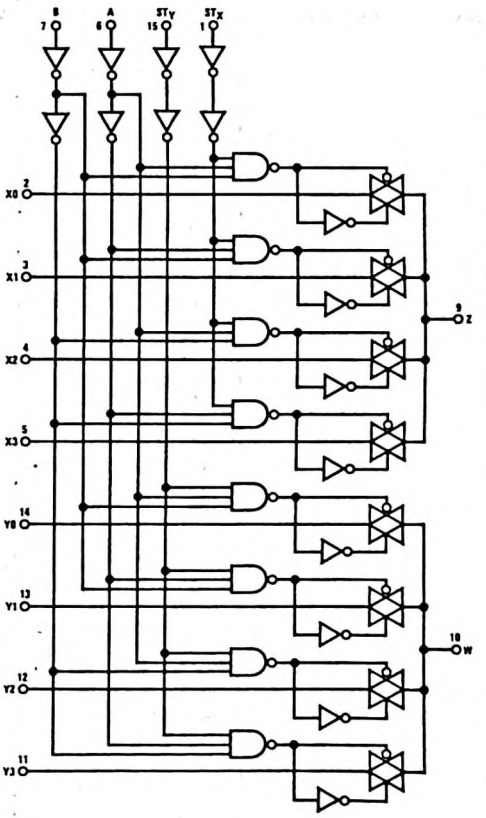
Order Number CD4529BMJ or CD4529BCJ
See NS Package J16A
Order Number CD4529BMN or CD4529BCN
See NS Package N16A

Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE®)		

X = Don't care

Logic Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	-0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	μA
		V_{DD} = 10V		1.0		0.002	1.0		60	μA
		V_{DD} = 15V		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Switch OFF is defined as $|I_O| \leq 10\ \mu A$, switch ON as defined by R_{ON} specification.

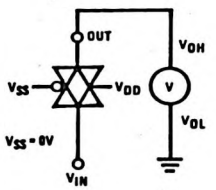
AC Electrical Characteristics CD4529BM/CD4529BC

$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

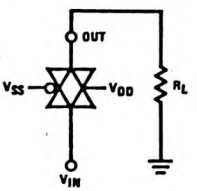
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF, $V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	$f = 100$ Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		$f = 100$ kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, $f = 1$ kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss, $I_{LOSS} = 20\ Log_{10} \frac{V_{OUT}}{V_{IN}}$	$V_{IN} = 1.77$Vrms Centered at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, −3 dB	$V_{IN} = 1.77$Vrms Centered at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk, $20\ Log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ dB	$V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			kHz

Test Circuits and Switching Time Waveforms

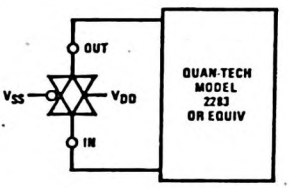
Output Voltage



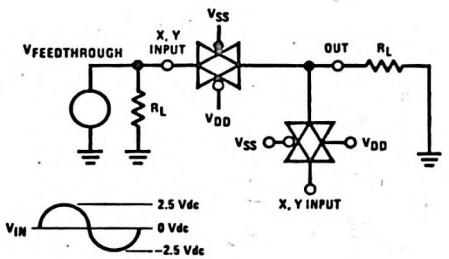
R_{ON} Characteristics



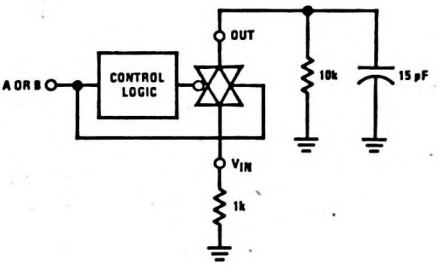
Noise Voltage



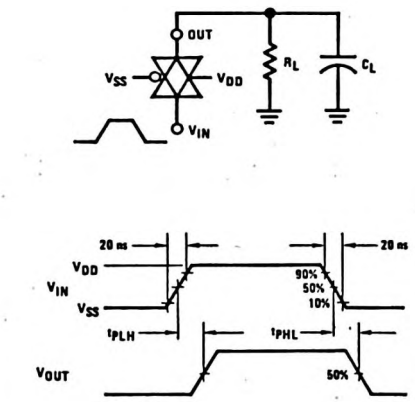
Frequency Response



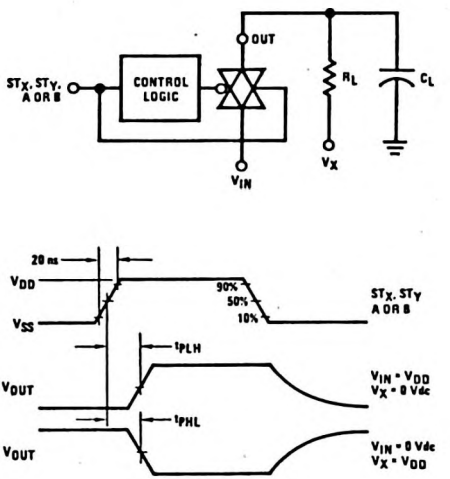
Crosstalk



Propagation Delay

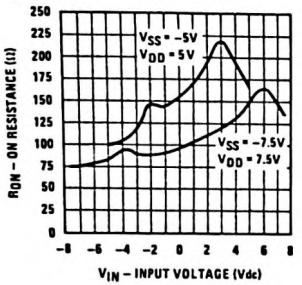


Turn-ON Delay Time

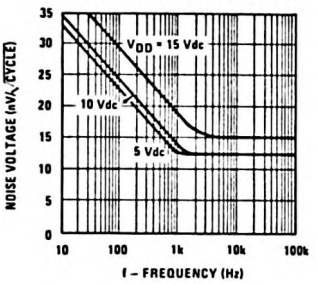


Typical Performance Characteristics

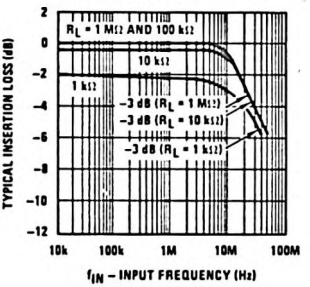
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics

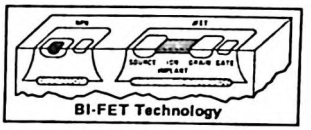


Typical Insertion Loss/ Bandwidth Characteristics



National Semiconductor

Analog Switches/Multiplexers



Quad SPST JFET Analog Switches

LF11331/LF12331/LF13331	4 normally open switches with disable
LF11332/LF12332/LF13332	4 normally closed switches with disable
LF11333/LF12333/LF13333	2 normally closed switches and 2 normally open switches with disable
LF11201/LF12201/LF13201	4 normally closed switches
LF11202/LF12202/LF13202	4 normally open switches

general description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

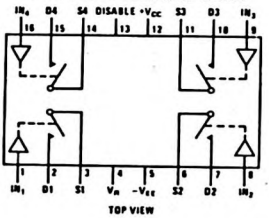
features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advan tage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

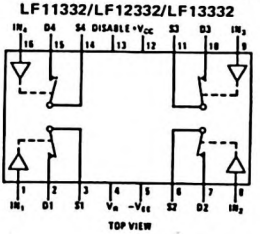
These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

connection diagrams (Dual-In-Line Packages) (All Switches Shown are For Logical "0")

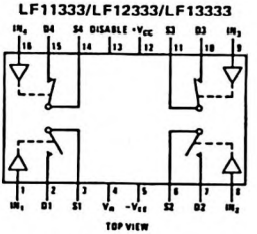
LF11331/LF12331/LF13331



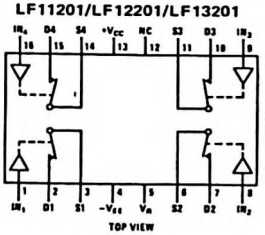
LF11332/LF12332/LF13332



LF11333/LF12333/LF13333



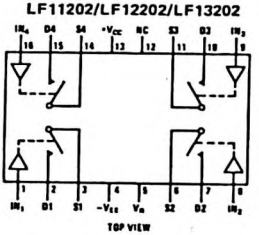
LF11201/LF12201/LF13201



Order Number LF11201D, LF12201D, LF13201D, LF11202D, LF12202D, LF13202D, LF11331D, LF12331D, LF13331D, LF11332D, LF12332D, LF13332D, LF11333D, LF12333D or LF13333D
See NS Package D16C

Order Number LF12201N, LF13201N, LF12202N, LF13202N, LF12331N, LF13331N, LF12332N, LF13332N, LF12333N or LF13333N
See NS Package N16A

LF11202/LF12202/LF13202



test circuit and schematic diagram

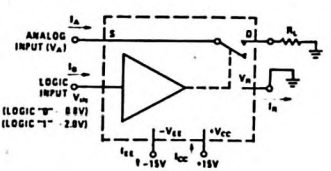


FIGURE 1. Typical Circuit for One Switch

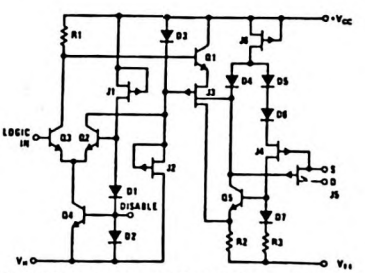


FIGURE 2. Schematic Diagram (Normally Open)

absolute maximum ratings

Positive Supply – Negative Supply (V_{CC}–V_{EE}) 36V
Reference Voltage $V_{EE} \leq V_R \leq V_{CC}$
Logic Input Voltage V_R –4.0V $\leq V_{IN} \leq V_R$ +6.0V
Analog Voltage $V_{EE} \leq V_A \leq V_{CC}$ +6V; $V_A \leq V_{EE}$ +36V
Analog Current $|I_A| < 20$ mA
Power Dissipation (Note 1)
- Molded DIP (N Suffix) 500 mW
- Cavity DIP (D Suffix) 900 mW

Operating Temperature Range
- LF11201, 2 and LF11331, 2, 3 –55°C to +125°C
- LF12201, 2 and LF12331, 2, 3 –25°C to +85°C
- LF13201, 2 and LF13331, 2, 3 0°C to +70°C

Storage Temperature –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

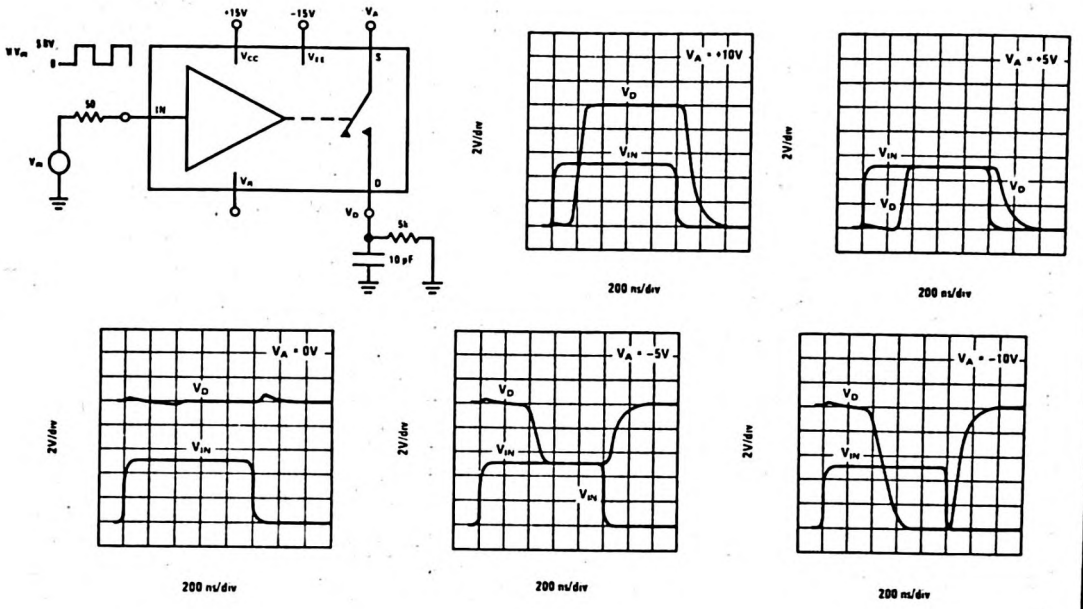
electrical characteristics (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		LF11331/2/3 LF11201/2			LF12331/2/3 LF12201/2 LF13331/2/3 LF13201/2			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	V_A = 0, I_D = 1 mA	T_A = 25°C		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		T_A = 25°C		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," V_S = V_D = ±10V	T_A = 25°C		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	V_{IN} = 5V	T_A = 25°C		3.6	10		3.6	40	µA
						25			100	µA
I_{INL}	Logical "0" Input Current	V_{IN} = 0.8	T_A = 25°C			0.1			0.1	µA
						1			1	µA
t_{ON}	Delay Time "ON"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		500			500		ns
t_{OFF}	Delay Time "OFF"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		90			90		ns
$t_{ON} - t_{OFF}$	Break-Before-Make	V_S = ±10V, *(Figure 3)*	T_A = 25°C		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," V_S = ±10V	T_A = 25°C		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," V_D = ±10V	T_A = 25°C		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," V_S = V_D = 0V	T_A = 25°C		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 3)	T_A = 25°C		–50			–50		dB
CT	Crosstalk	*(Figure 4)*, (Note 3)	T_A = 25°C		–65			–65		dB
SR	Analog Slew Rate	(Note 4)	T_A = 25°C		50			50		V/µs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 5)	T_A = 25°C		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.
Note 2: Unless otherwise specified, V_{CC} = +15V, V_{EE} = –15V, V_R = 0V, and limits apply for –55°C $\leq T_A \leq$ +125°C for the LF11331,2,3 and the LF11201,2, –25°C $\leq T_A \leq$ +85°C for the LF12331,2,3 and the LF12201,2, and 0°C $\leq T_A \leq$ +70°C for the LF13331,2,3 and the LF13201, 2.
Note 3: These parameters are limited by the pin to pin capacitance of the package.
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.
Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay times will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.
Note 6: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

test circuit and typical performance curves

Delay Time, Rise Time, Settling Time, and Switching Transients



additional test circuits

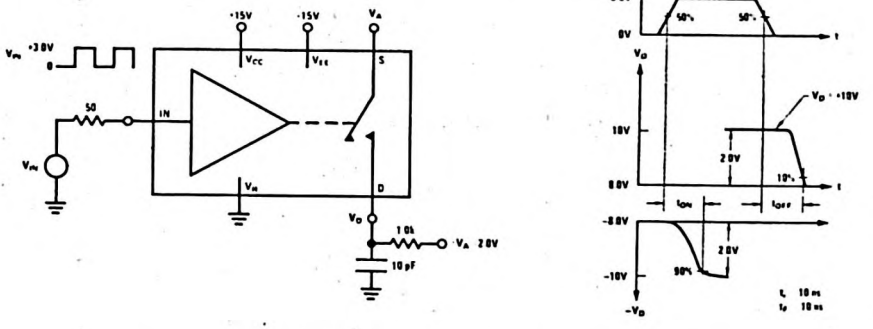


FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

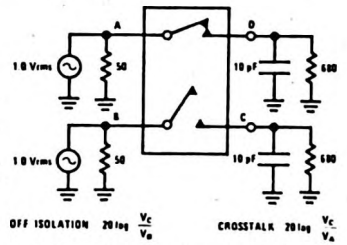
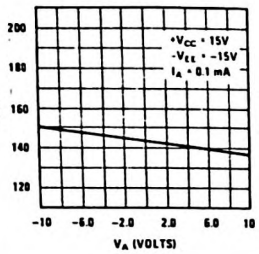


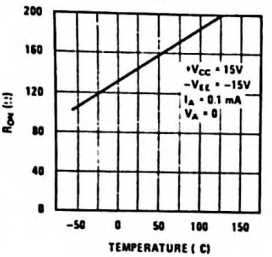
FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

typical performance characteristics

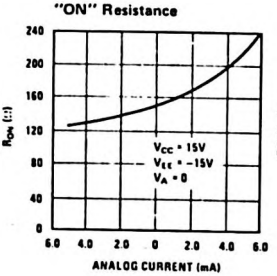
"ON" Resistance



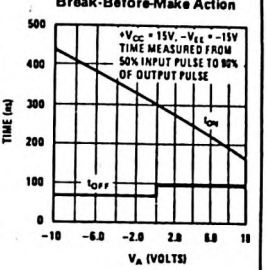
"ON" Resistance



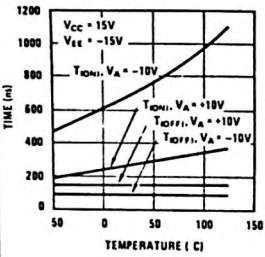
"ON" Resistance



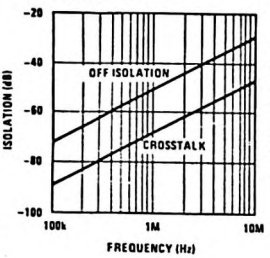
Break-Before-Make Action



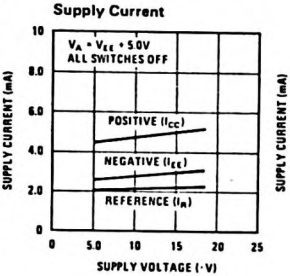
Switching Times



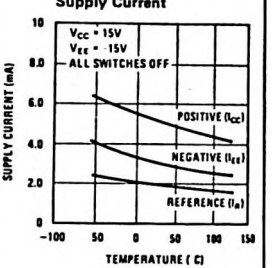
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



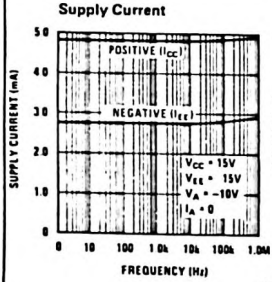
Supply Current



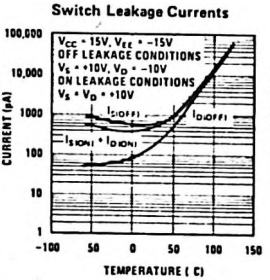
Supply Current



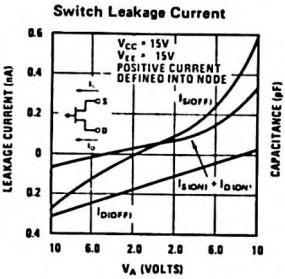
Supply Current



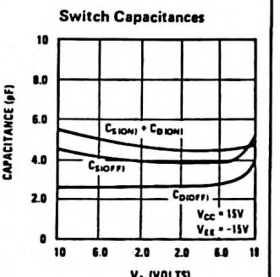
Switch Leakage Currents



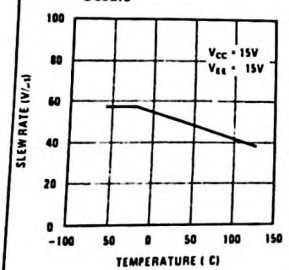
Switch Leakage Current



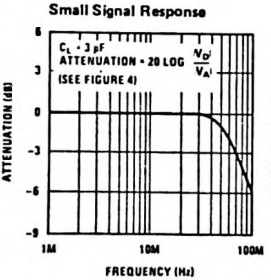
Switch Capacitances



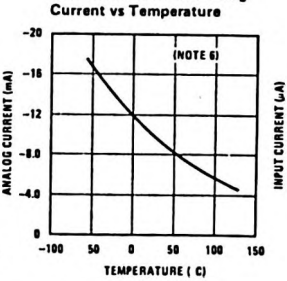
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



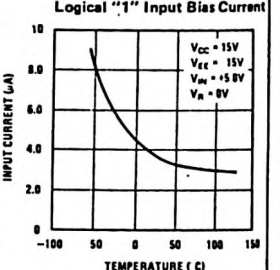
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



application hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than (V_{CC} − 2.5V). If the input voltage is greater than (V_{CC} − 2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from (V_{EE} + 5V) to (V_{CC} − 5V). For analog voltages greater than (V_{CC} − 5V), the switch will remain ON independent of the logic input voltage. For analog voltages less than (V_{EE} + 5V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as (V_{CC} − 36V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC} - V_A$) decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to (V_{CC} − 4.5V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an interal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5*, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈ 0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

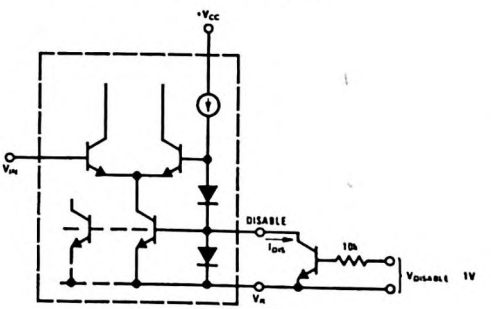
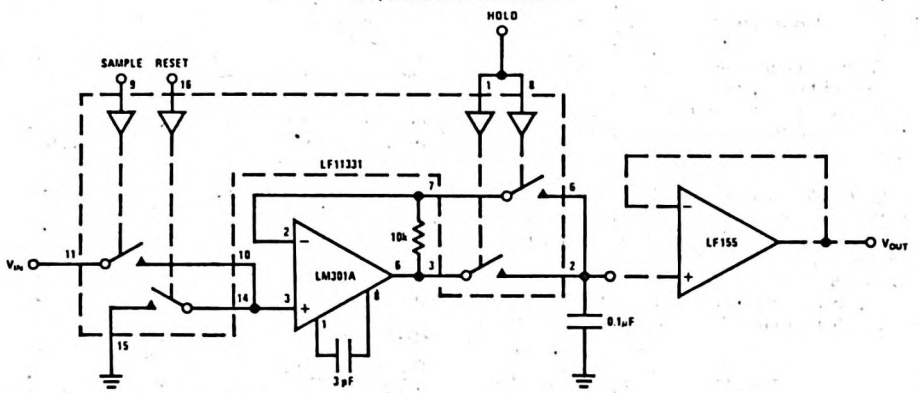


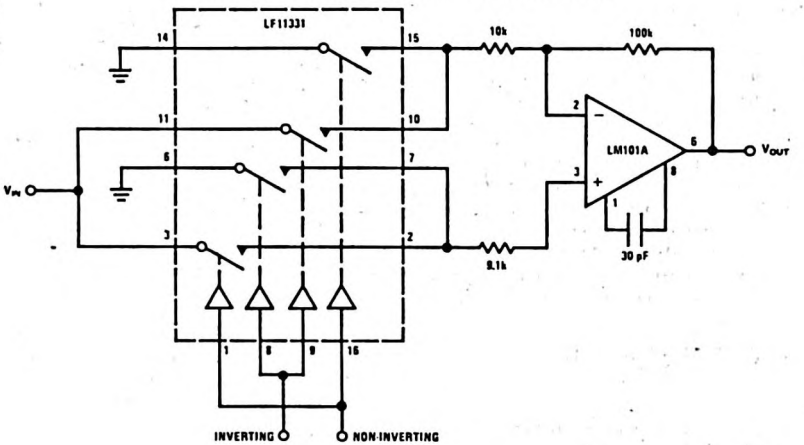
FIGURE 5. Disable Function

typical applications

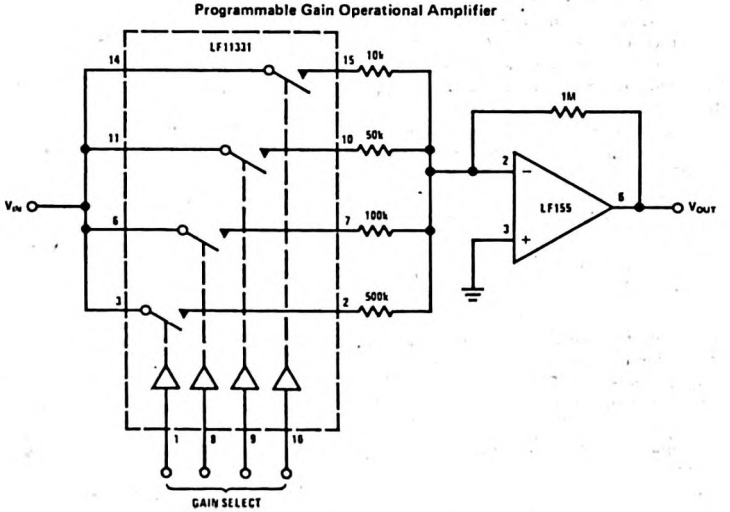
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier

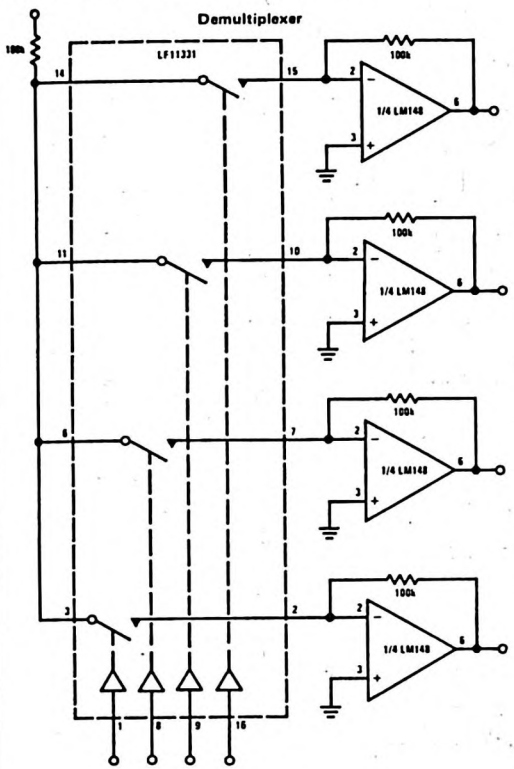


Programmable Gain Operational Amplifier

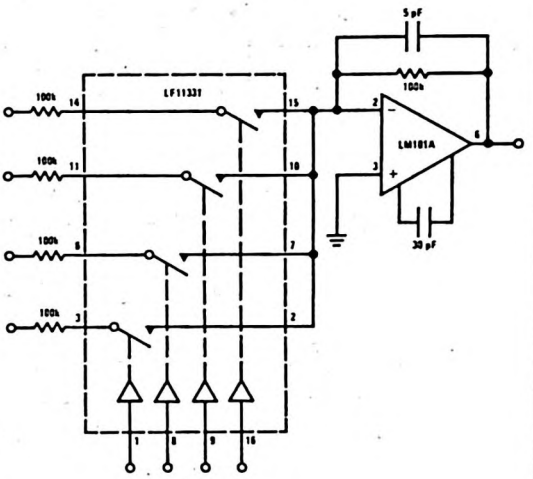


typical applications (con't)

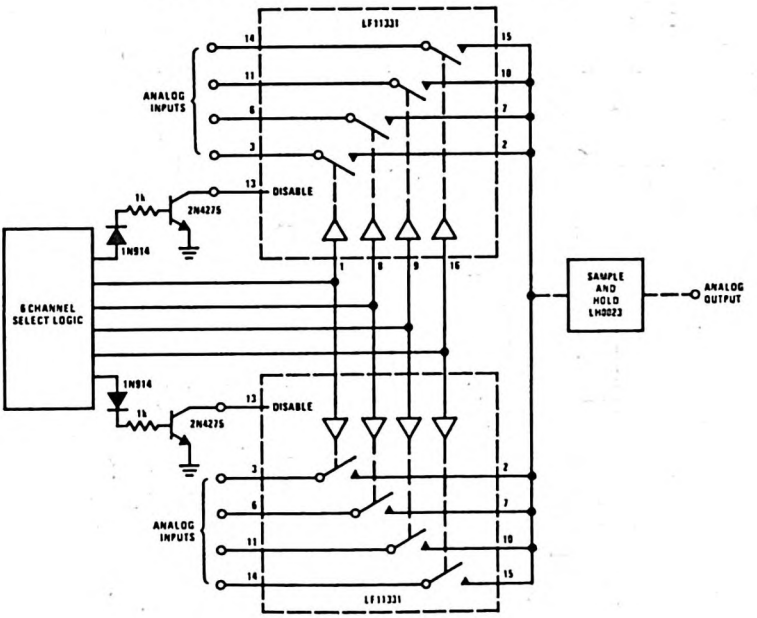
Demultiplexer



Multiplexer/Mixer

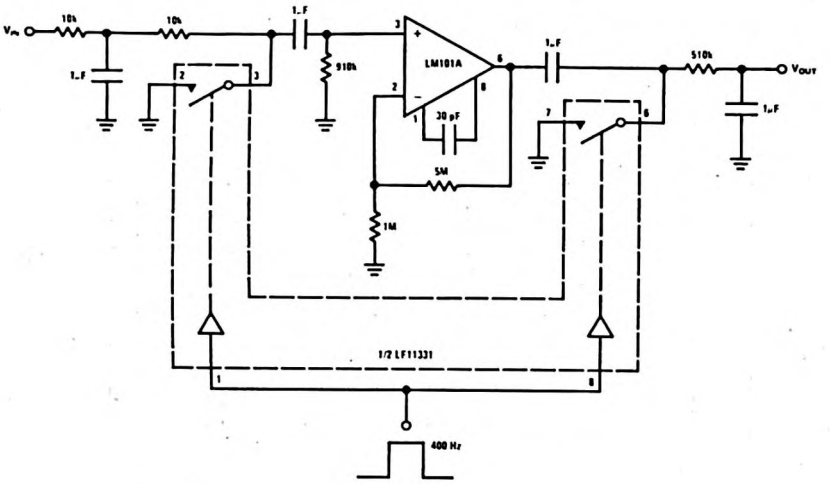


8-Channel Analog Commutator with 6-Channel Select Logic

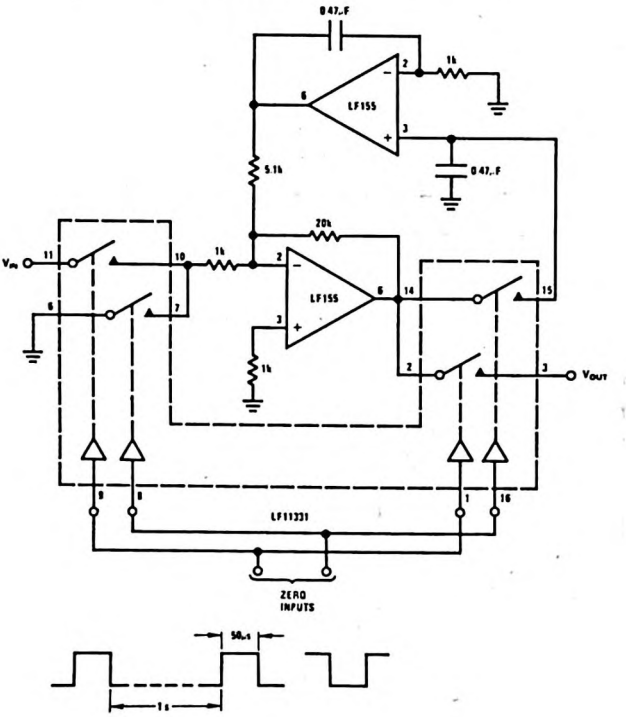


typical applications (con't)

Chopper Channel Amplifier

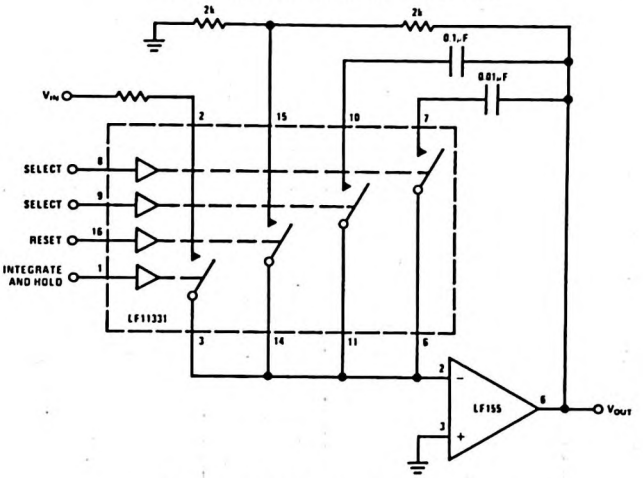


Self-Zeroing Operational Amplifier

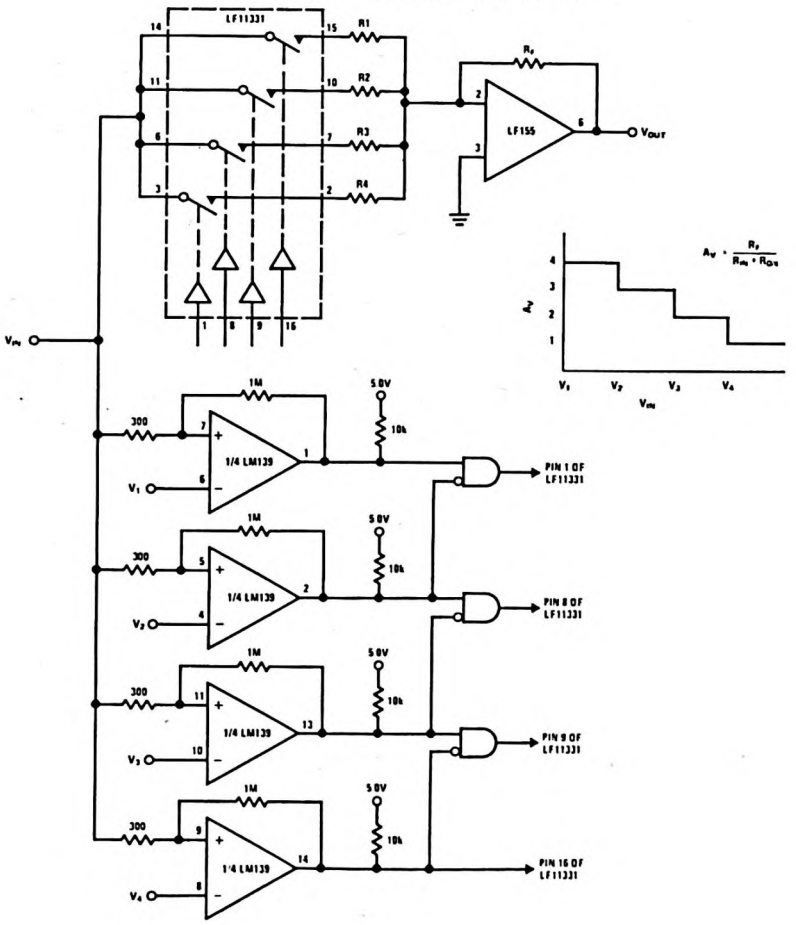


typical applications (con't)

Programmable Integrator with Reset and Hold

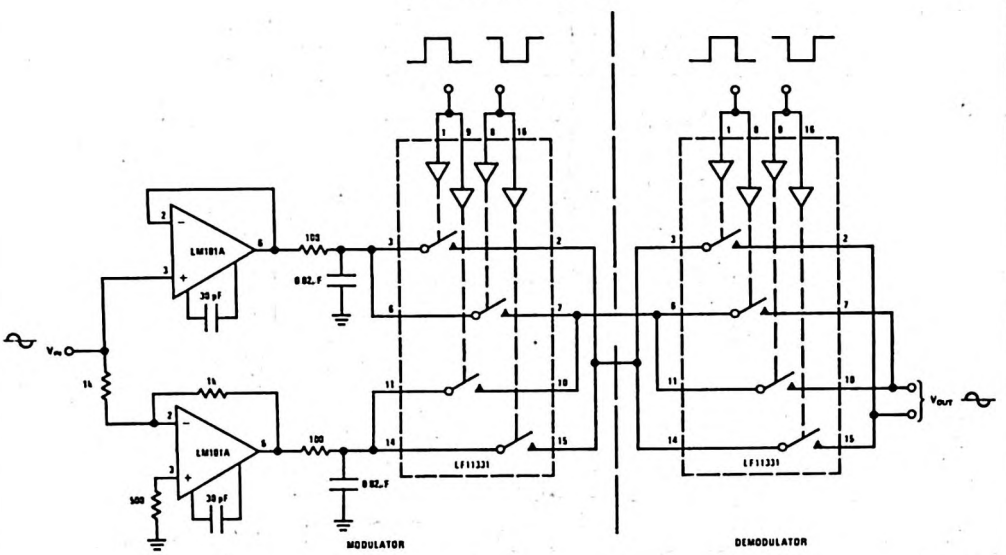


Staircase Transfer Function Operational Amplifier



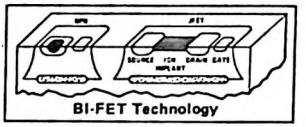
typical applications (con't)

DSB Modulator-Demodulator



National Semiconductor

Analog Switches/Multiplexers



LF11508/LF12508/LF13508 8-Channel Analog Multiplexer
LF11509/LF12509/LF13509 4-Channel Differential Analog Multiplexer

general description

The LF11508/LF12508/LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

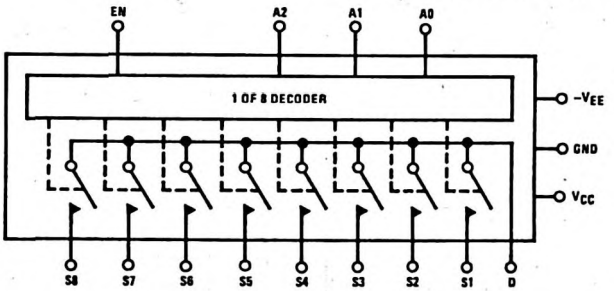
The LF11509/LF12509/LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF11508 series and should be used whenever differential analog inputs are required.

features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: t_{OFF} = 0.2 μs; t_{ON} = 2 μs typ
- Lower leakage devices available

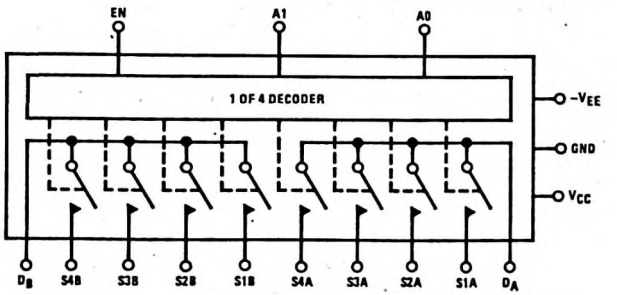
functional diagrams and truth tables

LF11508/LF12508/LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF11509/LF12509/LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

absolute maximum ratings

	LF11508, LF11509	LF12508, LF12509	LF13508, LF13509
Positive Supply – Negative Supply ($V_{CC} - V_{EE}$)	36V	36V	36V
Positive Analog Input Voltage (Note 1)	V_{CC}	V_{CC}	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$	$-V_{EE}$	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}	V_{CC}	V_{CC}
Negative Digital Input Voltage	−5V	−5V	−5V
Analog Switch Current	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_D	–	–	500 mW
θ_{jA}	–	–	150°C/W
Cavity DIP (D) P_D	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

electrical characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LF11508, LF11509			LF12508, LF12509, LF13508, LF13509			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	$V_{OUT} = 0V$, $I_S = 100\,\mu A$	$T_A = 25°C$		380	500		380	650	Ω
					600	750		500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \le V_{OUT} \le +10V$, $I_S = 100\,\mu A$	$T_A = 25°C$		0.01	1		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	$V_{OUT} = 0V$, $I_S = 100\,\mu A$	$T_A = 25°C$		20	100		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", $V_S = 11$, $V_D = -11$, (Note 4)	$T_A = 25°C$			1			5	nA
					10	50		0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", $V_S = 11$, $V_D = -11$, (Note 4)	$T_A = 25°C$			10			20	nA
					25	500		0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" $V_D = 11V$, (Note 4)	$T_A = 25°C$			10			20	nA
					35	500		1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7			0.7	V
I_{INL}	Digital "0" Input Current	$V_{IN} = 0.7V$	$T_A = 25°C$		1.5	20		1.5	30	μA
						40			40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	$V_{EN} = 0.7V$	$T_A = 25°C$		1.2	20		1.2	30	μA
						40			40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	$T_A = 25°C$		2.0	3		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	$T_A = 25°C$		1.6			1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	$T_A = 25°C$		1.6			1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	$T_A = 25°C$		0.2			0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	$T_A = 25°C$		−66			−66		dB
CT	Crosstalk	LF11509 Series, (Note 6)	$T_A = 25°C$		−66			−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", $V_{OUT} = 0V$, $V_S = 0V$	$T_A = 25°C$		2.2			2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", $V_{OUT} = 0V$, $V_S = 0V$	$T_A = 25°C$		11.4			11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	$T_A = 25°C$		7.4	10		7.4	12	mA
					9.2	13		7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	$T_A = 25°C$		2.7	4.5		2.7	5	mA
					2.9	5.5		2.8	6	mA

notes

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

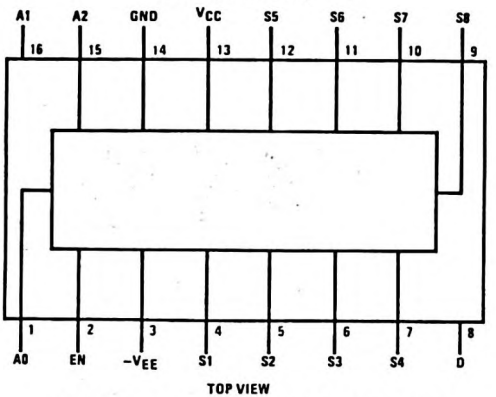
Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L = 200$, $C_L = 7$ pF, $V_S = 3$ Vrms, f = 500 kHz.

connection diagrams

LF11508/LF12508/LF13508
Dual-In-Line Package

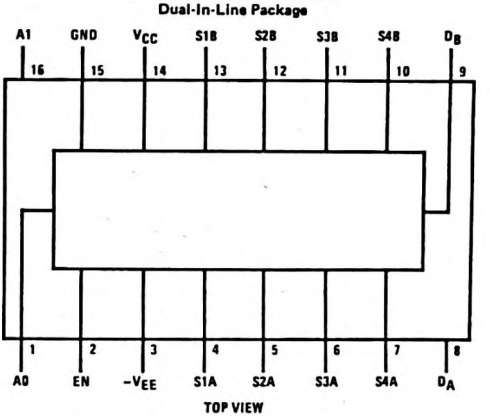


TOP VIEW

Order Number LF11508D, LF12508D or LF13508D
See NS Package D16A

Order Number LF13508N
See NS Package N16A

LF11509/LF12509/LF13509
Dual-In-Line Package

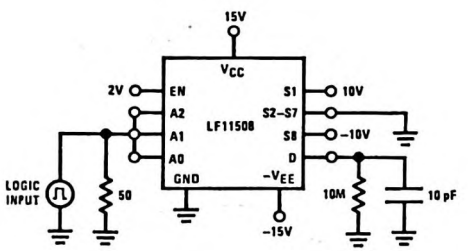


TOP VIEW

Order Number LF11509D, LF12509D or LF13509D
See NS Package D16A

Order Number LF13509N
See NS Package N16A

ac test circuits and switching time waveforms



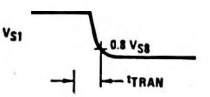
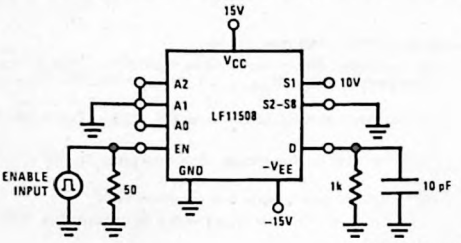


FIGURE 1. Transition Time

ac test circuits and switching time waveforms (Continued)



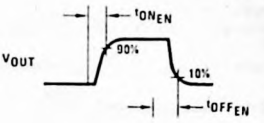
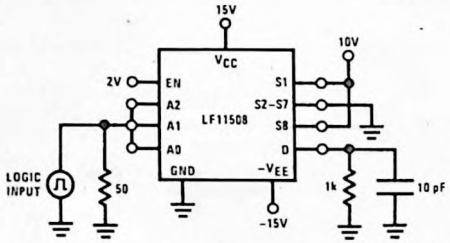


FIGURE 2. Enable Times



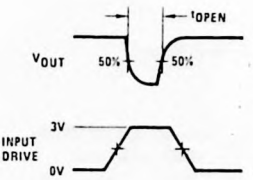
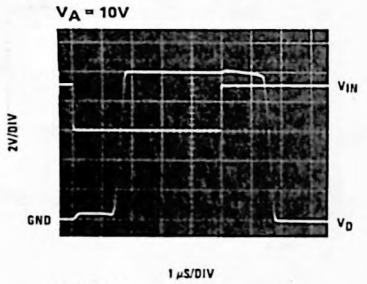
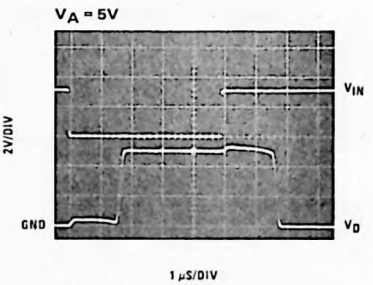
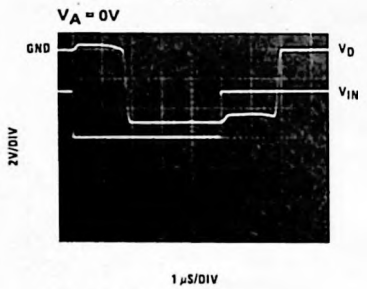


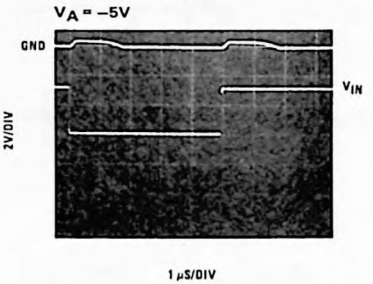
FIGURE 3. Break-Before-Make

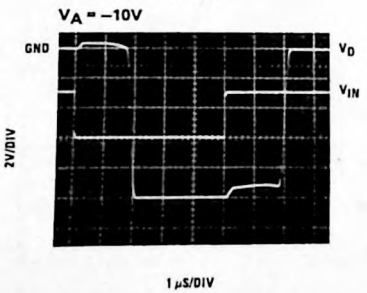
transition times and transients

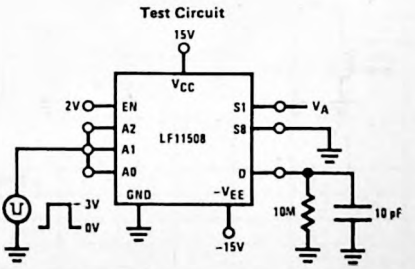






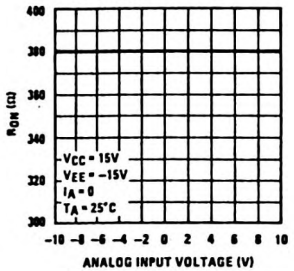




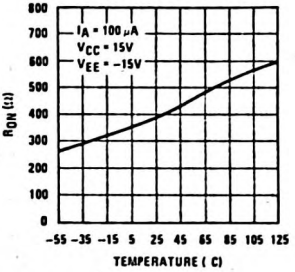


typical performance characteristics

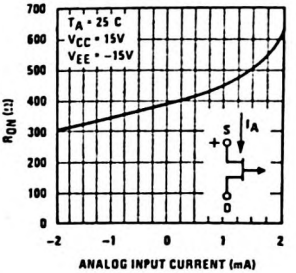
"ON" Resistance



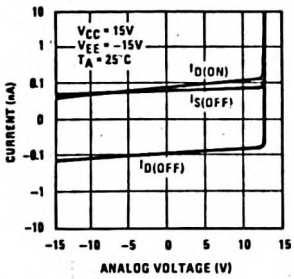
"ON" Resistance



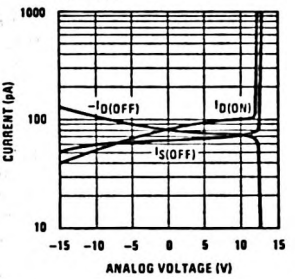
"ON" Resistance



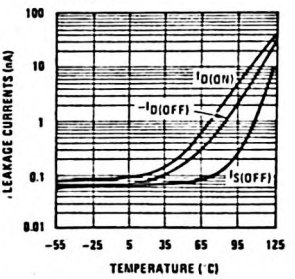
Switch Leakage Currents



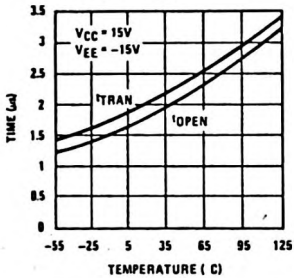
Switch Leakage Currents



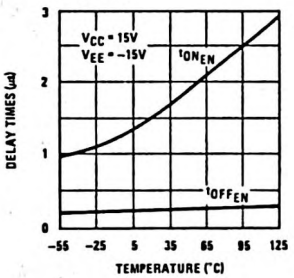
Switch Leakage Currents



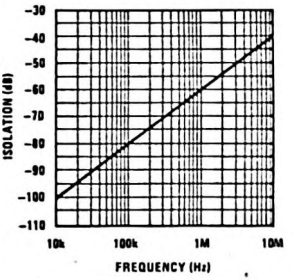
Switching Times (Figures 1 and 3)



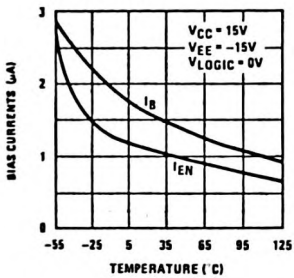
Enable Delay Times (Figure 2)



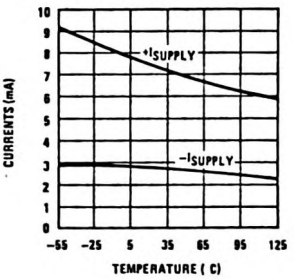
"OFF" Isolation and Crosstalk



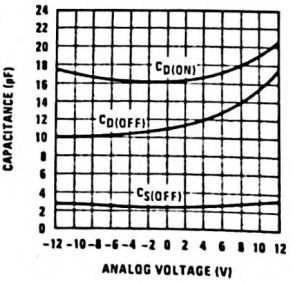
Bias Currents



Supply Currents



Switch Capacitances



application hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is ±0.4V over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE} + 36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference (≈ 2.1V). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction ($< 0.1\ \mu A$).

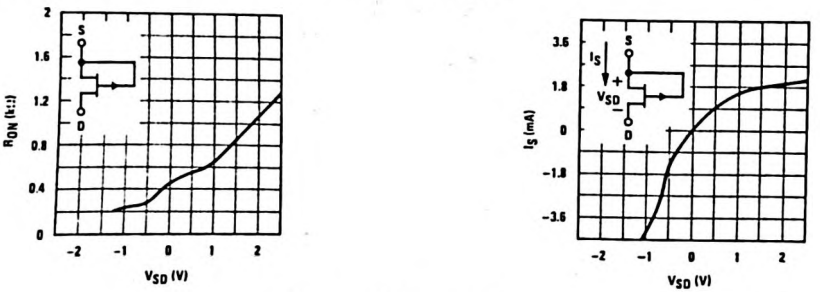


FIGURE 4. JFET Characteristics

typical applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multichannel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6).*

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

   $$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})}$$ where:

   R_{IN} = following stage input impedance

   ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

   Example: Let R_{ON} = 450 Ω, ΔR_{ON} = 0, R_S = 0, T_A = 25°C and allowable E = 0.01% which is equivalent to 1/2 LSB in a 12-bit system:

   $$R_{IN}\Big|_{min} = \frac{R_{ON}\,(100-E)}{E} = 4.5\ M\Omega$$

   Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

   t_s(ON): is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

   C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	t_s(ON) TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$t = C_S\,(R_{ON} + R_S) \| R_{IN}$

t_s(OFF): is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case doubling of the t_s(ON).

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:

   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

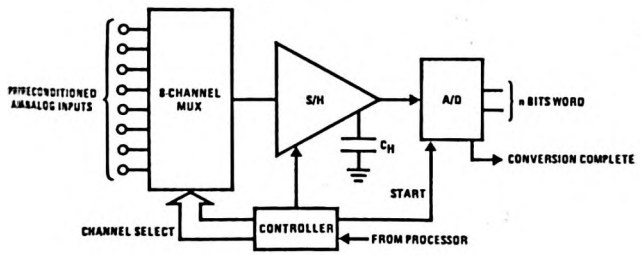


FIGURE 5. Random-Addressed, Multiplexed DAU

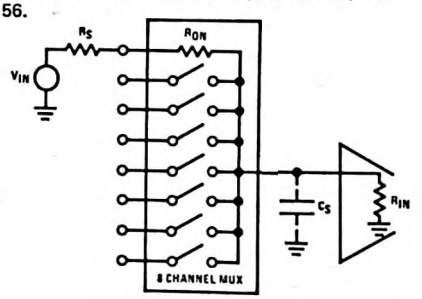


FIGURE 6. 8-Channel MUX

typical applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let $T_C = 40\ \mu s$ (MM4357), $V_{FS} = 10V$ and $n = 8$.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1\ mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_C + T_{MUX})} = 3k\ \text{samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})_{max}}{\pi\ V_{p\text{-}p}}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

The system speed can be improved by using the S/H shown in *Figure 5.* This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: $T_C = 40\ \mu s$, $T_A = 0.5\ \mu s$, $n = 8$: $T_C/T_A = 80$

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_A + T_{aq} + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5\ mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (5 + 40)\ 10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8.*

typical applications (Continued)

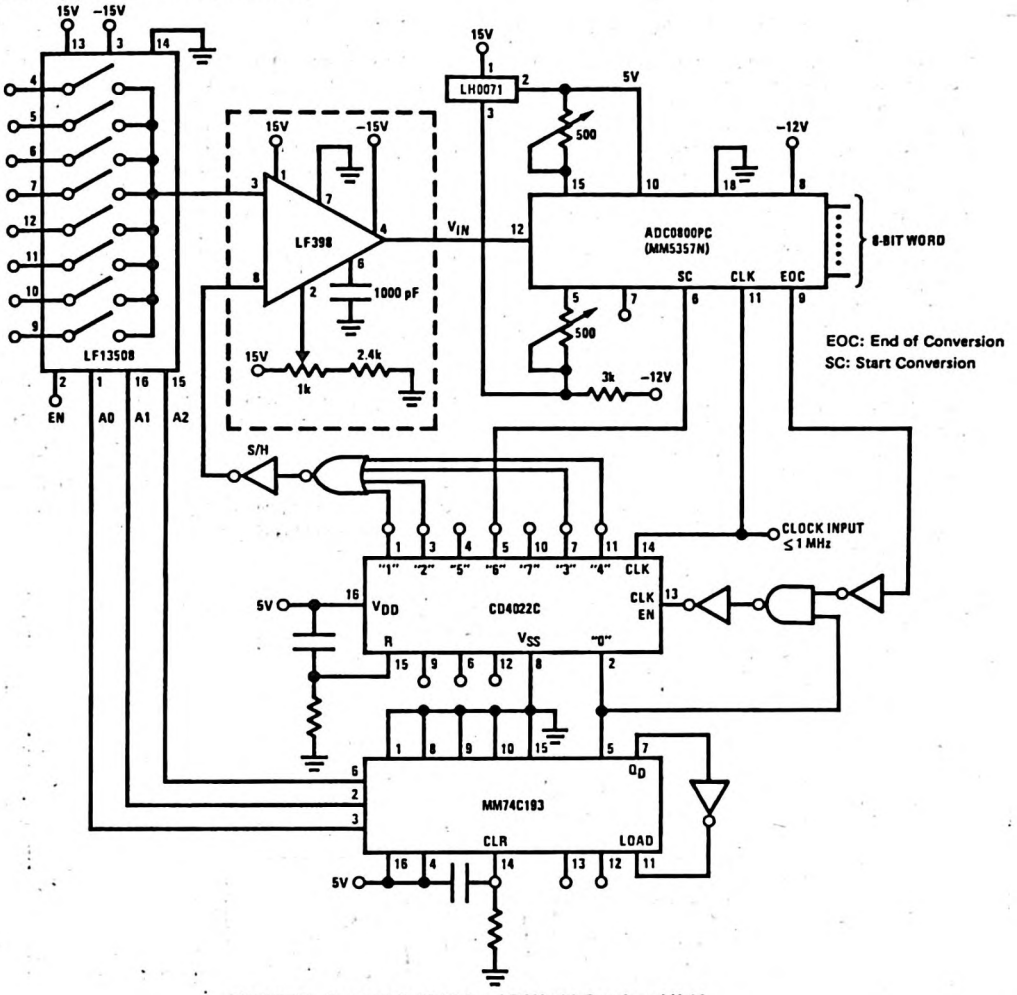


FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

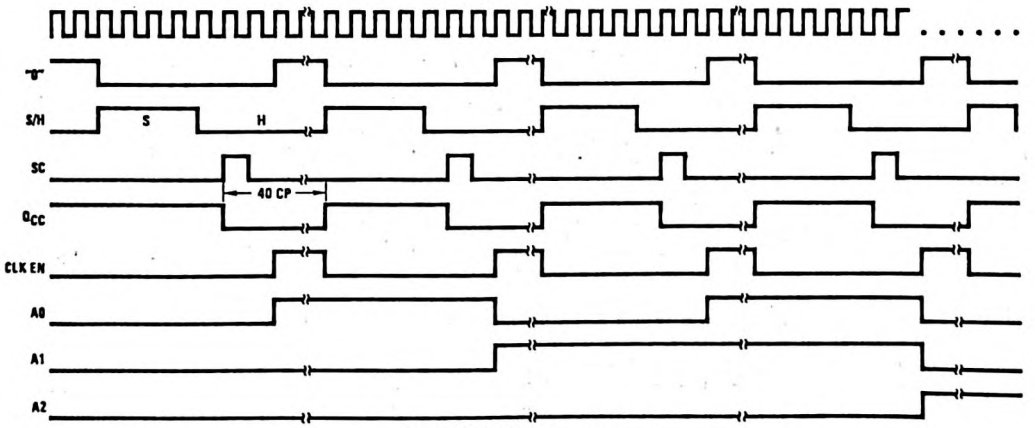


FIGURE 7b. Timing Diagram

typical applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9.* A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. } R = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

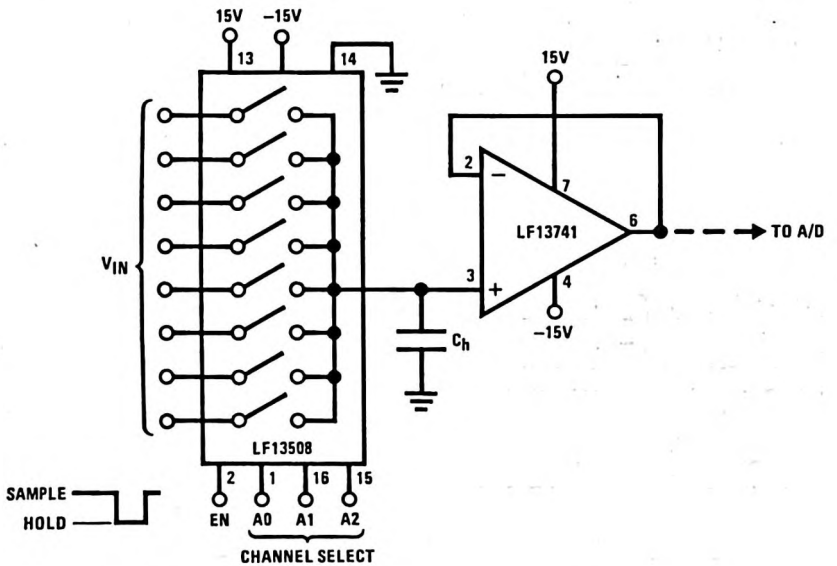
and

$$\left|\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\ \mu s} = 19.5\ \text{mV}/\mu\text{s for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10*, where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_s(ON)$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12*.



- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40\ k\Omega$
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \simeq 10\ pF\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

typical applications (Continued)

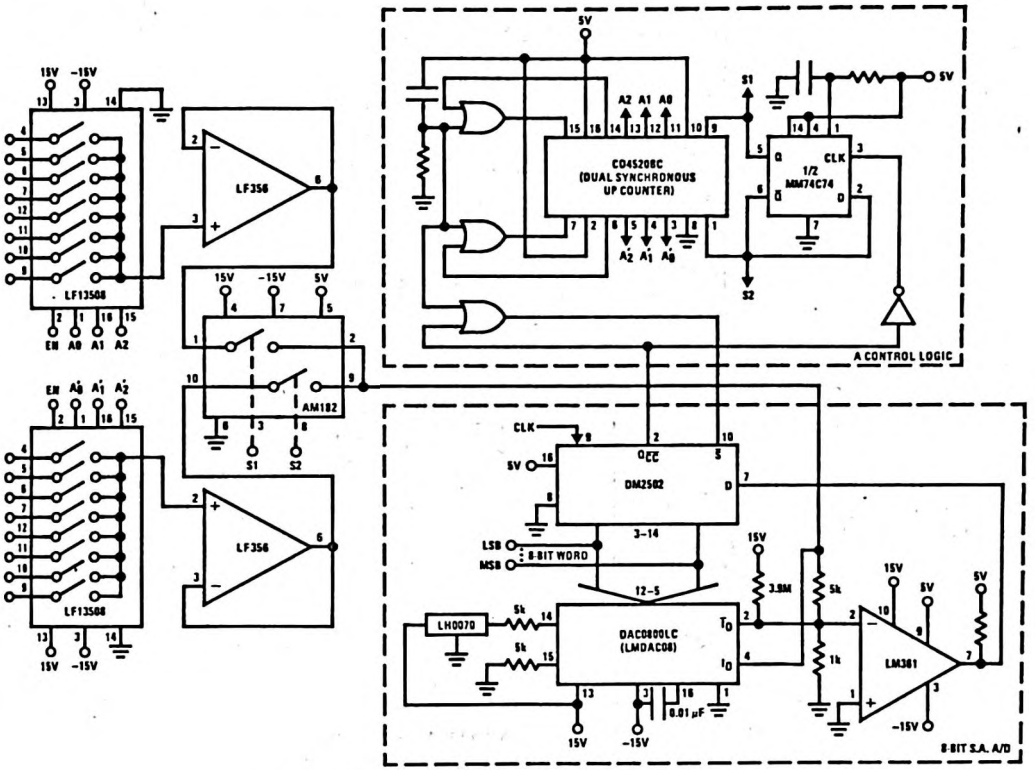


FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

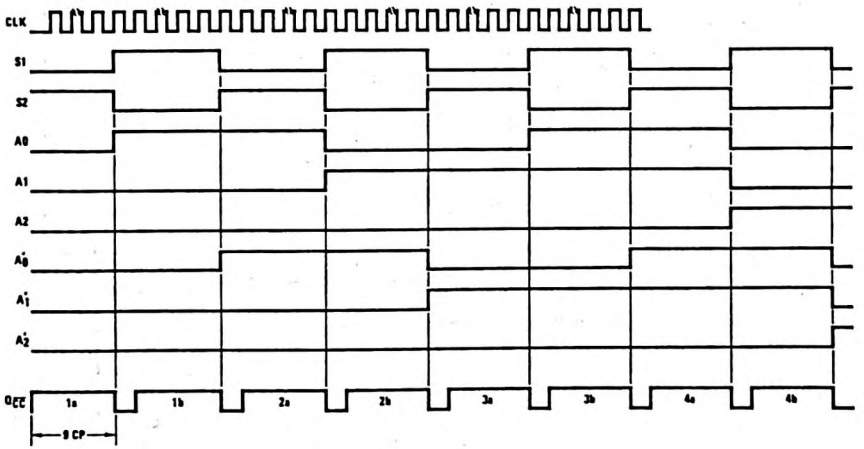


FIGURE 9b. Timing Diagram

typical applications (Continued)

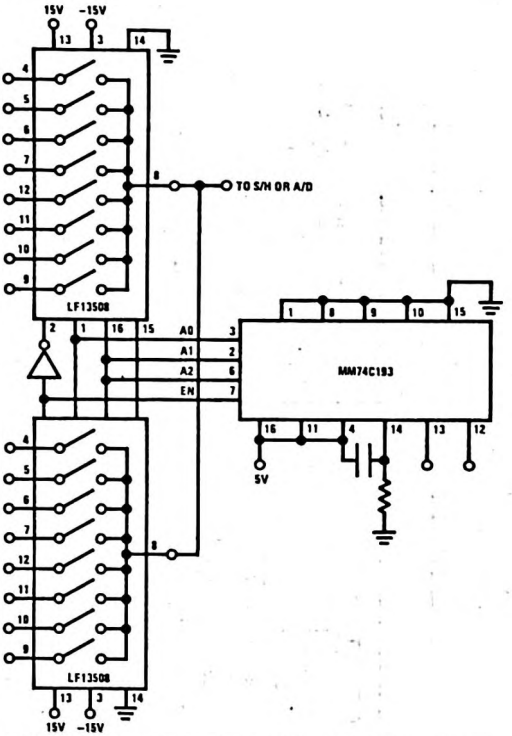
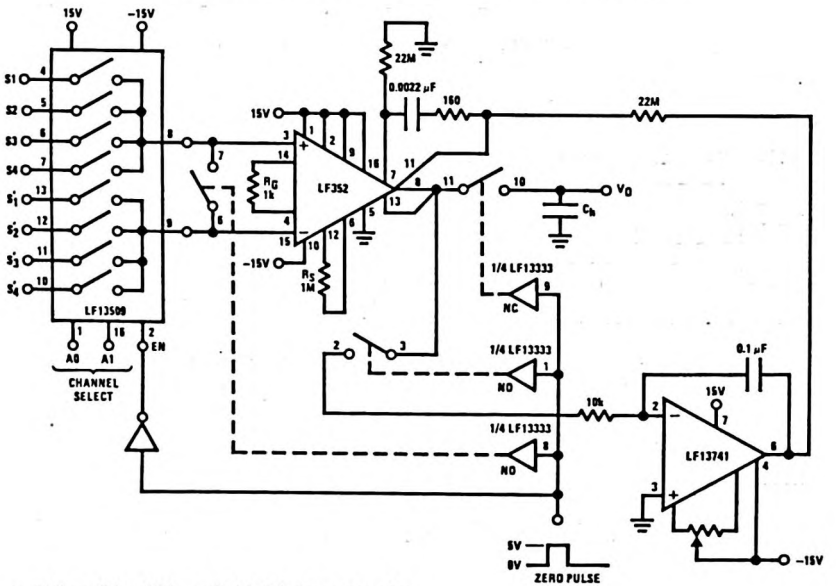


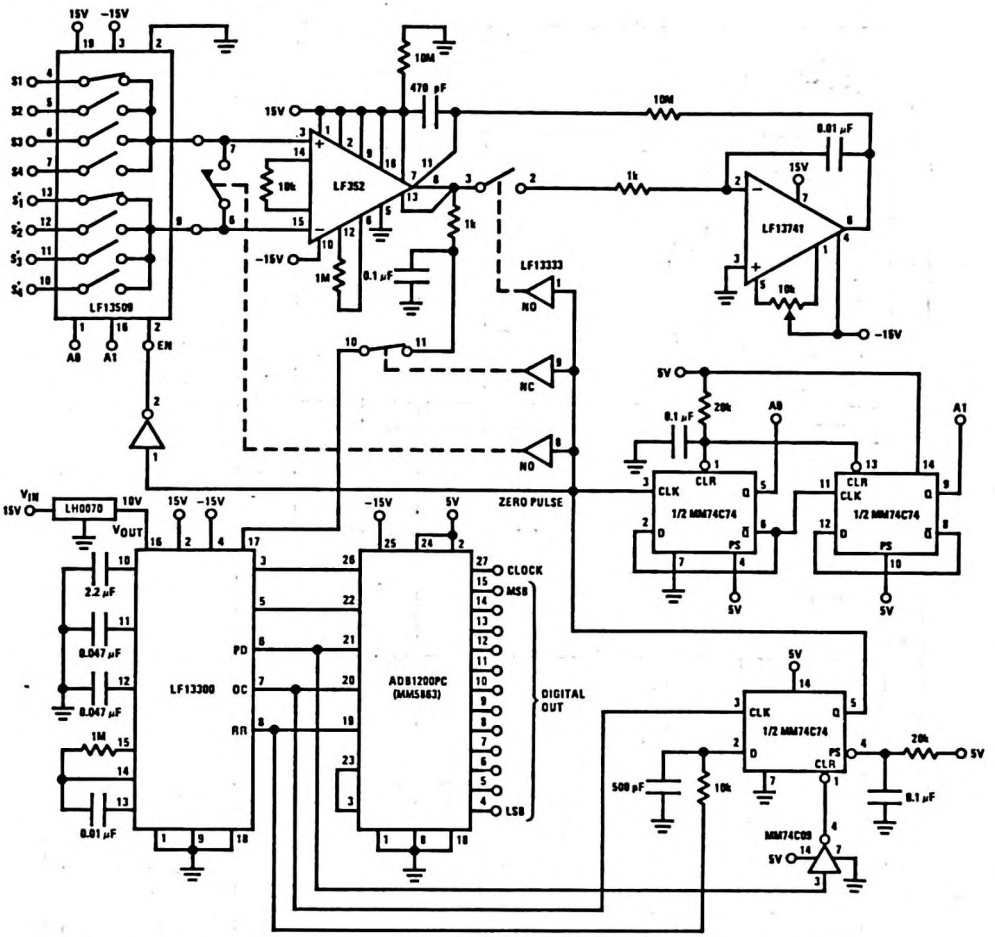
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing



- Differential multiplexer disabled during auto zeroing
- Minimum zeroing pulse width will depend upon the integrator R1C
- This scheme provides input offset adjust especially useful with high gain connections. The device, LF352, provides pins for output offset adjust. For more details, see LF352 data sheet.

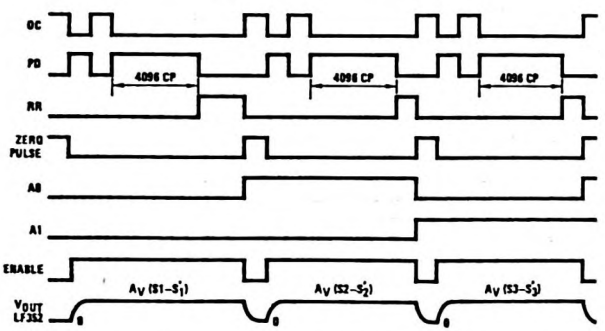
FIGURE 11. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier

typical applications (Continued)



- f_{CLOCK} max = 200 kHz
- The LF352 instrumentation amplifier is auto zeroed during offset correction cycle of the LF13300 A/D
- The system accuracy will mostly depend on the instrumentation amplifier gain linearity

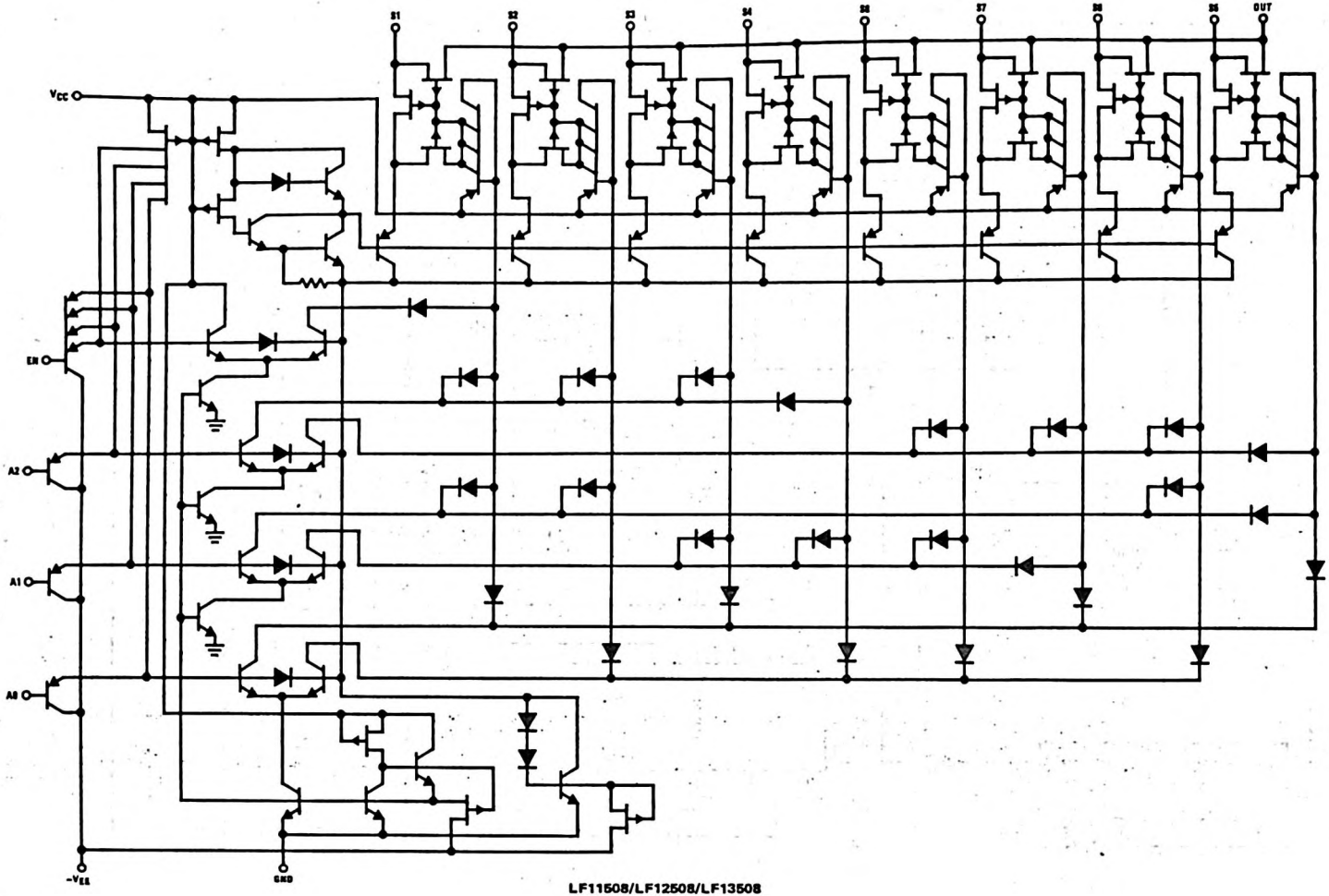
FIGURE 12a. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier and 12-Bit A/D Converter



PD: Polarity Detection
OC: Offset Correction
RR: Ramp Reference
For more details, see LF13300 data sheet

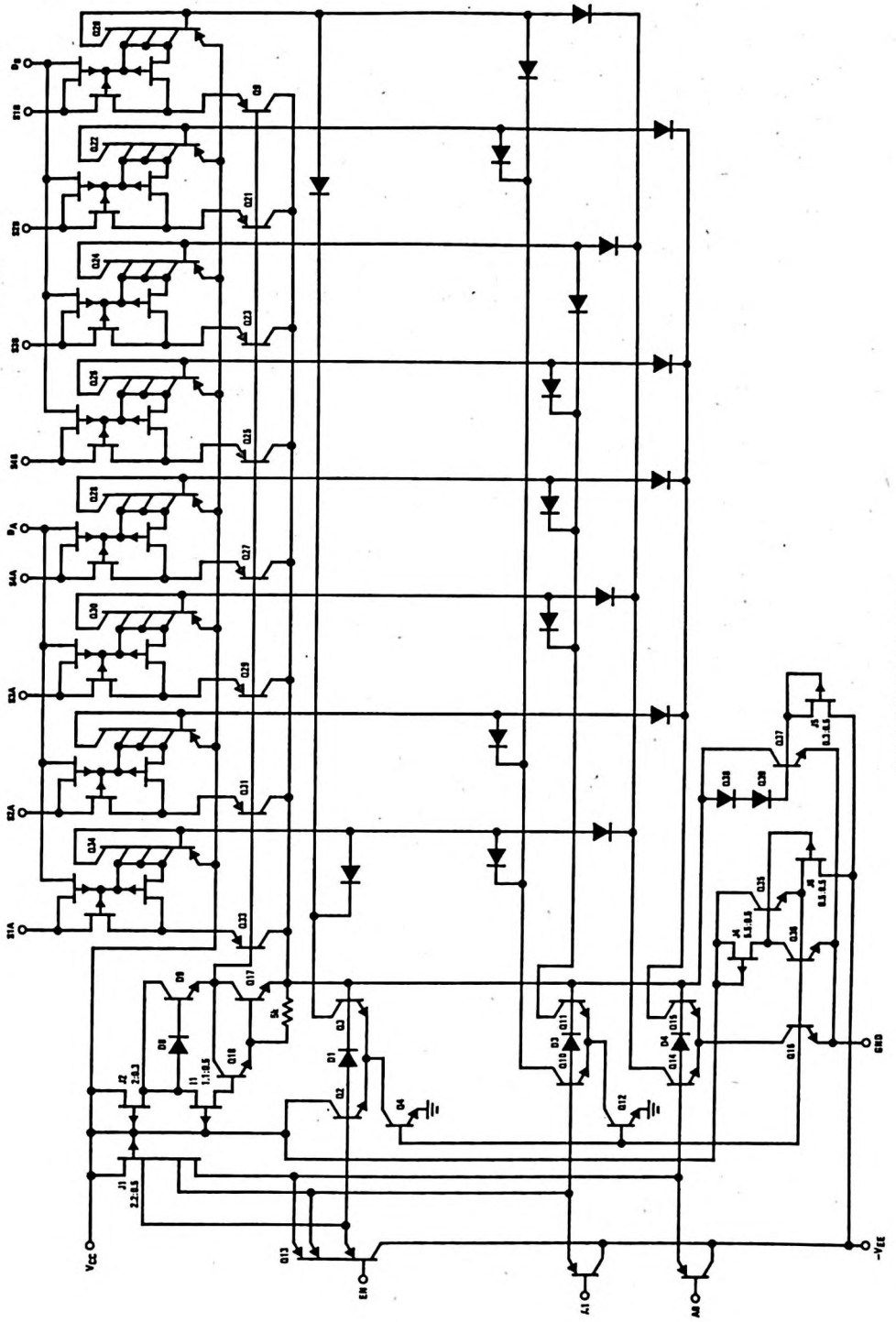
FIGURE 12b. System Timing Diagram for Differential MUX

schematic diagrams



LF11508/LF12508/LF13508

schematic diagrams (Continued)



LF11509/LF12509/LF13509

Section 8

Sample and Hold

8

National Semiconductor

LF198/LF298/LF398
Monolithic Sample and Hold Circuits

general description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

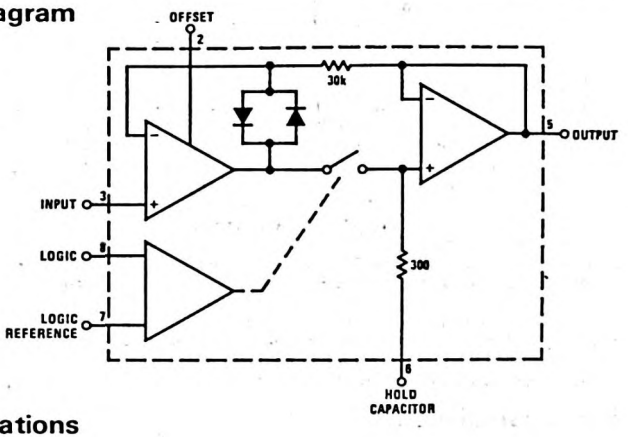
P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

features

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

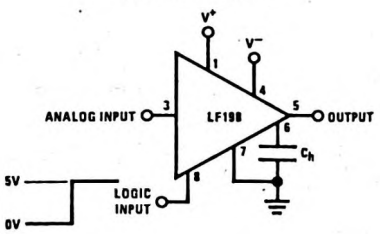
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

functional diagram

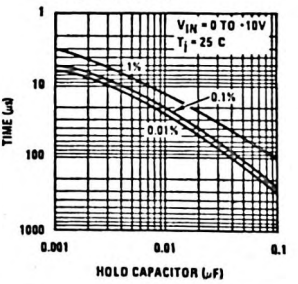


typical applications

Typical Connection



Acquisition Time



absolute maximum ratings

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198	−55°C to +125°C
LF298	−25°C to +85°C
LF398	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LF198/LF298			LF398			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	T_j = 25°C		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	T_j = 25°C		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	T_j = 25°C		10^{10}			10^{10}		Ω
Gain Error	T_j = 25°C, R_L = 10k		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	T_j = 25°C, C_h = 0.01μF	86	96		80	90		dB
Output Impedance	T_j = 25°C, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	T_j = 25°C, C_h = 0.01μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	T_j = 25°C		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	T_j = 25°C, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	ΔV_{OUT} = 10V, C_h = 1000 pF		4			4		μs
	C_h = 0.01μF		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2V		5			5		mA
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		dB
Differential Logic Threshold	T_j = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198 is 150°C, for the LF298, 115°C, and for the LF398, 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S = ±15V, T_j = 25°C, −11.5V ≤ V_{IN} ≤ +11.5V, C_h = 0.01μF, and R_L = 10 kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.

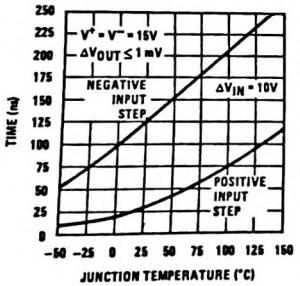
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

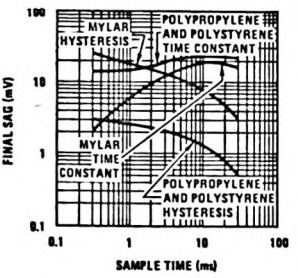
typical performance characteristics

Aperture Time*

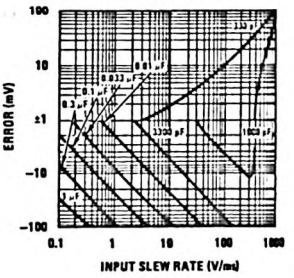


*See definition

Capacitor Hysteresis

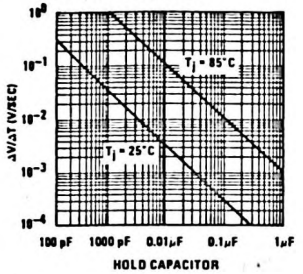


Dynamic Sampling Error

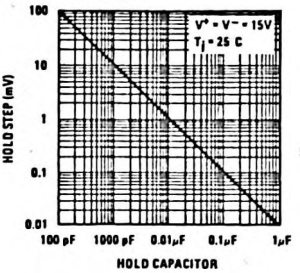


typical performance characteristics (con't)

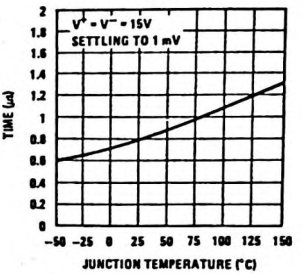
Output Droop Rate



Hold Step

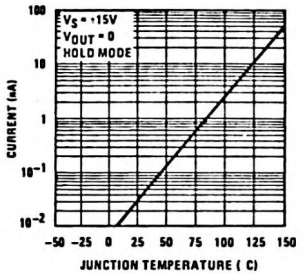


"Hold" Settling Time*

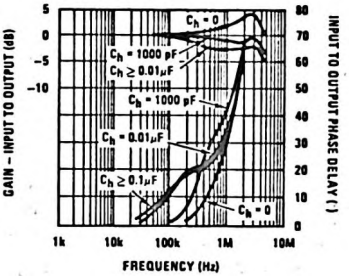


*See definition

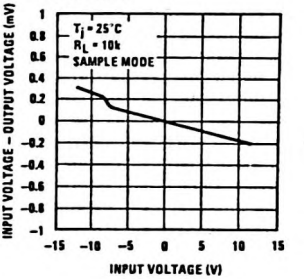
Leakage Current into Hold Capacitor



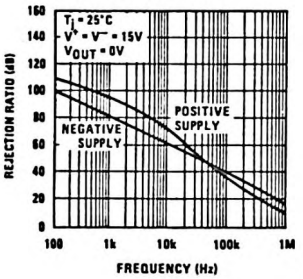
Phase and Gain (Input to Output, Small Signal)



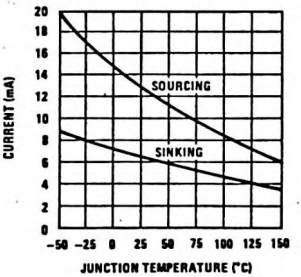
Gain Error



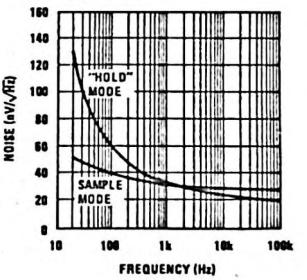
Power Supply Rejection



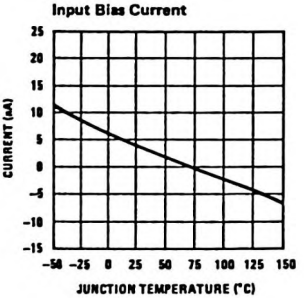
Output Short Circuit Current



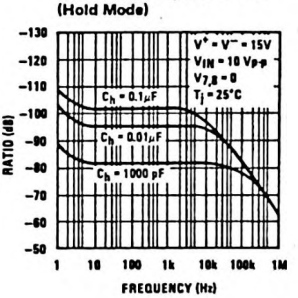
Output Noise



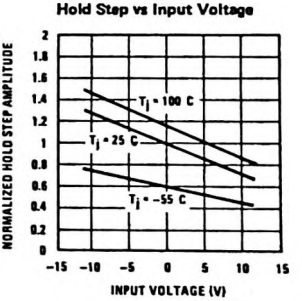
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage



application hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with $> 1\%$ hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. For more exact data, see the curve labeled dielectric absorption error vs sample time. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 0.2 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 0.2 V/μs.

Sampling Dynamic Signals

Sample error due to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1μs)(0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs)(0.6 V/μs) = –96 mV. Total output error is +60 mV (digital) –96 mV (analog) for a total of –36 mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

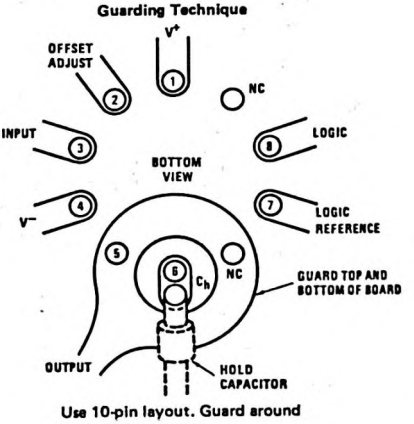
A curve labeled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

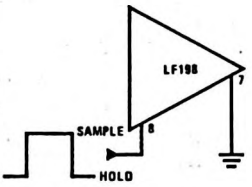
Guarding Technique



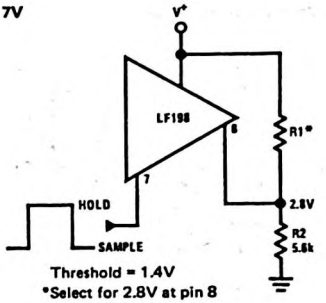
Use 10-pin layout. Guard around C_h is tied to output.

logic input configurations

TTL & CMOS
$3V \leq V_L$ (Hi State) $\leq 7V$

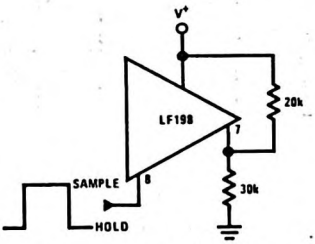


Threshold = 1.4V

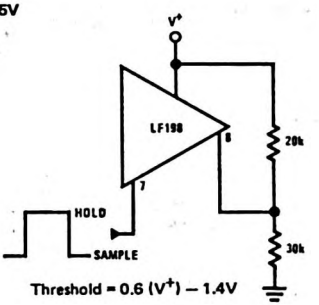


Threshold = 1.4V
*Select for 2.8V at pin 8

CMOS
$7V \leq V_L$ (Hi State) $\leq 15V$

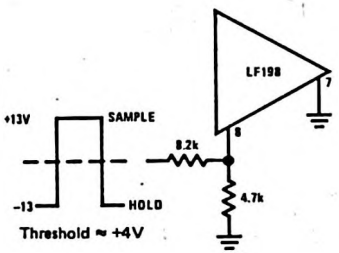


Threshold = 0.6 (V^+) + 1.4V

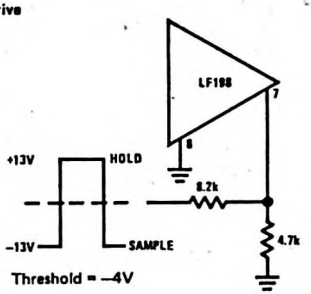


Threshold = 0.6 (V^+) – 1.4V

Op Amp Drive



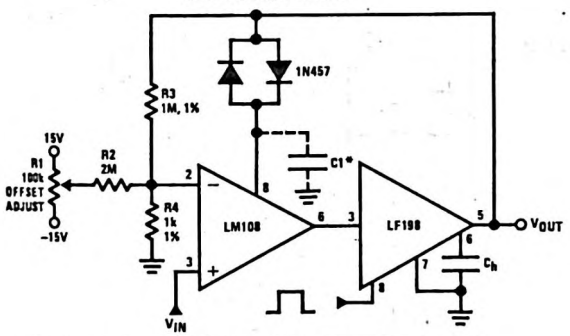
Threshold ≈ +4V



Threshold = –4V

typical applications (con't)

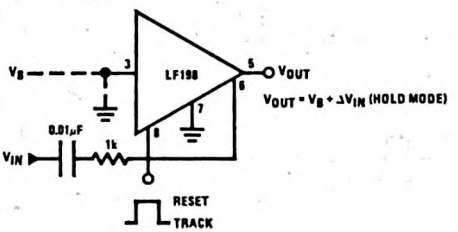
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

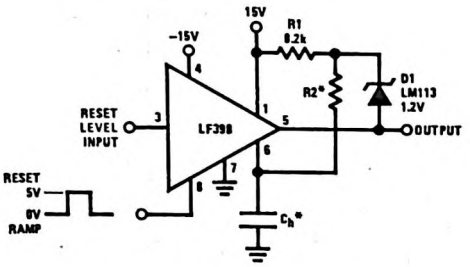
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit
(Output Follows Input in Hold Mode)



typical applications (con't)

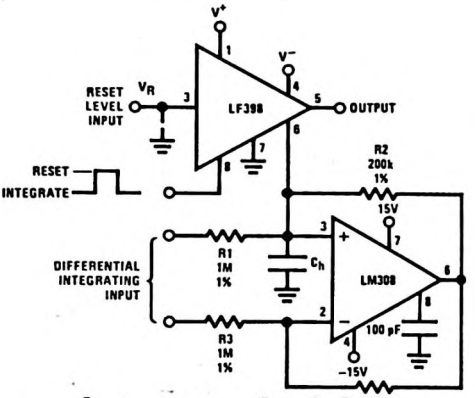
Ramp Generator with Variable Reset Level



*Select for ramp rate $R \geq 10k$

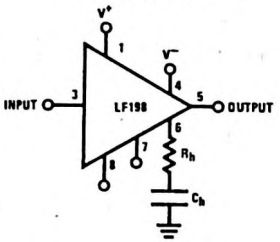
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

Integrater with Programmable Reset Level



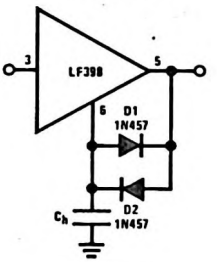
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

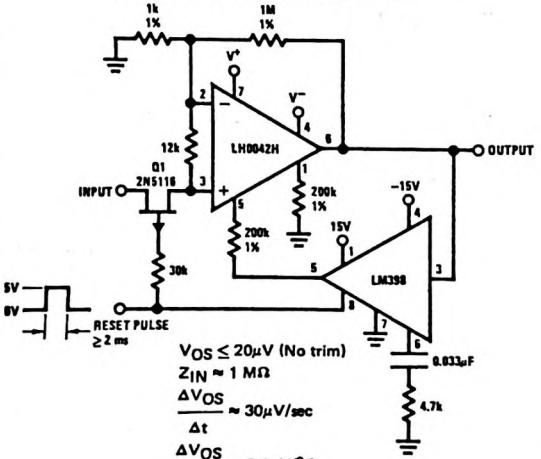


$$\text{Select } (R_h)(C_h) >> \frac{1}{2\pi f_{IN}\ (\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



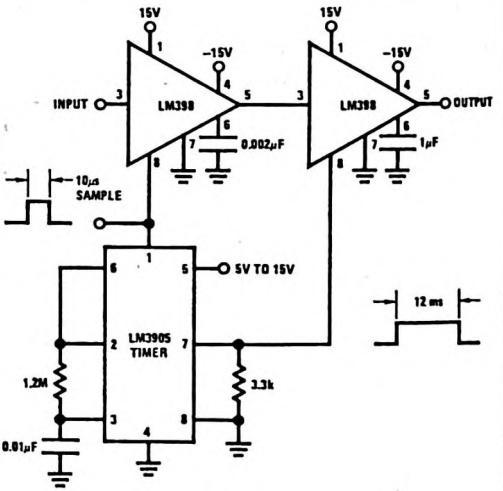
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$$

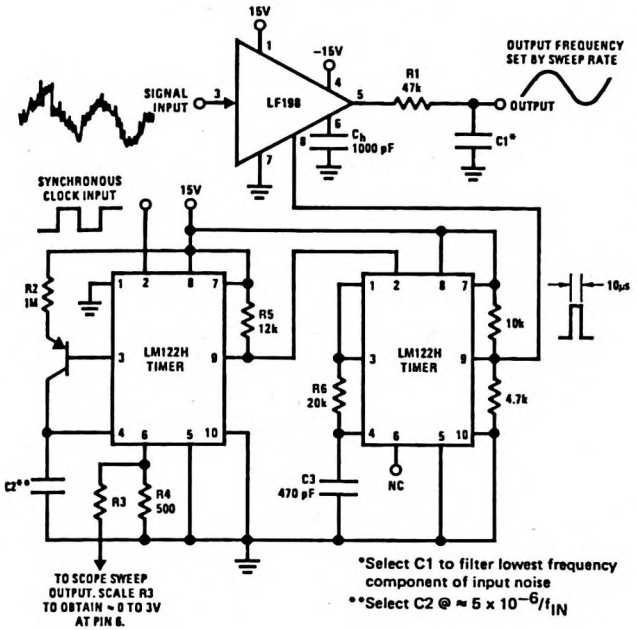
$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$$

Fast Acquisition, Low Droop Sample & Hold



typical applications (con't)

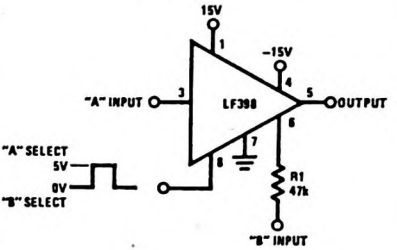
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

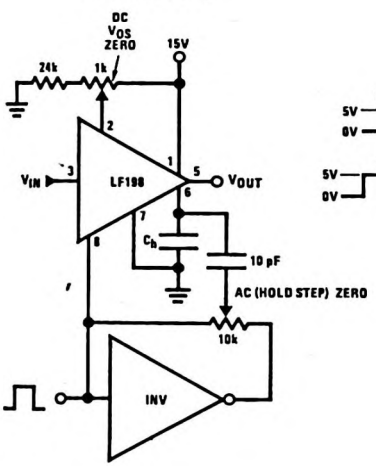
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2-Channel Switch

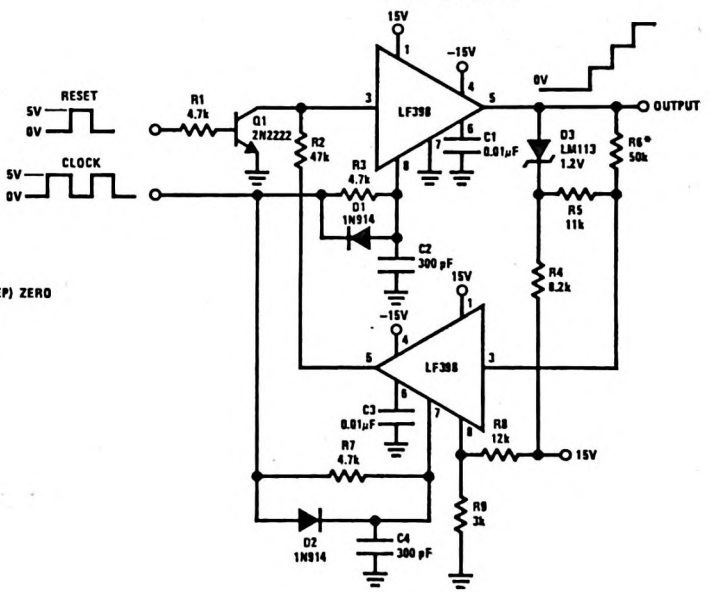


	A	B
Gain	1 ±0.02%	1 ±0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≈1 MHz	≈400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



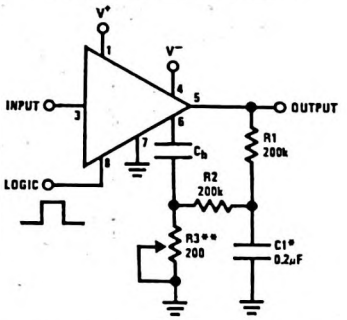
Staircase Generator



*Select for step height 50k → ≃ 1V Step

typical applications (con't)

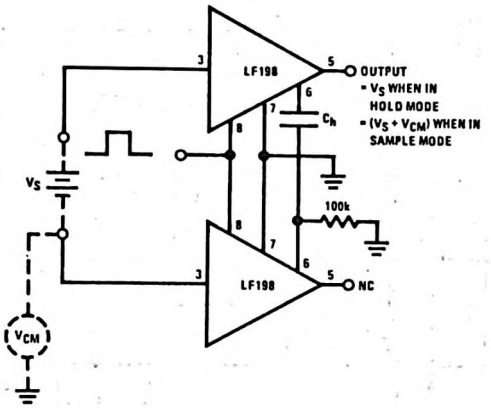
Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{T}{100k}$

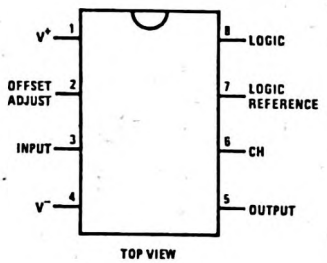
**Adjust for amplitude

Differential Hold



connection diagram

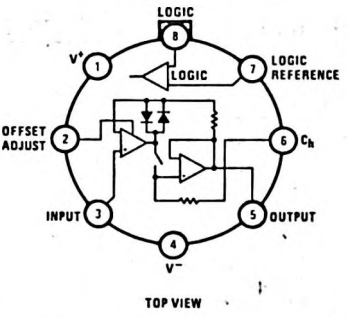
Dual-In-Line Package



Order Number LF198J, LF298J or LF398J
See NS Package J08A

Order Number LF398N
See NS Package N08B

Metal Can Package



Order Number LF198H, LF298H or LF398H
See NS Package H08C

National Semiconductor

LH0023/LH0023C, LH0043/LH0043C Sample and Hold Circuits

general description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

features

LH0023/LH0023C

- Sample accuracy—0.01% max
- Hold drift rate—0.5 mV/sec typ
- Sample acquisition time—100 μs max for 20V
- Aperture time—150 ns typ
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

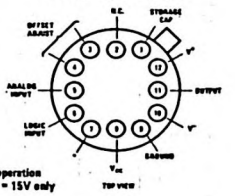
features

LH0043/LH0043C

- Sample acquisition time—15 μs max for 20V
  4 μs typ for 5V
- Aperture time—20 nS typ
- Hold drift rate—1 mV/sec typ
- Sample accuracy—0.1% max
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

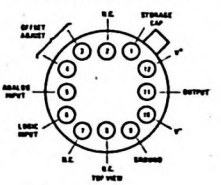
block and connection diagrams

LH0023/LH0023C

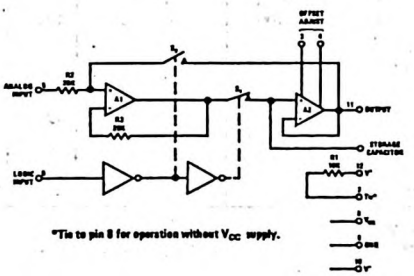


*Tie for operation with V^+ = 15V only

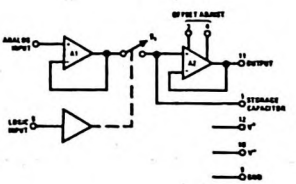
LH0043/LH0043C



Order Number LH0023H
LH0023CH, LH0043H
or LH0043CH
See NS Package H12B



*Tie to pin 8 for operation without V_{CC} supply.



absolute maximum ratings

Supply Voltage (V^+ and V^-)		±20V
Logic Supply Voltage (V_{CC})	LH0023, LH0023C	+7.0V
Logic Input Voltage (V_6)		+5.5V
Analog Input Voltage (V_5)		±15V
Power Dissipation		See graph
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0023, LH0043	−55°C to +125°C
	LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Soldering (10 sec)		300°C

electrical characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0023			LH0023C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current — I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current — I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current — I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current — I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current — pin 1	V_5 = ±10V; V_{11} = ±10V, T_A = 25°C		100	200		200	500	pA
	V_5 = ±10V; V_{11} = ±10V		0.6	1.0		1.0	2	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		10	20		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.1			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±20			±20	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C	±10	±11		±10	±11		V
	$R_L \geq$ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to +85°C for the LH0023C. All typical values are for T_A = 25°C.

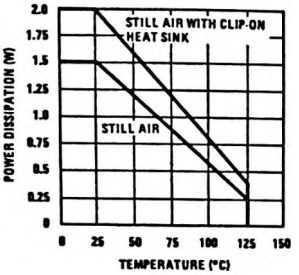
electrical characteristics LH0043/LH0043C: (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0043			LH0043C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	V_6 = 2.4V			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	V_6 = 0.4V			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_5 = 0V, V_6 = 2V, V_{11} = 0V V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	T_C = 25°C	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current — I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current—pin 1	V_5 = ±10V; V_{11} = ±10, T_C = 25°C		10	25		20	50	pA
	V_5 = ±10V; V_{11} = ±10V		10	25		2	5	nA
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF, T_C = 25°C		10	25		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF		10	25		2	5	mV/ms
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_C = 25°C		1	2.5		2	5	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.001 μF ΔV_{OUT} = 20V, C_S = 0.01 μF ΔV_{OUT} = 5V, C_S = 0.001 μF		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	V_{OUT} = 5V, C_S = 0.001 μF	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±40			±40	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C $R_L \geq$ 2k	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

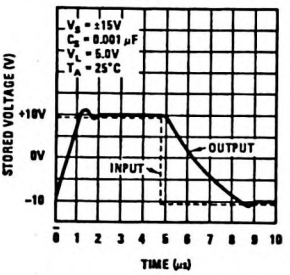
Note 2: Unless otherwise noted, these specifications apply for V^+ = +15V, V^- = −15V, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for T_C = 25°C.

typical performance characteristics

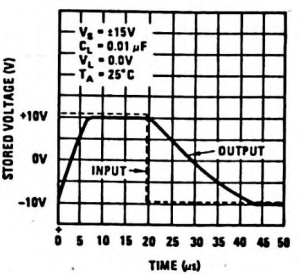
Power Dissipation



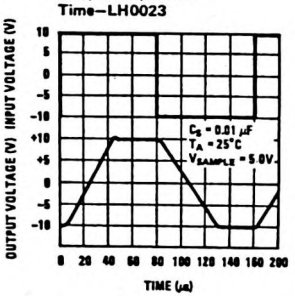
Sample Acquisition Time—LH0043



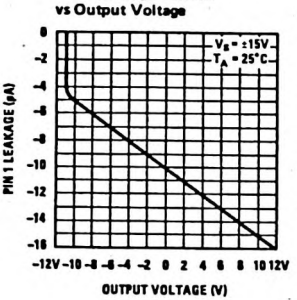
Sample Acquisition Time—LH0043



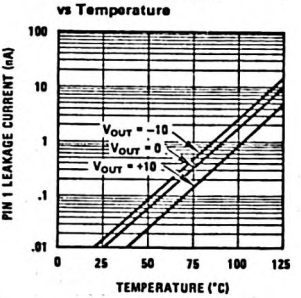
Sample Acquisition Time—LH0023



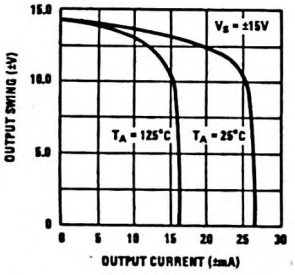
Pin 1 Leakage Current vs Output Voltage



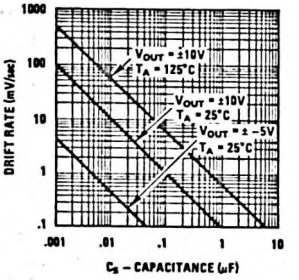
Pin 1 Leakage Current vs Temperature



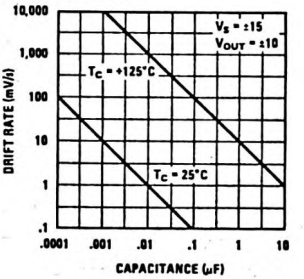
Output Current Limiting



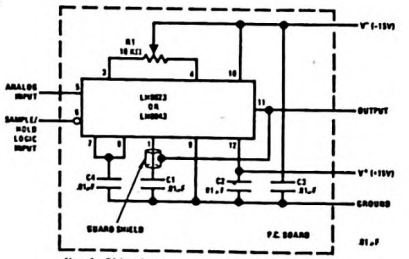
Drift Rate vs Capacitance



Drift vs Capacitance (LH0043)



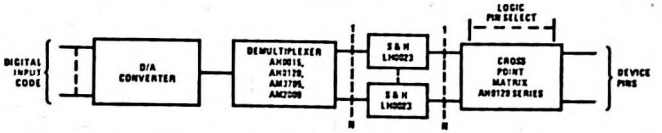
typical applications



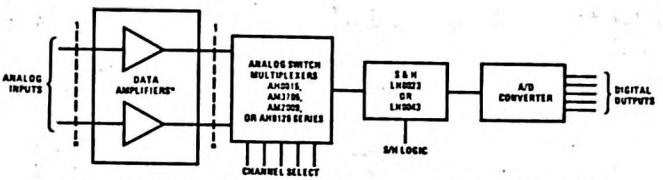
Note 1: C1 is polystyrene.
Note 2: C2, C3, C4 are ceramic disc.
Note 3: Jumper 7–8 and C4 not required for LH0043.
Note 4: R1 optional if zero trim is required.

How to Build a Sample and Hold Module

typical applications (con't)

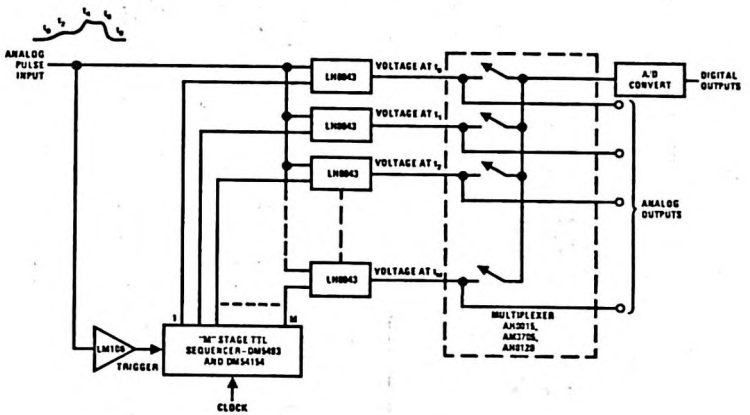


Forcing Function Setup for Automatic Test Gear

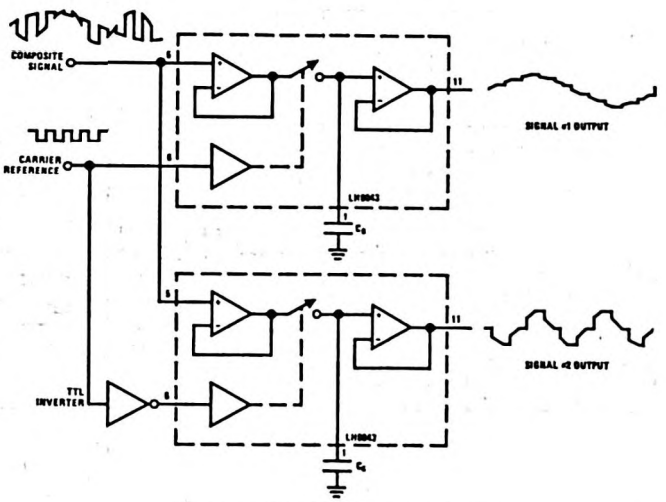


*See op amp selection guide for details. Most popular types include LH0052, LH175, LM108, LM112 and LM118.

Data Acquisition System



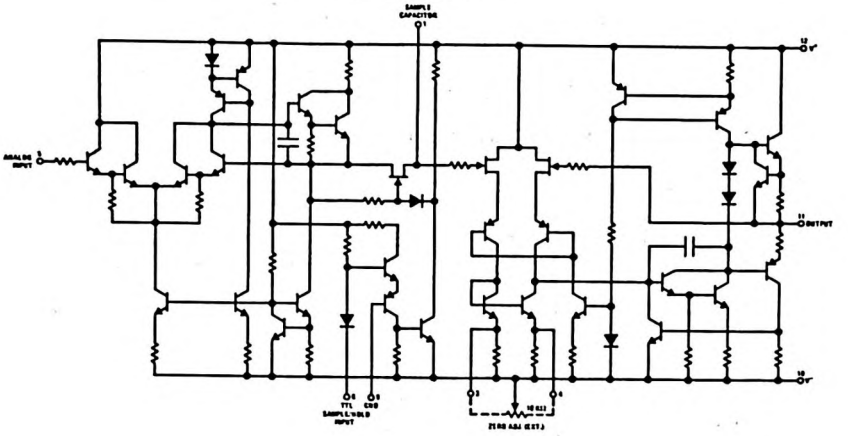
Single Pulse Sampler



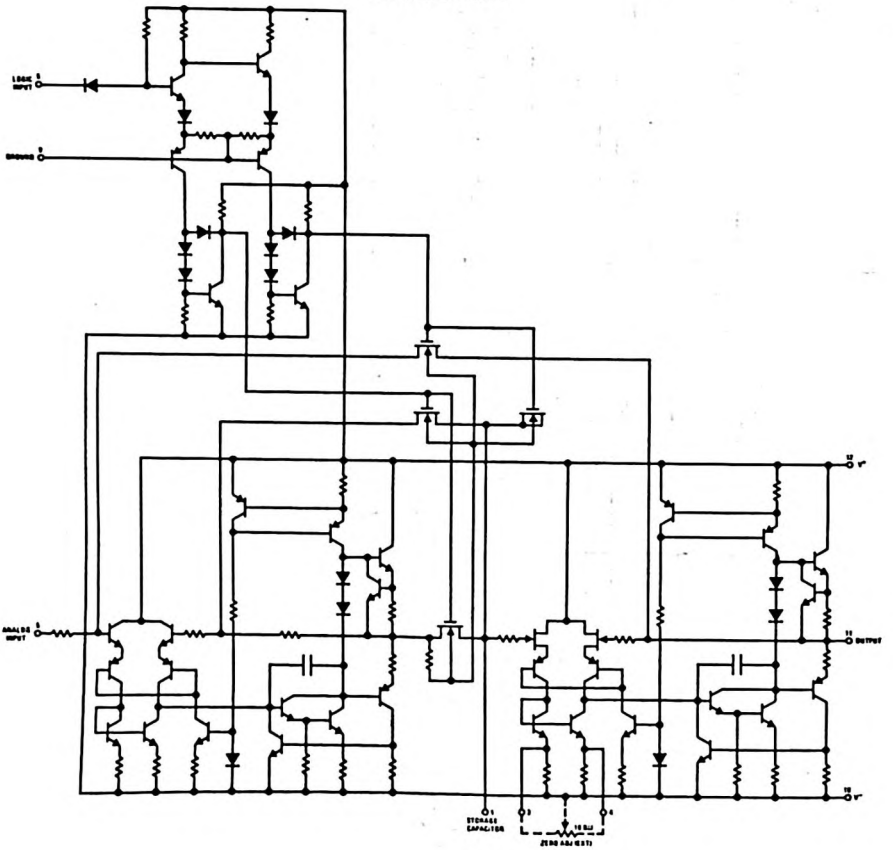
Two Channel Double Sideband Demodulator

schematic diagrams

LH0043/LH0043C



LH0023/LH0023C



applications information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection — LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_o RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_o RC_S}$$

where: R = the internal resistance in series with C_S

Δe_o = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_o C_S}}{20}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection—LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3} = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With C_S = 0.01 μF, the slew rate can be estimated by $\frac{dV}{dt} = \frac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}} = 1$V/$\mu$s or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization—LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply—LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of −55 to +125°C (−25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215–1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation—LH0023

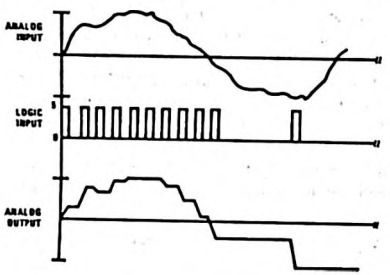
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

applications information (con't)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state (V_6 = 0.8V) which commands the switch S1 closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode (V_6 = 2.0V), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.



8.0 Definitions

- V_5: The voltage at pin 5, e.g., the analog input voltage.
- V_6: The voltage at pin 6, e.g., the logic control input signal.
- V_{11}: The voltage at pin 11, e.g., the output signal.
- T_A: The temperature of the ambient air.
- T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

National Semiconductor

LH0053/LH0053C High Speed Sample and Hold Amplifier

general description

The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0μs.

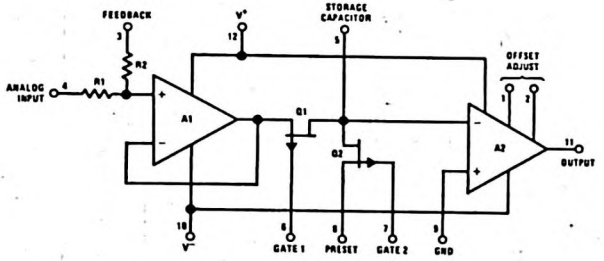
The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

An auxiliary switch within the device extends its usefulness in applications such as preset integrators.

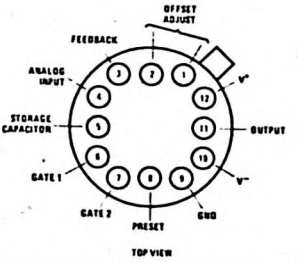
features

- Sample acquisition time 10μs max for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

schematic and connection diagrams

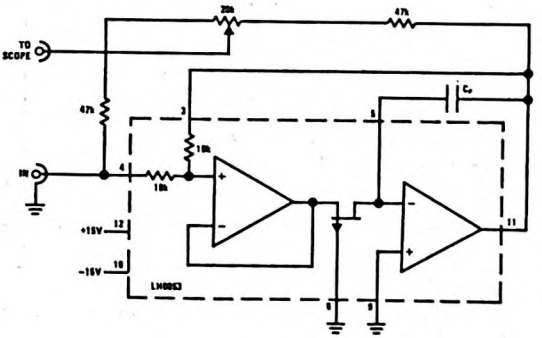


Metal Can Package



Order Number LH0053H or LH0053CH
See NS Package H12B

ac test circuit



Acquisition Time Test Circuit

absolute maximum ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6 and V_7)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10 mA
Power Dissipation	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

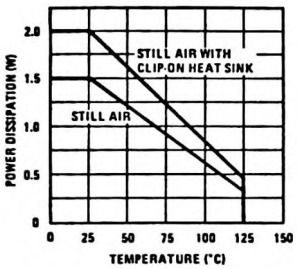
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0053			LH0053C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	V_6 = 0.5V, T_A = 25°C V_6 = 0.5			−5.0 −100			−5.0 −100	µA µA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	V_6 = 4.5V, T_A = 25°C V_6 = 4.5V			1.0 1.0			1.0 1.0	nA µA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_4 = 0V V_6 = 0.5V		13	18		13	18	mA
Input Bias Current (I_4)	V_4 = 0V, T_A = 25°C		120	250		150	500	nA
Input Resistance		9.0	10	11	9.0	10	11	kΩ
Analog Output Voltage Range	R_L = 2.0k	±10	±12		±10	±12		V
Output Offset Voltage	V_4 = 0V, V_6 = 0.5V, T_A = 25°C V_4 = 0V, V_6 = 0.5V		5.0	7.0 10		5.0	10 15	mV mV
Sample Accuracy (Note 2)	V_4 = ±10V, V_6 = 0.5V, T_A = 25°C		0.1	0.2		0.1	0.3	%
Aperture Time	ΔV_6 = 4.5V, T_A = 25°C		10	25		10	25	ns
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF, V_8 = 0V		5.0	10		8.0	15	µs
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 100 pF, V_6 = 0V		4.0			4.0		µs
Output Slew Rate	ΔV_{IN} = ±10V, T_A = 25°C, C_F = 1000 pF		20			20		V/µs
Large Signal Bandwidth	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		200			200		kHz
Leakage Current (Pin 5)	V_4 = ±10V, T_A = 25°C, V_4 = ±10V		6.0	30 30		10	50 3.0	pA nA
Drift Rate	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		6.0	30		10	50	mV/s
Drift Rate	V_4 = ±10V, C_F = 1000 pF			30			3.0	V/s
Q2 Switch ON Resistance	V_7 = 0.5V, I_8 = 1.0 mA, T_A = 25°C		100	300		100	300	Ω

Note 1: Unless otherwise noted, these specifications apply for V_S = ±15V, pin 9 grounded, a 1000 pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperature range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for T_A = 25°C.

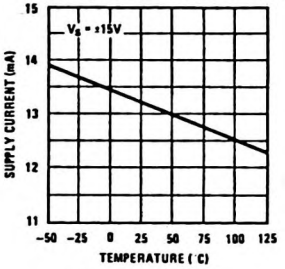
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

typical performance characteristics

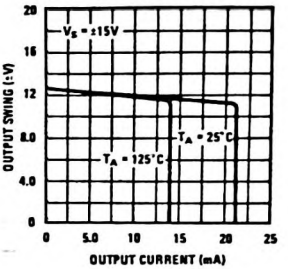
Power Dissipation



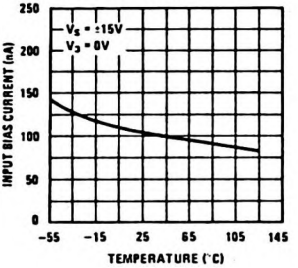
Supply Current vs Temperature



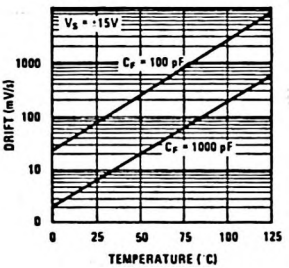
Output Current Limiting



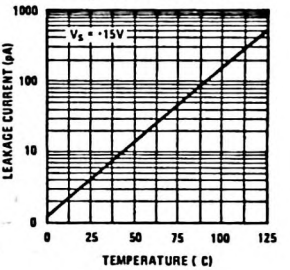
Input Bias Current



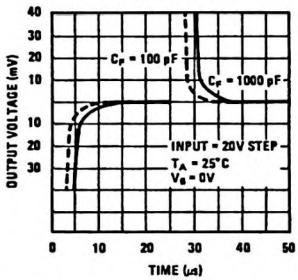
Drift



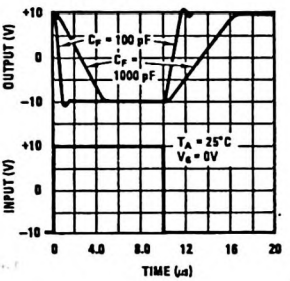
Leakage Current at Pin 5



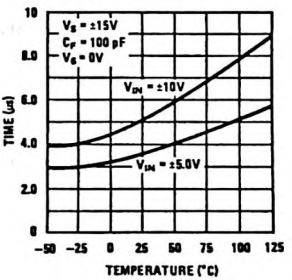
Sample Acquisition Time



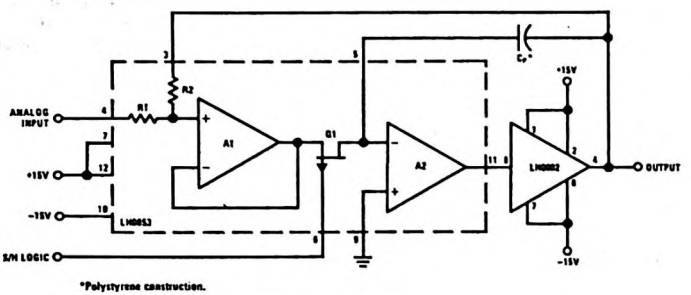
Output Slew Rate



Acquisition Time vs Temperature

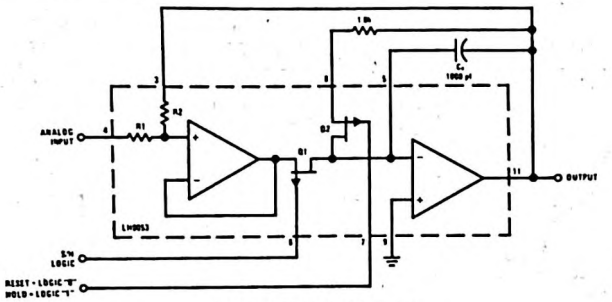


typical applications

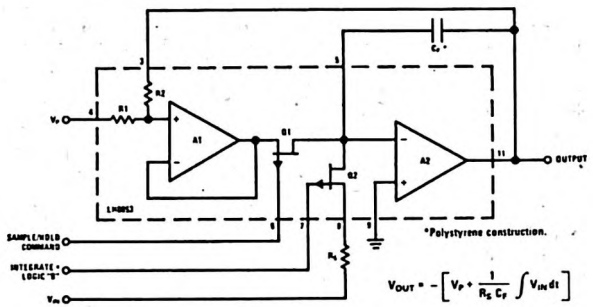


Increasing Output Drive Capability

typical applications (con't)



Sample and Hold with Reset



Preset Integrator

applications information

SOURCE IMPEDANCE COMPENSATION

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if R_S = 10Ω, a gain error of 0.1% results. Figure 1 and 2 show methods for accommodating non-zero source impedance.

DRIFT ERROR MINIMIZATION

In order to minimize drift error, care in selection C_F and layout of the printed circuit board is required. The capacitor should be of high quality teflon, polycarbonate or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

CAPACITOR SELECTION

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typical 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (20V/μs) and the setting time of output amplifier (≅ 1.0μs). For values above C_F = 1000 pF, acquisition time is given by:

$$t_a = \frac{C_F\,\Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step; e. g. 20V

I_{DSS} = The ON current of switch Q1 ≅ 5.0 mA

t_{S2} = The setting time of output amplifier ≅ 1.0μs

applications information (con't)

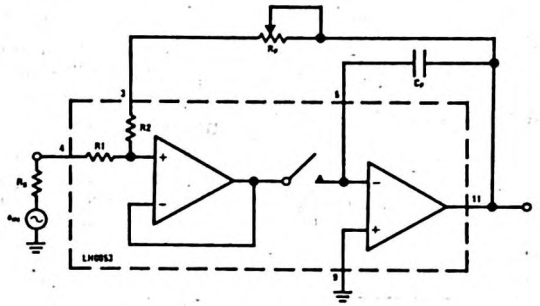


FIGURE 1. Non-Zero Source Impedance Compensation

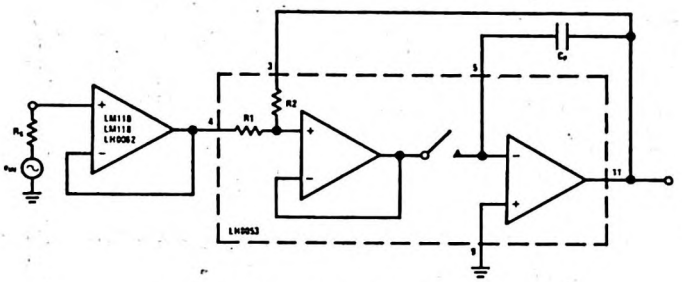


FIGURE 2. Non-Zero Source Impedance Buffering

GATE INPUT CONSIDERATIONS

5.0V TTL Applications

The LH0053 Gate inputs Gate 1 (pin 6) and Gate 2 (pin 7) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10k pull-up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in Figure 3. To obtain the highest speed and fastest acquisition time, the gate drive shown in Figure 6 is recommended.

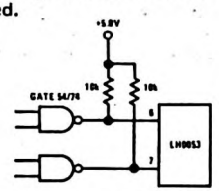


FIGURE 3. TTL Logic Compatibility

CMOS Applications

The LH0053 gate inputs may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in Figure 4.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

Unused Switch, Q2

In applications when switch Q2 is not used the logic input (pin 7) should be returned to +5.0V (or +15V for HTL applications) through a 10kΩ resistor. Analog Input, preset (pin 8) should be grounded.

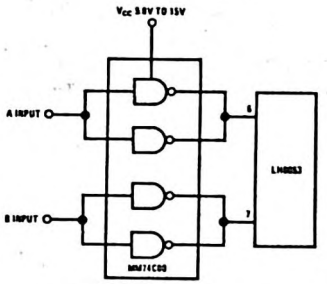


FIGURE 4. CMOS Logic Compatibility

HEAT SINKING

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermolloy 2240 will reduce the internal temperature rise by about 20°C. The result is a two-fold improvement in drift rate at temperature.

applications information (con't)

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

POWER SUPPLY DECOUPLING

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to by-pase V^+ (pin 12) and V^- (pin 10) to ground with 0.1μF disc capacitors in order to prevent oscillation. Should this procedure prove inadequate, the disc capacitors should be paralled with 4.7μF solid tantalum electrolytic capacitors.

DC OFFSET ADJUST

Output offset error may be adjusted to zero using the circuit shown in Figure 5. Offset null should be accomplished in the sample mode ($V_6 \leq 0.5V$) and analog input (pin 4) equal to zero volts.

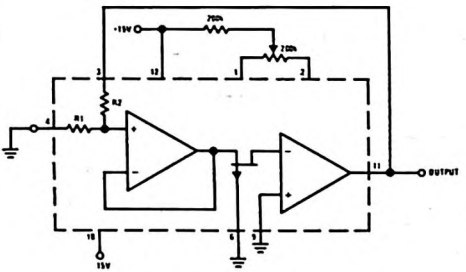


FIGURE 5. Offset Null Circuit

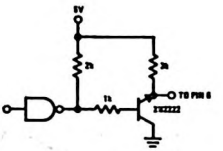


FIGURE 6. High Speed Drive Circuit

definition of terms

Voltage, V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage, V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input, $V_6 \leq 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leq 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, Gate 1, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from time the logic input passes through it's threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of input voltage.

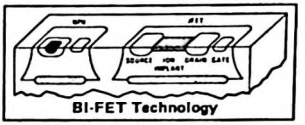
Section 9

Amplifiers

9

National Semiconductor

Amplifiers



LF152/LF252/LF352
FET Input Instrumentation Amplifier

general description

The LF152 series is the first monolithic JFET input instrumentation amplifier. The well-matched high voltage JFET input devices provide very high input impedance and extremely low bias currents, making the LF152 ideal in applications where high source impedances are encountered.

The LF152 very accurately amplifies a differential input signal and rejects common-mode signal and noise. It is not an op amp, but operates with an internal closed loop gain connection which allows good linearity with no external feedback. The LF152 eliminates the need for extremely precise resistor matching to obtain high common-mode rejection (CMR) and provides high input impedance as compared to the use of conventional op amps connected as a difference amplifier.

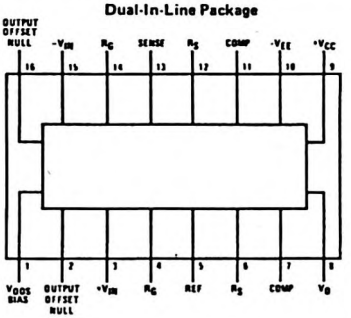
The LF152 utilizes internal differential current feedback eliminating the need for precision external feedback components. The amplifier gain can be easily adjusted from 1 to 1000 by changing the value of a single resistor. The transfer function for the LF152 is highly accurate because it has a very low initial gain error and non-linearity. The bandwidth and slew rate are externally controlled and the sense input and device output are pinned out separately for added versatility.

features

- JFET inputs
- High input impedance — $2 \times 10^{12}\Omega$
- Low bias currents — 3 pA
- Low noise currents — 0.01 pA rms
- Low gain nonlinearity — 0.02%
- High common-mode rejection ratio (G = 100) — 110 dB min
- Single resistor gain adjust
- External compensation for extended gain and frequency ranges
- Both input and output offset adjust capability to allow a change of gain without rezeroing
- Low supply current — 1 mA

connection diagram

Dual-In-Line Package



Order Number LF152D, LF252D or LF352D
See NS Package D16A

simplified schematic

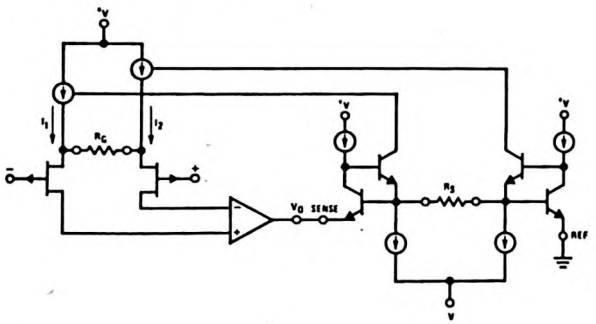


FIGURE 1

typical circuit

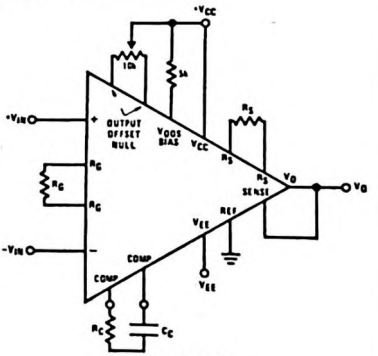


FIGURE 2

absolute maximum ratings

	LF152	LF252	LF352
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage Range	±22V	±18V	±18V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Power Dissipation and Thermal Resistance (Note 1)			
Cavity DIP (D) P_D (25°C)	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature	+150°C	+110°C	+100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$	$-65°C \leq T_A \leq +150°C$	$-65°C \leq T_A \leq +150°C$
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	LF152			LF252/LF352			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G_R	Gain Range	$R_C = 160\Omega$, $C_C = 0.002\mu F$	1		1000	1		1000	
G	Gain Equation	$G = R_S/R_G$							
G_E	Error From Gain Equation	$T_A = 25°C$, $G = 1-100$, $R_L = 10k$		0.05	0.1		0.05	0.2	%
G_{NL}	Gain Nonlinearity	$T_A = 25°C$, $G = 1-100$, $R_L = 10k$		0.02	0.05		0.02	0.1	%
$\Delta G\ \Delta T$	Gain Temperature Coefficient			3			3		ppm/°C
V_O	Output Voltage Range	$R_L = 2k$	±9			±9			V
R_O	Output Resistance	$T_A = 25°C$, $G = 1$		1.2			1.5		Ω
V_{IN}	Input Voltage Range		±10	±12		±10	±12		V
I_B	Input Bias Current	$T_A = 25°C$		3	20		3	40	pA
				3	20		0.2	3	nA
I_{IO}	Input Offset Current	$T_A = 25°C$		0.5	10		0.5	20	pA
				0.3	2.0		0.05	0.6	nA
R_{IN}	Input Resistance	$T_A = 25°C$							
	Differential			$2x10^{12}$			$2x10^{12}$		Ω
	Common Mode			$2x10^{12}$			$2x10^{12}$		Ω
C_{IN}	Input Capacitance	$T_A = 25°C$							
	Differential			2.5			2.5		pF
	Common Mode			5.0			5.0		pF
CMRR	Common-Mode Rejection (RTI) (Note 4)	$G = 1$	75	85		65	80		dB
		$G = 10$	95	105		85	100		dB
		$G = 100$	110	125		100	120		dB
		$G = 1000$	115	125		105	120		dB
V_{IOS}	Input Offset Voltage	$T_A = 25°C$		8	15		15	30	mV
$\Delta V_{IOS}/\Delta T$	Temperature Coefficient			10			10		µV/°C
$\Delta V_{IOS}/\Delta V_S$	Supply Sensitivity			100			200		µV/V
V_{OOS}	Output Offset Voltage	$T_A = 25°C$			200			400	mV
$\Delta V_{OOS}/\Delta T$	Temperature Coefficient			600			600		µV/°C
$\Delta V_{OOS}/\Delta V_S$	Supply Sensitivity			400			800		µV/V
I_{REF}	Reference Current			15			20		µA
R_{REF}	Reference Input Resistance			500			250		MΩ
I_S	Supply Current	$T_A = 25°C$		0.7	2.2		1.2	2.2	mA

ac electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	LF152			LF252/LF352			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
e_n	Noise Voltage (RTI) (Note 5)	T_A = 25°C							
		0.1 Hz – 10 Hz		1.3↑670/G			1.3↑670/G		μVp-p
		10 Hz – 10 kHz		8↑450/G			8↑450/G		μVrms
i_n	Noise Current (RTI) (Note 5)	T_A = 25°C, 10 Hz – 10 kHz		0.01			0.01		pArms
GBW	Small Signal Bandwidth	T_A = 25°C, ↑3 dB							
		G = 1		140			140		kHz
		G = 10		50			50		kHz
		G = 100		30			30		kHz
		G = 1000		7			7		kHz
		T_A = 25°C, ±1% Flatness							
		G = 1		5			5		kHz
		G = 10		4			4		kHz
		G = 100		2			2		kHz
		G = 1000		1.5			1.5		kHz
↑ PBW	Full-Power Bandwidth			25			25		kHz
↑ SR	Slew Rate			1			1		V/μs
↑ t_s	Settling Time 0.1%	T_A = 25°C							
		G = 1		15			15		μs
		G = 10		15			15		μs
		G = 100		40			40		μs
		G = 1000		200			200		μs

NNote 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{j\,MAX}$, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,MAX} - T_A)/\theta_{jA}$ or the 25°C $P_{D\,MAX}$, whichever is less.

NNote 2: These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted. Parameters are specified for R_C = 160Ω, C_C = 0.002μF, and a proper layout such as the PC board in *Figure 7*, which is laid out for *FFigure 2 and Figure 4*.

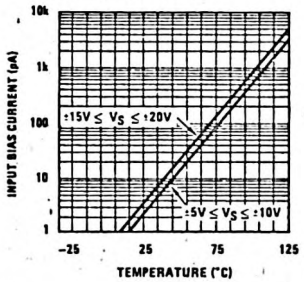
NNote 3: If V_{OOS} adjust is not used, pins 1, 2 and 16 MUST be shorted to V_{CC}.

NNote 4: Referred to input (RTI). May be referred to output by subtracting gain in dB.

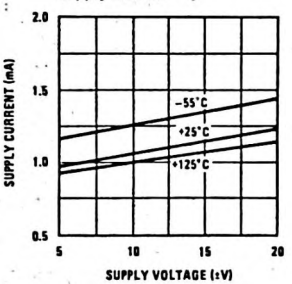
NNote 5: Referred to input (RTI). May be referred to output by multiplying by gain G.

ttypical performance characteristics

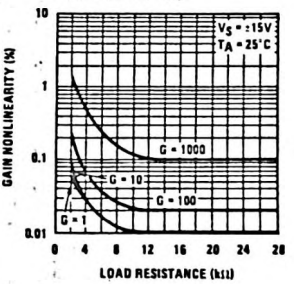
Input Bias Current



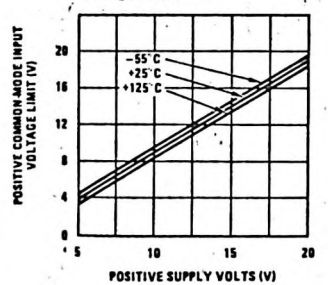
Supply Current



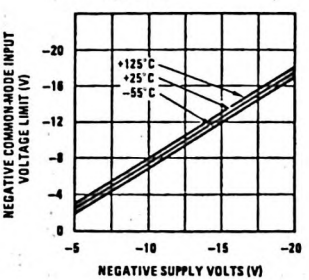
Gain Nonlinearity



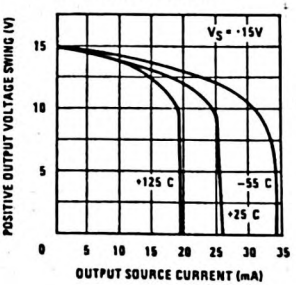
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit

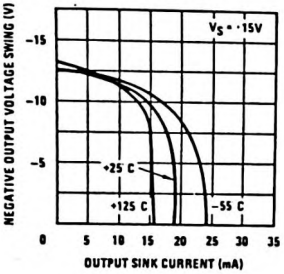


Positive Current Limit

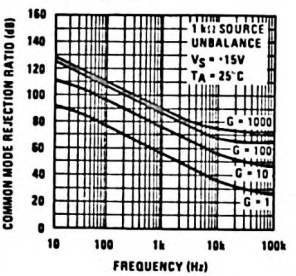


typical performance characteristics (con't)

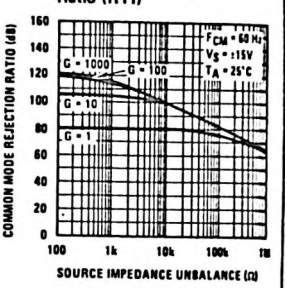
Negative Current Limit



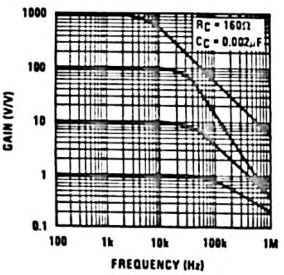
Common-Mode Rejection Ratio (RTI)



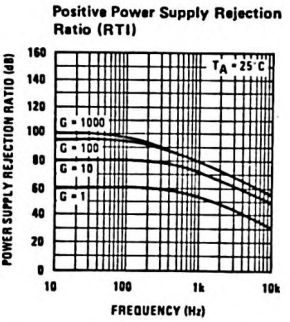
Common-Mode Rejection Ratio (RTI)



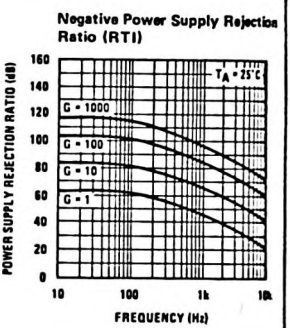
Frequency Response



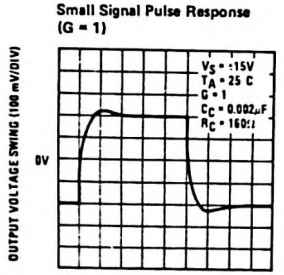
Positive Power Supply Rejection Ratio (RTI)



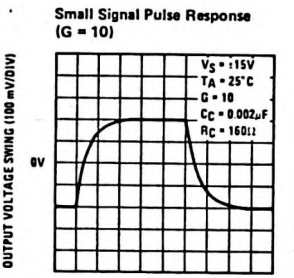
Negative Power Supply Rejection Ratio (RTI)



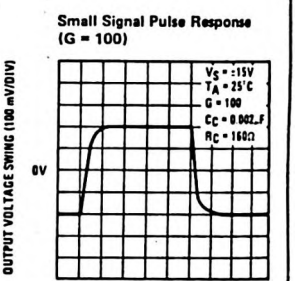
Small Signal Pulse Response (G = 1)



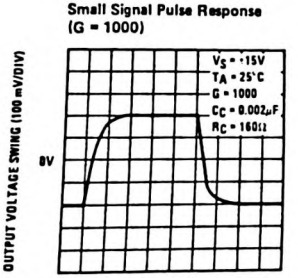
Small Signal Pulse Response (G = 10)



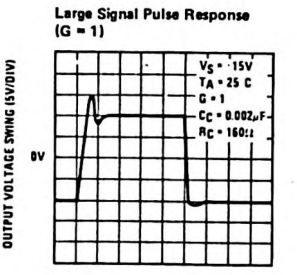
Small Signal Pulse Response (G = 100)



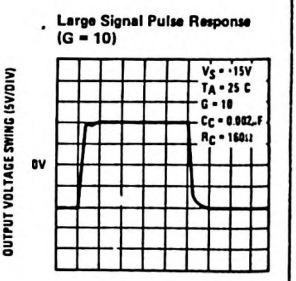
Small Signal Pulse Response (G = 1000)



Large Signal Pulse Response (G = 1)

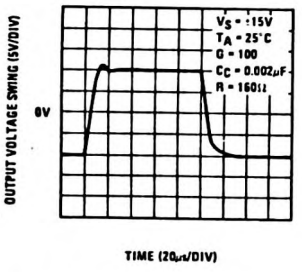


Large Signal Pulse Response (G = 10)

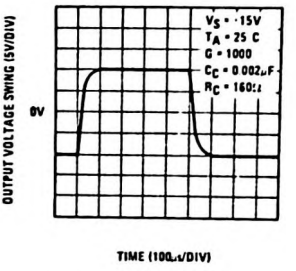


typical performance characteristics (con't)

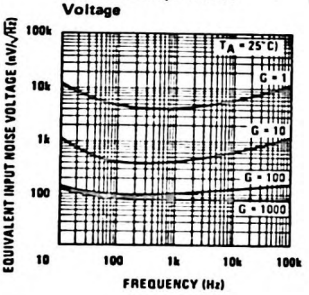
Large Signal Pulse Response
(G = 100)



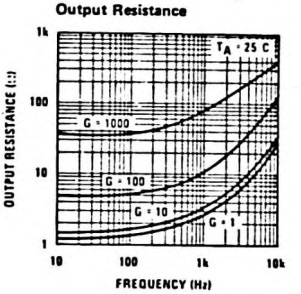
Large Signal Pulse Response
(G = 1000)



Equivalent Input Noise
Voltage



Output Resistance



application hints

BASIC OPERATION

The LF152 is a monolithic JFET input differential current feedback instrumentation amplifier. The BI-FET process used to fabricate the LF152 makes it possible to take advantage of JFETs throughout the design. In the simplified schematic of *Figure 1*, the differential input voltage is impressed across resistor R_G via the input JFETs, while the difference between the sense and reference voltages is impressed across the resistor R_S. The gain of the amplifier is determined by the ratio of resistor R_S to resistor R_G ($G = R_S/R_G$). (For clarity let's follow a signal through the amplifier:)

In *Figure 1*, let $R_G = R_S = 1\ M\Omega$, the (—) input be grounded, and the (+) input be 1V; the output should be 1V. The 1V signal applied developes 1μA through R_G from right to left and unbalances the current drive to the second stage amplifier. The additional current driven into the (+) input of the second stage amplifier causes the output to increase. As V_O increases, the sense input voltage increases and the left side of R_S also increases. When the sense input has risen 1V, 1μA will flow through R_S from left to right and, thus, subtract 1μA from I_1. An opposite action simultaneously occurs in I2 which brings the currents into the second stage and thus the system back into balance.

The LF152 series is designed to optimize key parameters in instrumentation amplifiers. The device has very high common-mode rejection, low gain non-linearity, extremely low bias currents and very high input impedance.

INPUTS

The P-channel JFET input devices of the LF152 series provide very low bias currents and very high input impedances.

The maximum differential input voltage is independent of the supply voltages, however, neither of the input voltages should be allowed to exceed the negative supply, as this will cause large currents to flow, which can result in a destroyed unit.

Exceeding the negative voltage range on either input will cause a reversal of phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative input voltage range on both inputs will force the amplifier output to a high state. Exceeding the positive input voltage range on a single input will not change the phase of the output; however, gain linearity will degrade. If both inputs exceed the positive input voltage range, the output of the amplifier will be forced to a high state.

The common-mode slew rate of the inputs should be limited to 5V/μs to insure low input bias currents.

application hints (con't)

USING THE SENSE, REFERENCE, AND OUTPUT PINS

The sense input and the output of the device are pinned out separately to allow increased flexibility in system designs (see applications). The reference input allows biasing of the output voltage, from +10V to --10V. The ac input resistance of both the sense and reference inputs is unusually high because their input currents are forced to be constant with voltage (typically 20μA).

The maximum linear output swing is determined by the magnitude of resistor R_S:

$$|V_{O\,MAX}| = 10\mu A\,(R_S)$$

If the output of the amplifier is to be abruptly changed more than 6V, a PNP transistor should be connected, as shown in *Figure 3*, to prevent the slew rate of the output from exceeding the slew rate of the sense stage. If this precaution is not taken, the base-emitter junction of the input transistor in the sense stage will transiently break down and its β will degrade, resulting in a permanent negative shift in output offset voltage.

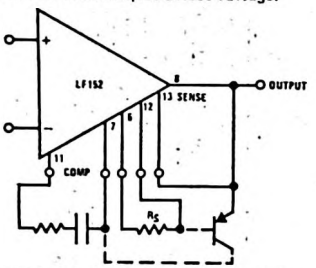


FIGURE 3. Large Signal Transient Suppression

OFFSET VOLTAGE

Because of the two stage design of the instrumentation amplifier, there are two independent contributors to offset voltage (V_{OS}). The output offset (V_{OOS}) is independent of gain while the input offset (V_{IOS}) is multiplied by the gain of the amplifier to the output.

$$V_{OS} = V_{IOS}\,(G) + V_{OOS}$$

The output offset of the LF152 can be adjusted as shown in *Figure 2*. In addition, the LF152 features input offset adjust which is not common to monolithic instrumentation amplifiers and is normally available only on expensive modules. The simple adjust scheme shown in *Figure 5* has only a slight increase in non-linearity compared to that of *Figure 4* and is recommended for most applications. Nulling both input and output offset makes the overall offset zero, independent of gain.

The output offset is affected by adjustment of the input offset. For every mV of input offset adjust, the output offset will change by approximately 32 mV. Adjustment of the output offset has no effect on the input offset, so it should always be done last.

Offset adjustment changes the temperature coefficient of the V_{OS} drift. The typical input offset drift of the unadjusted device is $-10\mu V/°C$. If the input offset is adjusted, the V_{IOS} drift increases by approximately

$$V_{IOS}\ \text{drift} \approx -10\mu V/°C + 2\mu V/°C/(\text{mV of adjustment})$$

The V_{OOS} drift will be improved by output offset adjust because the magnitudes of the current sources adjusted become less sensitive to V_{BE} variations. If V_{OOS} adjust is not used, pins 1, 2 and 16 must be shorted to the positive supply for circuit operation.

OFFSET VOLTAGE ADJUSTMENT PROCEDURE

For gains less than 100, only output offset adjustment is needed. For gains greater than 100, input offset adjust is usually necessary since the input offset voltage amplified to the output may be out of the range of the output offset adjust. Input offset adjust is also needed if zero overall offset is desired while varying the amplifier gain.

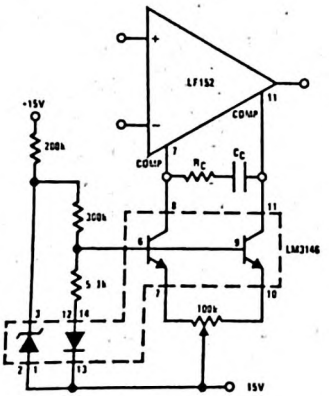


FIGURE 4. Input Offset Adjust

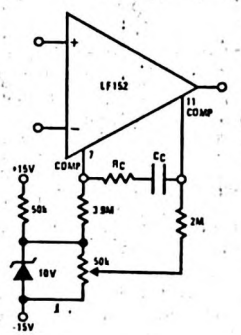


FIGURE 5. Simple Input Offset Adjust

application hints (con't)

To adjust the input offset, the following procedure should be used:

The effective input offset voltage appears directly across R_G when both inputs are connected to ground, and can be measured by a voltmeter referenced to ground. This offset error across R_G can be zeroed by the input offset adjustment circuit shown in *Figure 4 or 5*. The remaining error at the output is strictly due to the output offset voltage which can then be nulled out with the circuit shown in *Figure 2*. The amplifier is now offset nulled independent of gain.

COMPENSATION

The variable bandwidth and slew rate of the LF152 are controlled by an RC network between the compensation pins of the amplifier as shown in *Figure 2*. R_C and C_C may be varied for optimum operating characteristics in a particular application.

Layout of accompanying circuitry may influence the value of this RC network. The lead lengths to resistors R_S and R_G should be minimized and the capacitance from these nodes should also be minimized for optimum frequency response. If $R_C = 160\Omega$ and $C_C = 0.002\mu F$ in the printed circuit board of *Figure 7*, the amplifier will be compensated for all gains from 1 to 1000. Gains from 0.1 to 10,000 may be obtained with different compensation.

GAIN ERROR AND NONLINEARITY

Gain error of the LF152 is the error between the average slope of the transfer function compared to the slope of R_S/R_G. In the LF152, the small gain error is essentially constant with gain and may be nulled out by trimming R_S.

Of the existing monolithic instrumentation amplifiers, the LF152 is among the lowest in gain nonlinearity error. Gain nonlinearity is the curvature of the transfer function from the theoretically perfect function as shown in *Figure 6*.

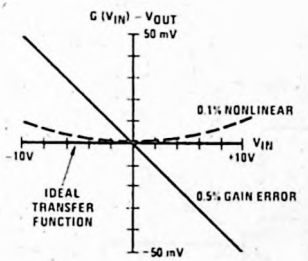


FIGURE 6. Gain Error and Nonlinearity

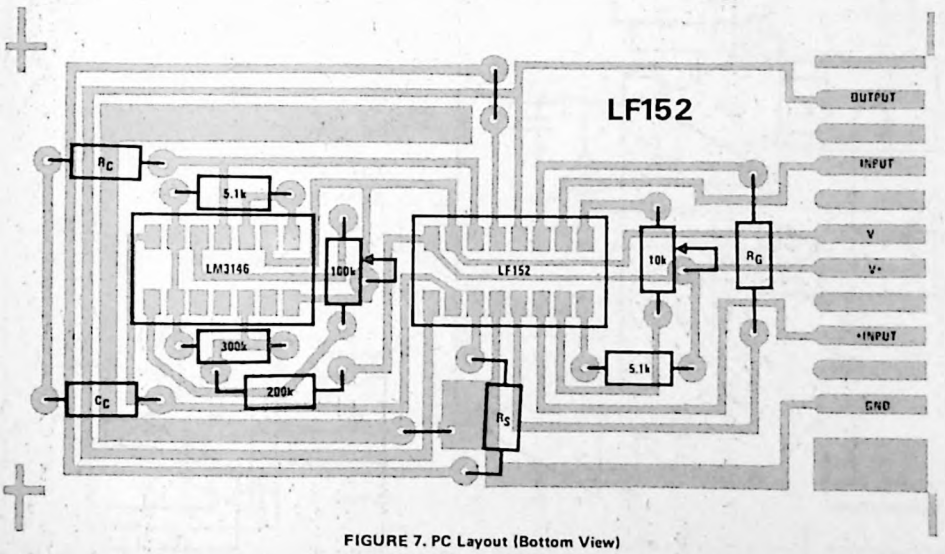
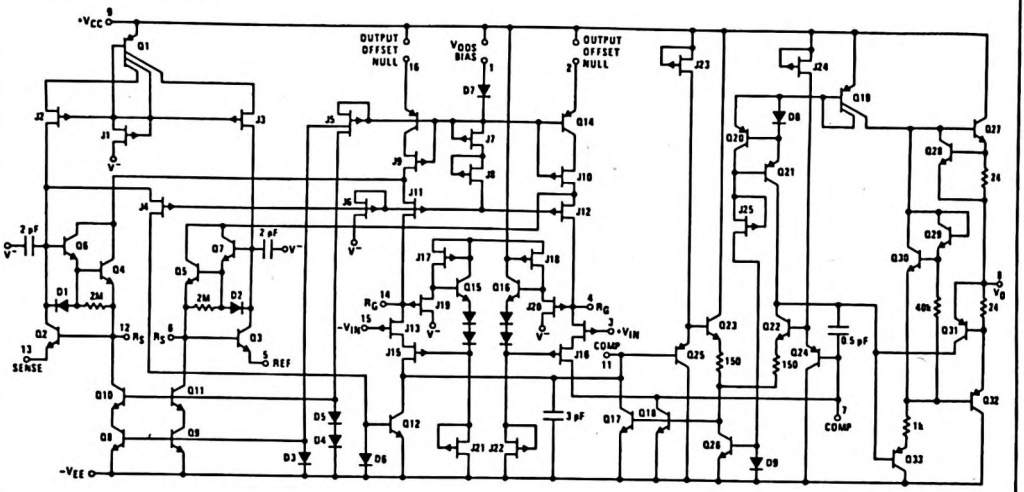


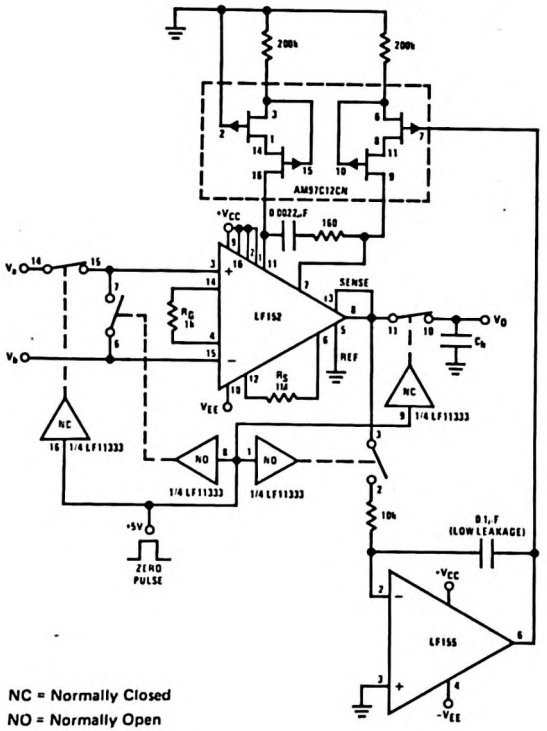
FIGURE 7. PC Layout (Bottom View)

detailed schematic



typical applications

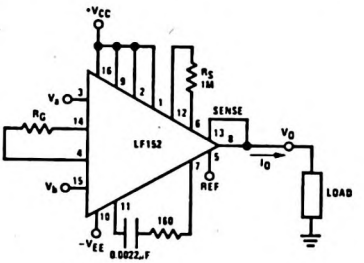
Automatic V_{IOS} Adjust ($G \geq 100$)



NC = Normally Closed
NO = Normally Open

Minimum pulse width to drive V_O to zero is 400μs.

General Purpose Instrumentation Amplifier



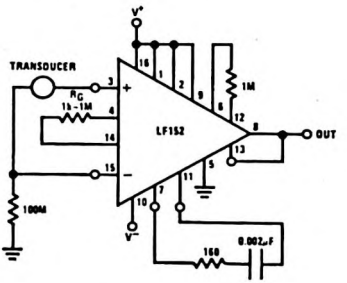
$$V_O = (V_a - V_b)\frac{R_S}{R_G} + V_{REF}$$

For $\frac{R_S}{R_G} = 1$

$V_O = V_a + V_{REF} - V_b$

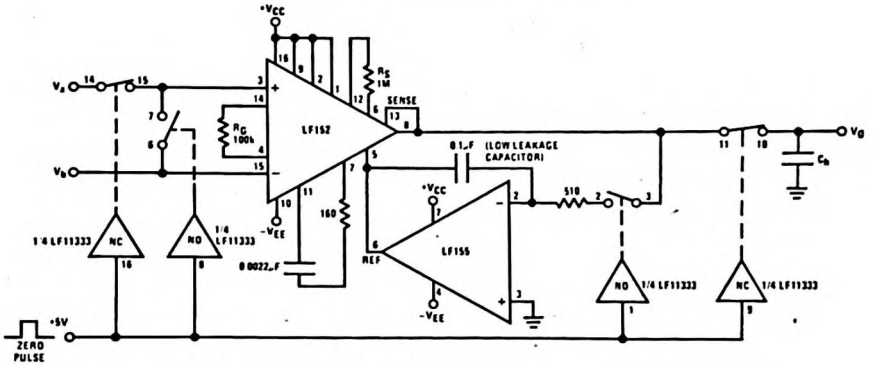
I_O SOURCE OR SINK ≤ 5 mA

Isolated Sensor



typical applications (con't)

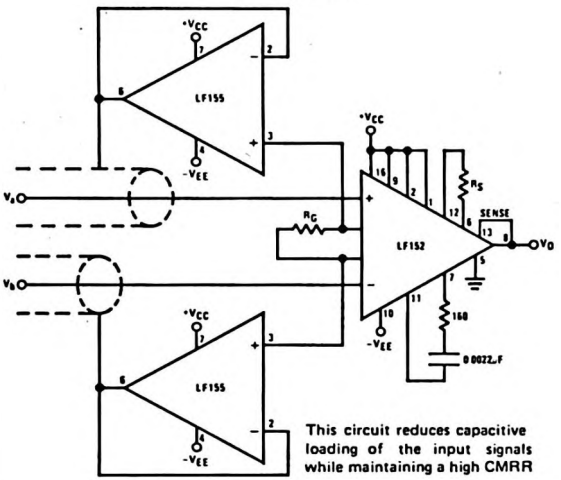
Automatic V_{OOS} Adjust (For G ≤ 100)



Minimum pulse width to drive V_O to zero is 450μs

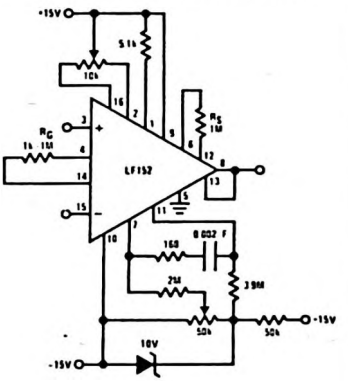
NC = Normally Closed
NO = Normally Open

AC Active Guard Drive

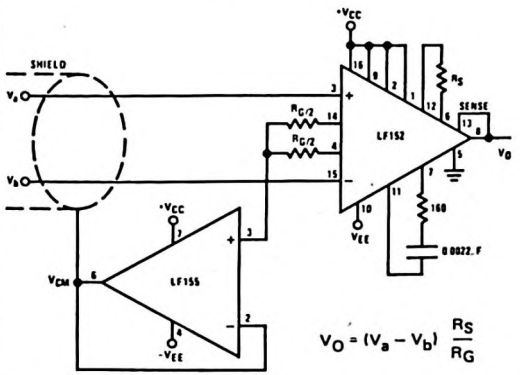


This circuit reduces capacitive loading of the input signals while maintaining a high CMRR

Typical Circuit with Full Offset Adjust



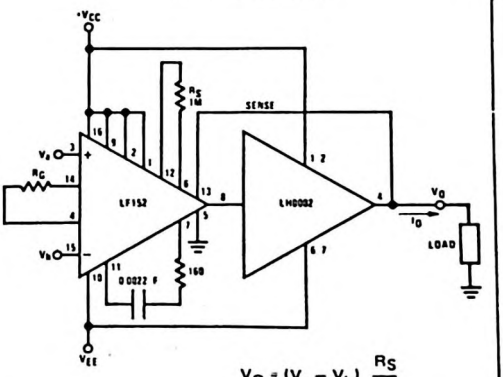
Active Guard Drive



$$V_O = (V_a - V_b)\frac{R_S}{R_G}$$

(This circuit reduces the degradation of CMRR caused by the capacitance of shielded cable.)

Output Current Boost

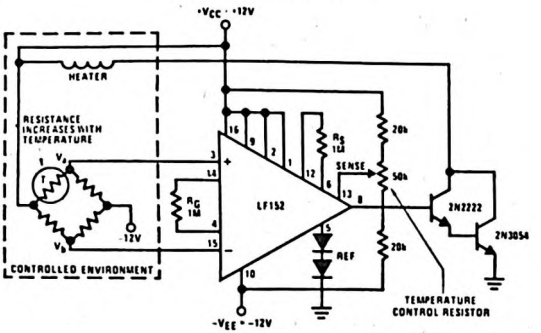


$$V_O = (V_a - V_b)\frac{R_S}{R_G}$$

I_O SOURCE OR SINK ≤ 95 mA

typical applications (con't)

Temperature Control Circuit

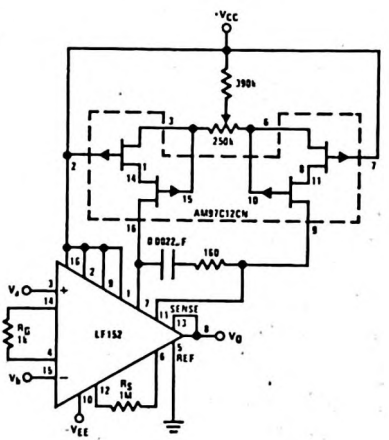


Under balanced conditions, $V_{SENSE} - V_{REF}$ appears across R_S, $V_a - V_b$ appears across R_G and $I_{RG} = I_{RS}$.

$$\frac{V_a - V_b}{R_G} = \frac{V_{SENSE}}{R_S} \text{ or } V_a - V_b = V_{SENSE}\,\frac{R_G}{R_S}$$

V_{SENSE} is fixed by the temperature control resistor and R_G/R_S is constant. The LF152 is used as a comparator with a feedback loop closed through the heater and the temperature dependent resistor. If $V_a - V_b > V_{SENSE}\ R_G/R_S$. The output goes high turning "ON" the heater. If $V_a - V_b < V_{SENSE}\ R_G/R_S$. The output goes low turning "OFF" the heater.

Alternate Input Offset (V_{IOS}) Adjust Scheme



definition of terms

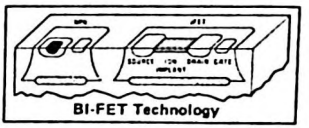
G **Closed loop gain.** $G = R_S/R_G$

G_E **Gain error.** A rotational error of the transfer function about the origin.

G_{NL} **Gain nonlinearity.** Curvature of the transfer function.

V_{OS} **Offset voltage.** Voltage offset of the transfer function at the origin $V_{OS} = V_{IOS}(G) + V_{OOS}$

National Semiconductor



LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B low supply current
LF156, LF156A, LF256, LF356, LF356A, LF356B wide band
LF157, LF157A, LF257, LF357, LF357A, LF357B wide band decompensated (AV_{MIN} = 5)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

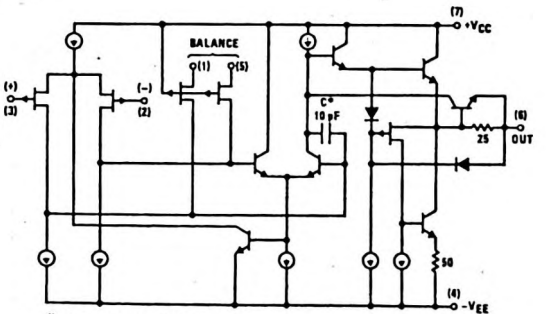
(LF155A, LF156A, LF157A)

- Low input bias current — 30 pA
- Low input offset current — 3 pA
- High input impedance — $10^{12}\Omega$
- Low input offset voltage — 1 mV
- Low input offset voltage temperature drift — 3μV/°C
- Low input noise current — 0.01 pA/√Hz
- High common-mode rejection ratio — 100 dB
- Large dc voltage gain — 106 dB

Uncommon Features

	LF155A	LF156A	LF157A (A_V = 5)*	UNITS
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/√Hz

Simplified Schematic



*C = 2 pF on LF157

Absolute Maximum Ratings

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7 LF355B/6B/7B	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)				
T_{jMAX}				
(H and J Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W	150°C/W
(J Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	140°C/W	140°C/W	140°C/W	140°C/W
(N Package) P_d			500 mW	500 mW
θ_{jA}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = ±15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = ±10V$, $R_L = 2k$							
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = ±15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = ±15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = ±15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = ±15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A; $A_V = 1$,	3	5		10	12					V/µs
		LF157A; $A_V = 5$							40	50		V/µs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		25			12			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		±10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6: $A_V = 1$,	5	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20		12		12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155/6/7	LF255/6/7	LF355A/6A/7A	LF355B/6B/7B	LF355/6/7
Supply Voltage, V_S	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm18V$	$\pm15V \le V_S \pm20V$	$V_S = \pm15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA} Pd$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

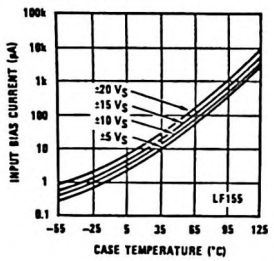
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

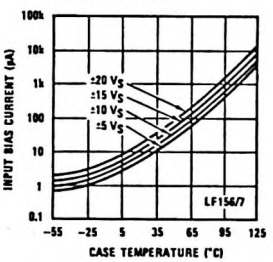
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

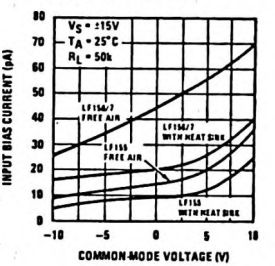
Input Bias Current



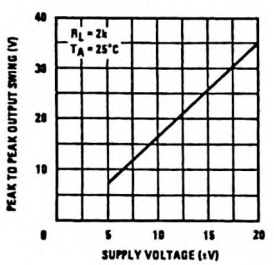
Input Bias Current



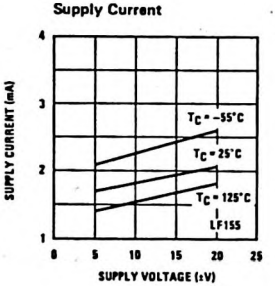
Input Bias Current



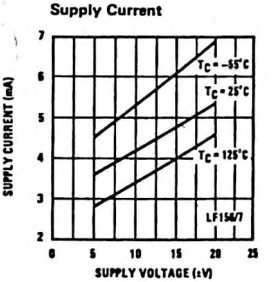
Voltage Swing



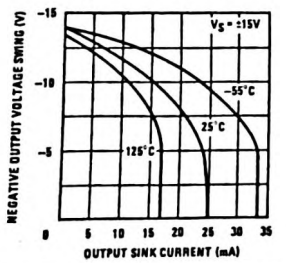
Supply Current



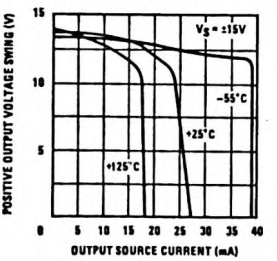
Supply Current



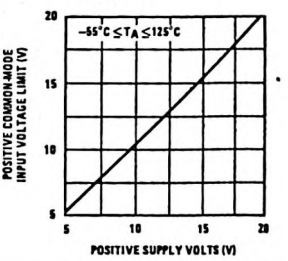
Negative Current Limit



Positive Current Limit

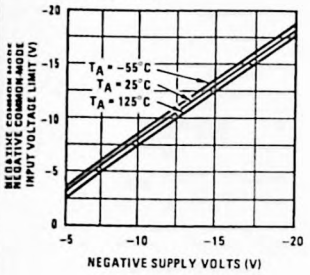


Positive Common-Mode Input Voltage Limit

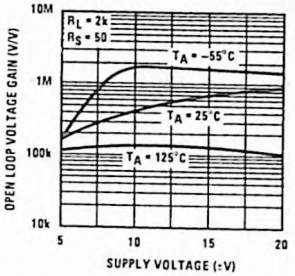


Typical DC Performance Characteristics (Continued)

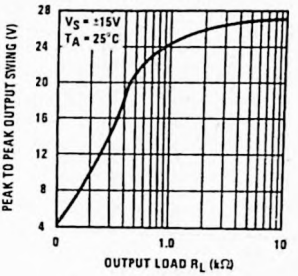
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

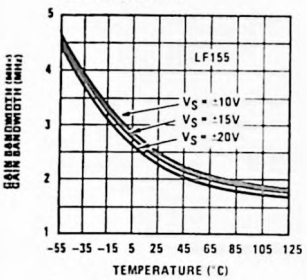


Output Voltage Swing

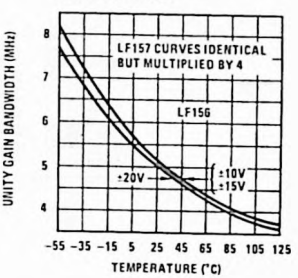


Typical AC Performance Characteristics

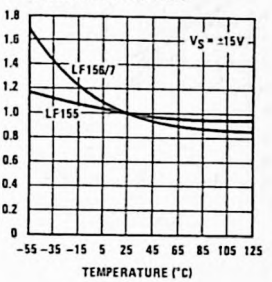
Gain Bandwidth



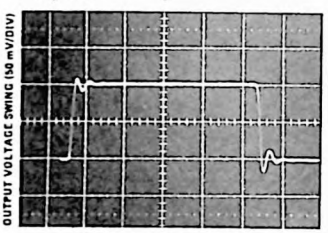
Gain Bandwidth



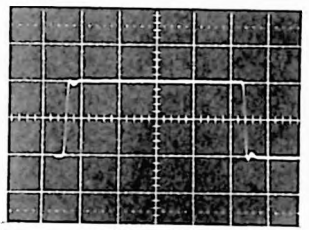
Normalized Slew Rate



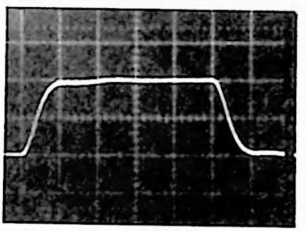
LF155 Small Signal Pulse Response, $A_V = +1$



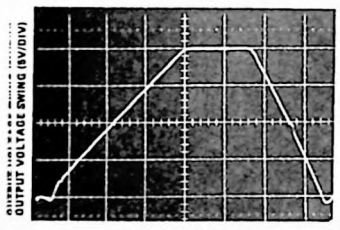
LF156 Small Signal Pulse Response, $A_V = +1$



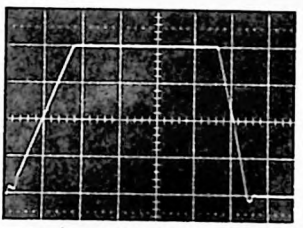
LF157 Small Signal Pulse Response, $A_V = +5$



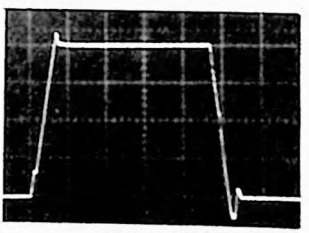
LF155 Large Signal Pulse Response, $A_V = +1$



LF156 Large Signal Pulse Response, $A_V = +1$

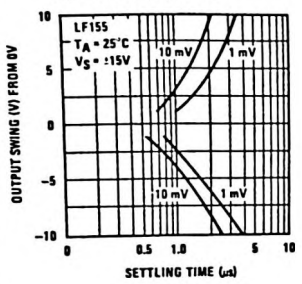


LF157 Large Signal Pulse Response, $A_V = +5$

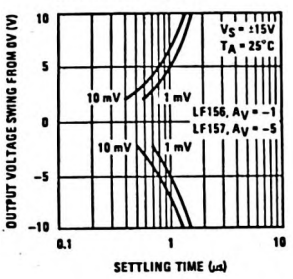


Typical AC Performance Characteristics (Continued)

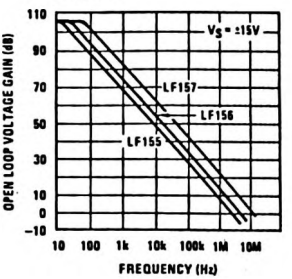
Inverter Settling Time



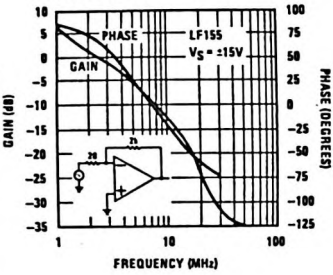
Inverter Settling Time



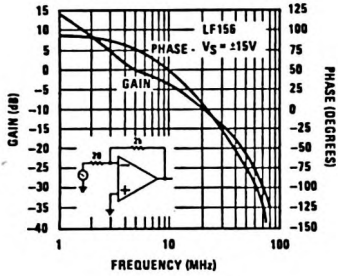
Open Loop Frequency Response



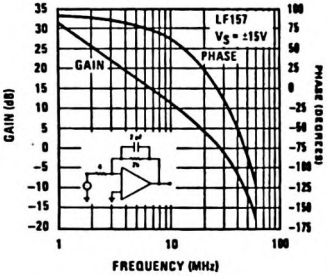
Bode Plot



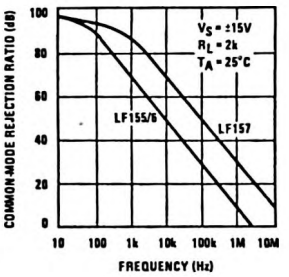
Bode Plot



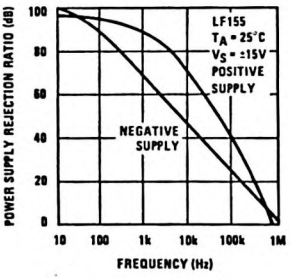
Bode Plot



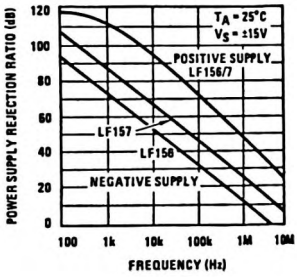
Common-Mode Rejection Ratio



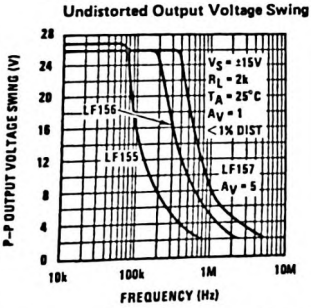
Power Supply Rejection Ratio



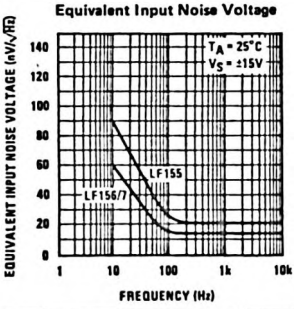
Power Supply Rejection Ratio



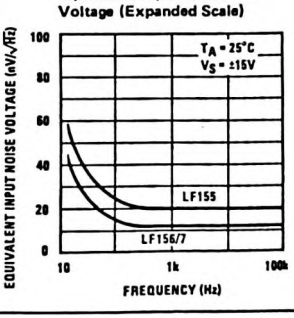
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

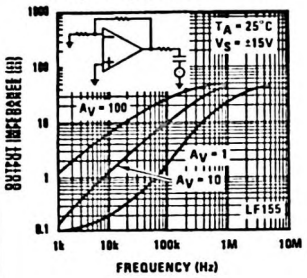


Equivalent Input Noise Voltage (Expanded Scale)

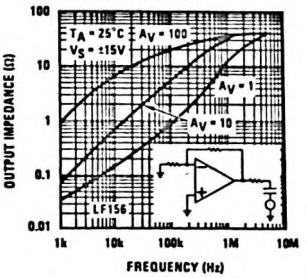


Typical AC Performance Characteristics (Continued)

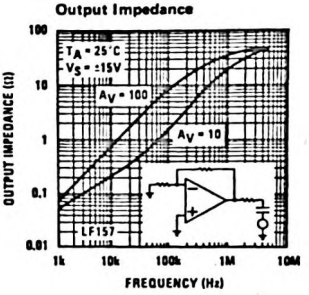
Output Impedance



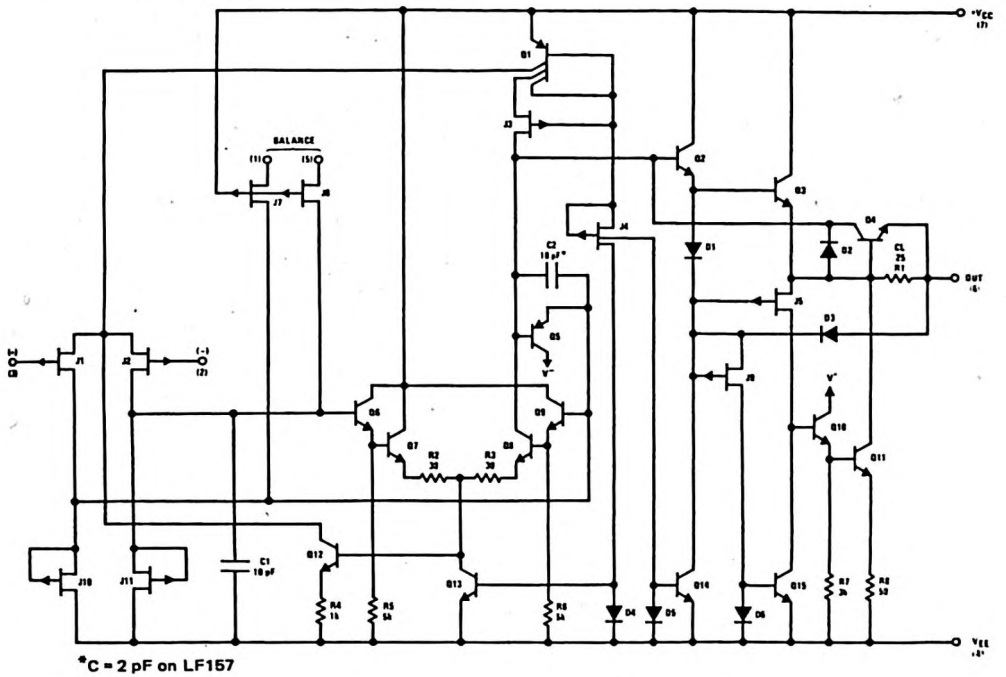
Output Impedance



Output Impedance



Detailed Schematic



*C = 2 pF on LF157

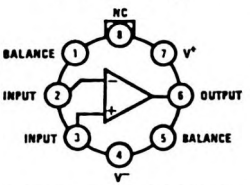
Connection Diagrams (Top Views)

Order Number

LF155AH	LF156AH	LF157AH
LF155H	LF156H	LF157H
LF255H	LF256H	LF257H
LF355AH	LF356AH	LF357AH
LF355H	LF356H	LF357H

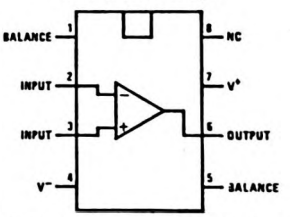
See NS Package H08B

Metal Can Package



Note 4: Pin 4 connected to case.

Dual-In-Line Package



Order Number LF355N, LF356N or LF357N
See NS Package N08A

Order Number LF355J, LF356J or LF357J
See NS Package J08A

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

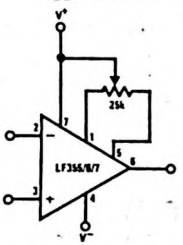
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

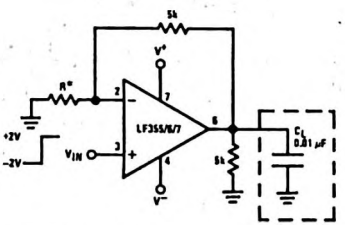
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



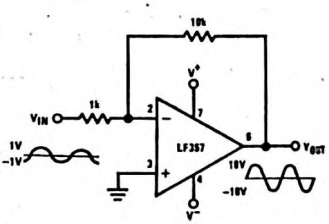
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\ \mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≈ 5 μs

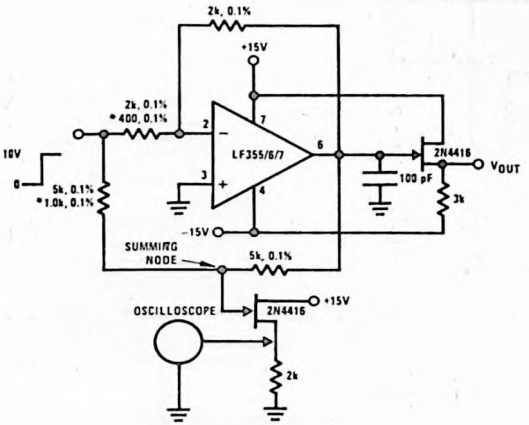
LF157. A Large Power BW Amplifier



For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

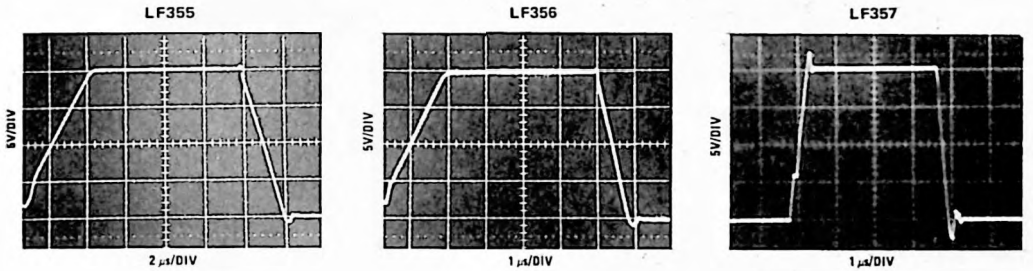
Typical Applications

Settling Time Test Circuit

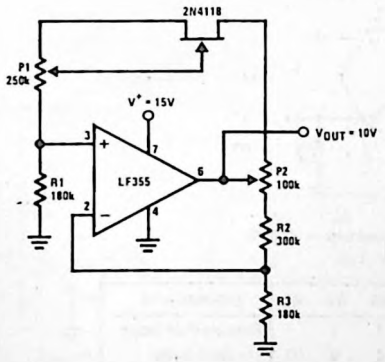


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



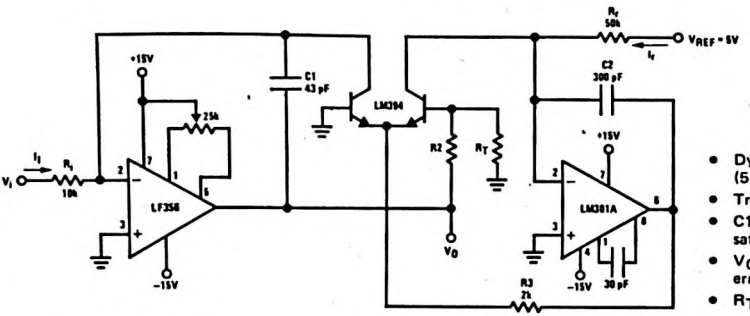
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^\circ C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

Typical Applications (Continued)

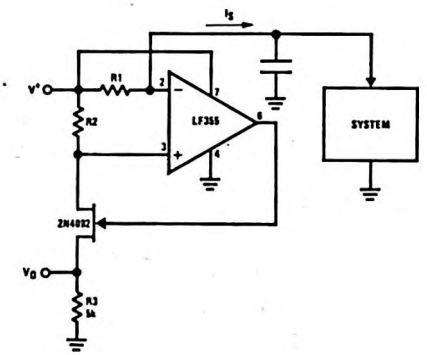
Fast Logarithmic Converter



- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

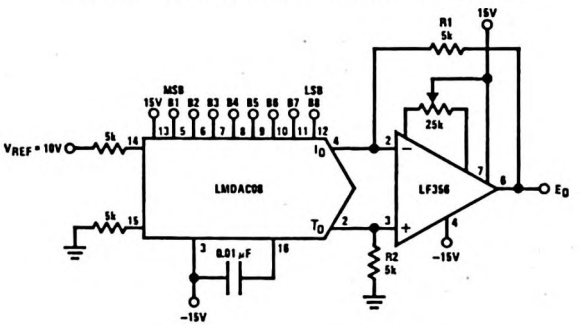
$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)}$$

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low supply current

8-Bit D/A Converter with Symmetrical Offset Binary Operation

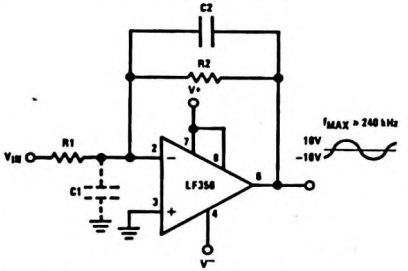


- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

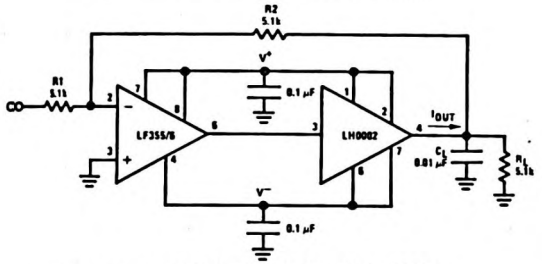
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



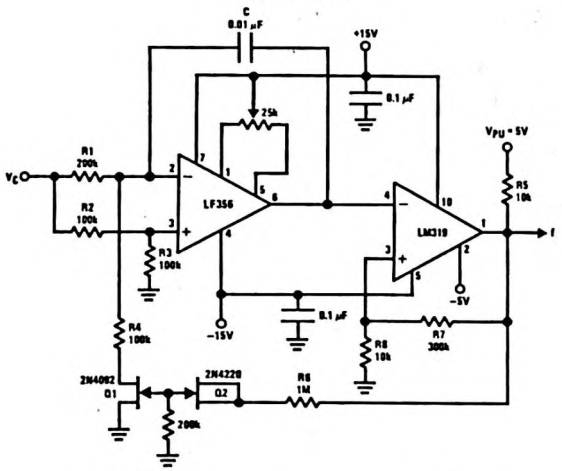
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

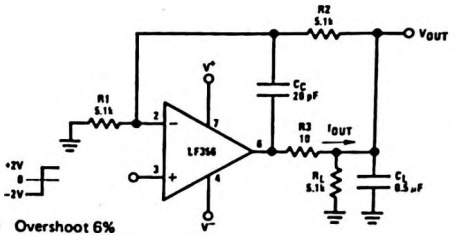
3 Decades VCO



$$f = \frac{V_C\,(R8+R7)}{[8\,V_{PU}\,R8\,R1]\,C},\ 0 \leq V_C \leq 30V,\ 10\text{ Hz} \leq f \leq 10\text{ kHz}$$

R1, R4 matched. Linearity 0.1% over 2 decades.

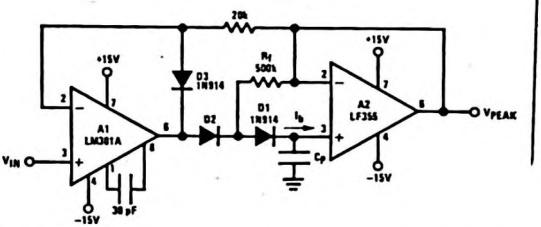
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

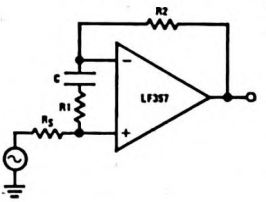
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ \text{V/µs} = 0.04\ \text{V/µs (with } C_L \text{ shown)}$$

Low Drift Peak Detector



- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_F.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< 1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



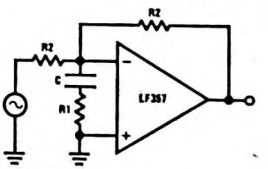
$$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3\,dB} \approx 5$ MHz

Inverting Unity Gain for LF157



$$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$$

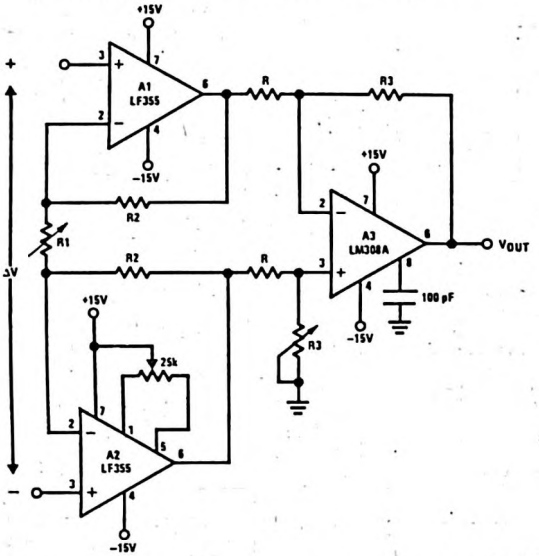
$$R1 = \frac{R2}{4}$$

$A_{V(DC)} = -1$

$f_{-3\,dB} \approx 5$ MHz

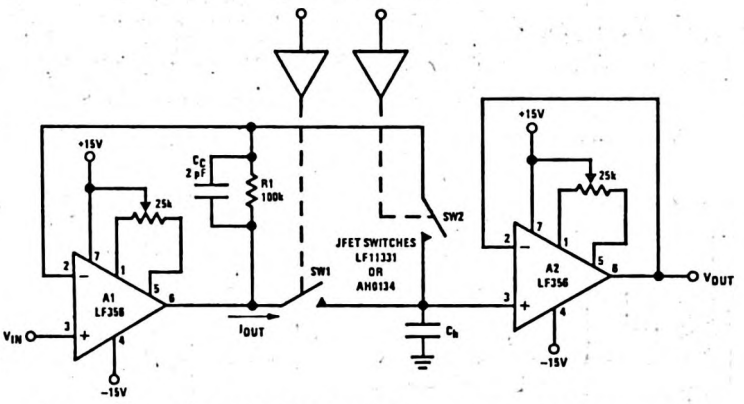
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

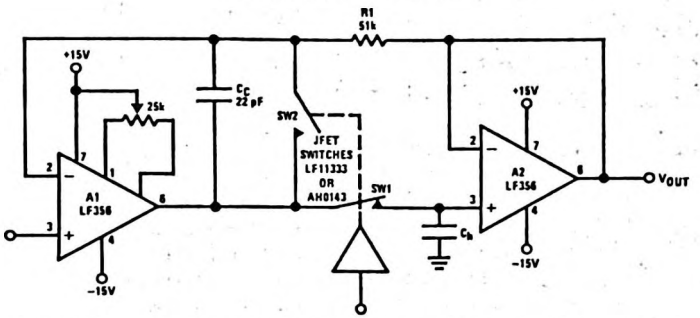
  $T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$ provided that:

  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$
- LF156 developes full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

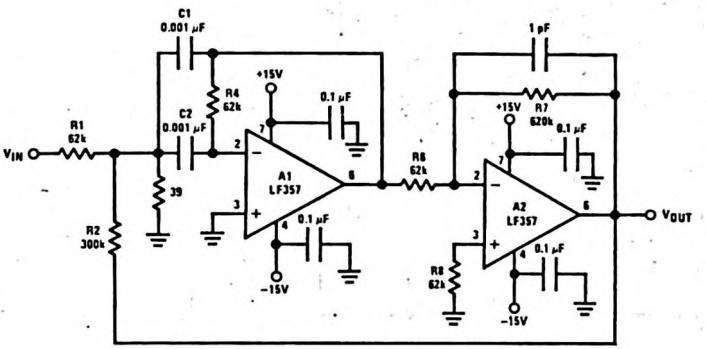
Typical Applications (Continued)

High Accuracy Sample and Hold



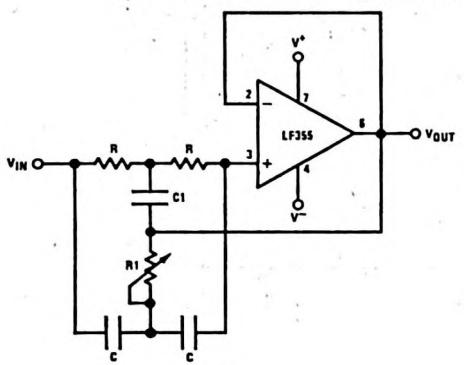
- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter



- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz
- $\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 µs

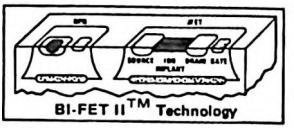
High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

National Semiconductor

LF347 Wide Bandwidth Quad JFET Input Operational Amplifier



General Description

The LF347 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LF348 and LM324 designs.

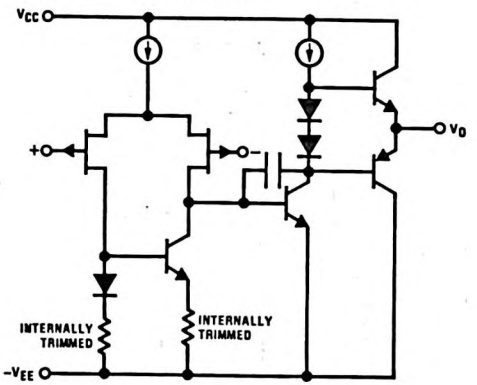
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

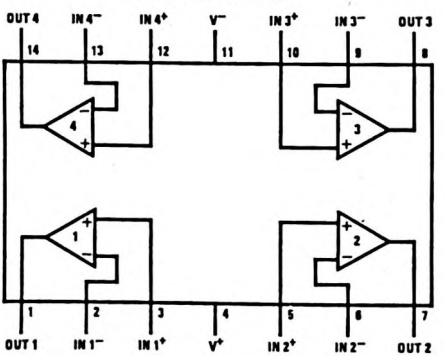
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LF347N, LF347AN or LF347BN
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	50		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50	100		50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 125°C/W junction to ambient or 95°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: P_D max rating cannot be exceeded.

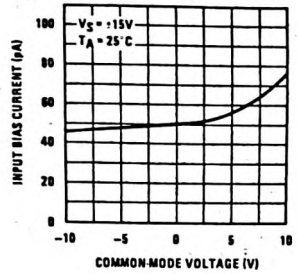
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

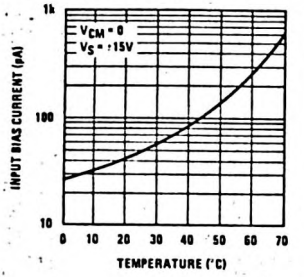
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

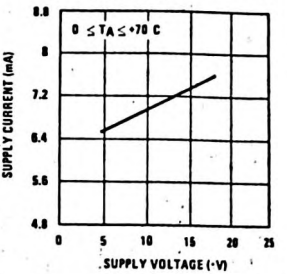
Input Bias Current



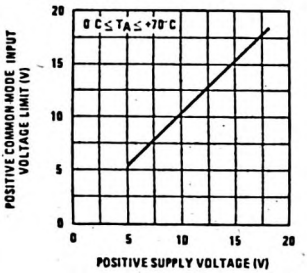
Input Bias Current



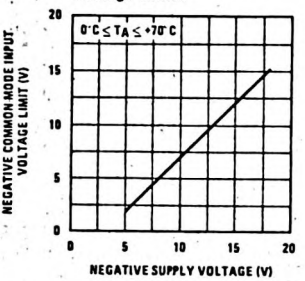
Supply Current



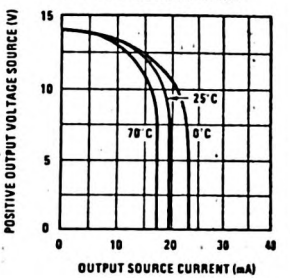
Positive Common-Mode Input Voltage Limit



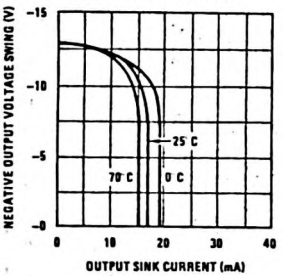
Negative Common-Mode Input Voltage Limit



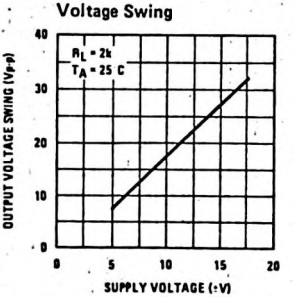
Positive Current Limit



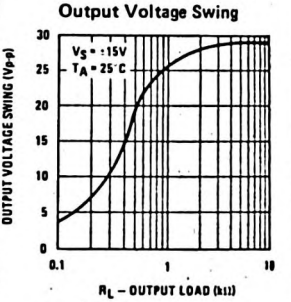
Negative Current Limit



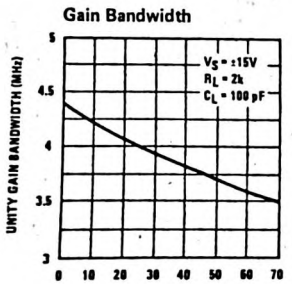
Voltage Swing



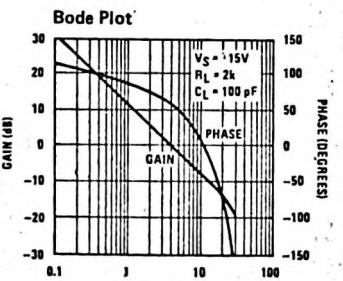
Output Voltage Swing



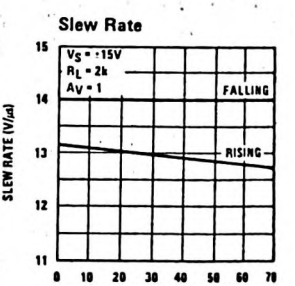
Gain Bandwidth



Bode Plot

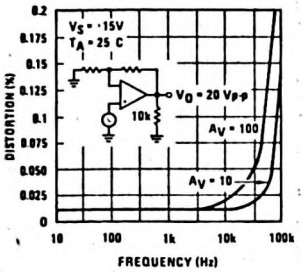


Slew Rate

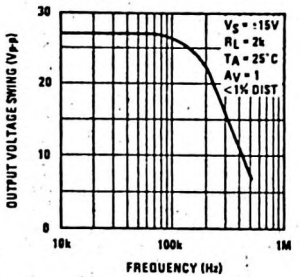


Typical Performance Characteristics (Continued)

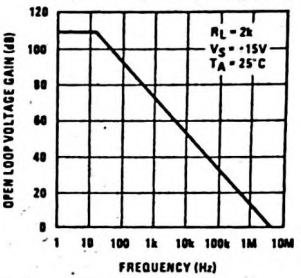
Distortion vs Frequency



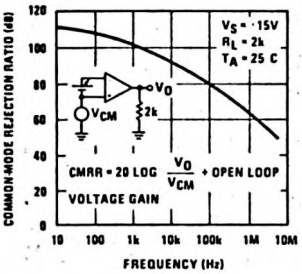
Undistorted Output Voltage Swing



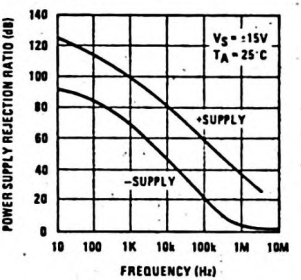
Open Loop Frequency Response



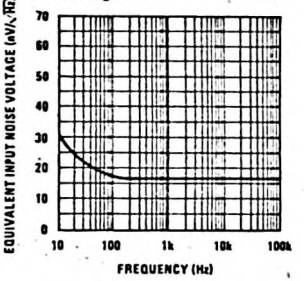
Common-Mode Rejection Ratio



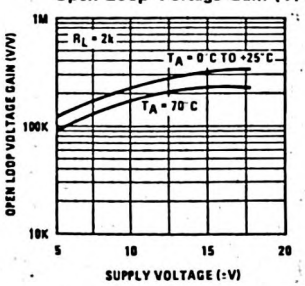
Power Supply Rejection Ratio



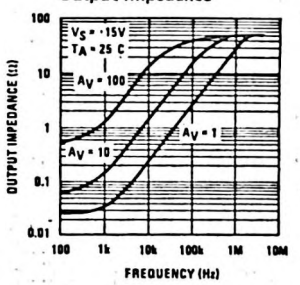
Equivalent Input Noise Voltage



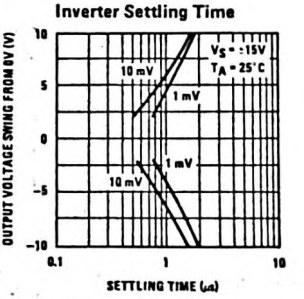
Open Loop Voltage Gain (V/V)



Output Impedance

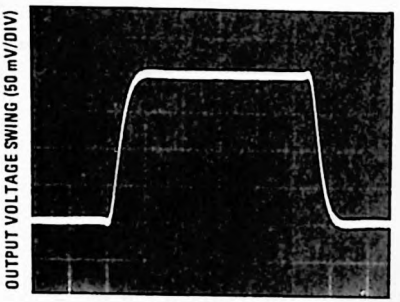


Inverter Settling Time

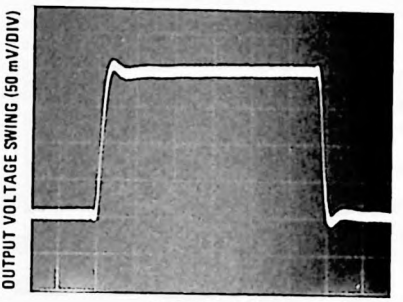


Pulse Response

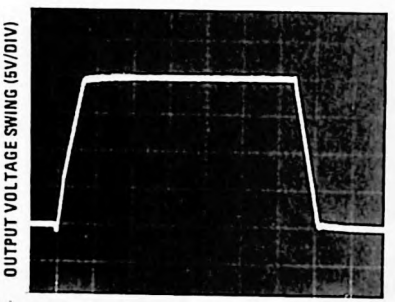
Small Signal Inverting



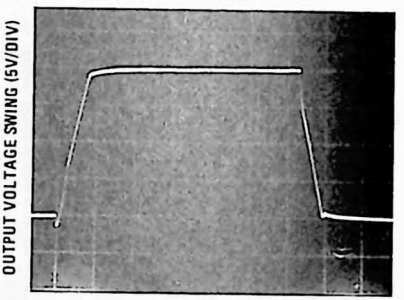
Small Signal Non-Inverting



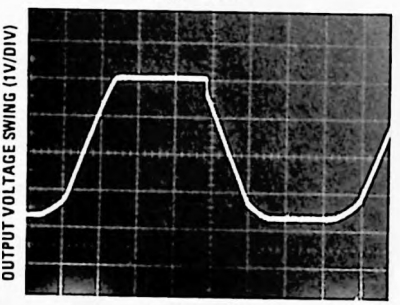
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF347 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF347 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

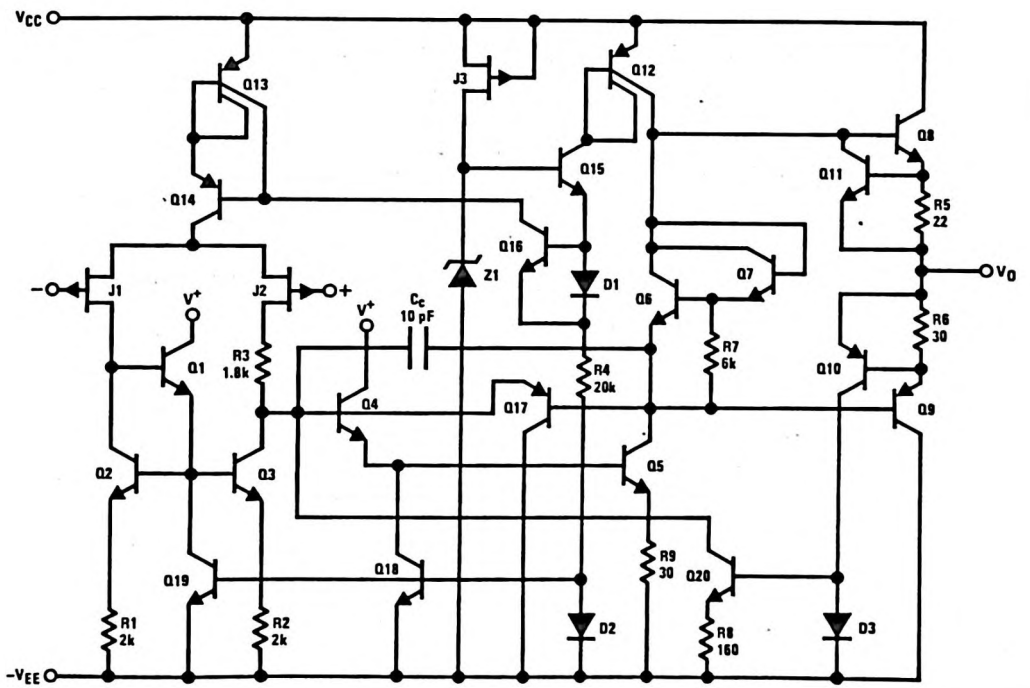
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

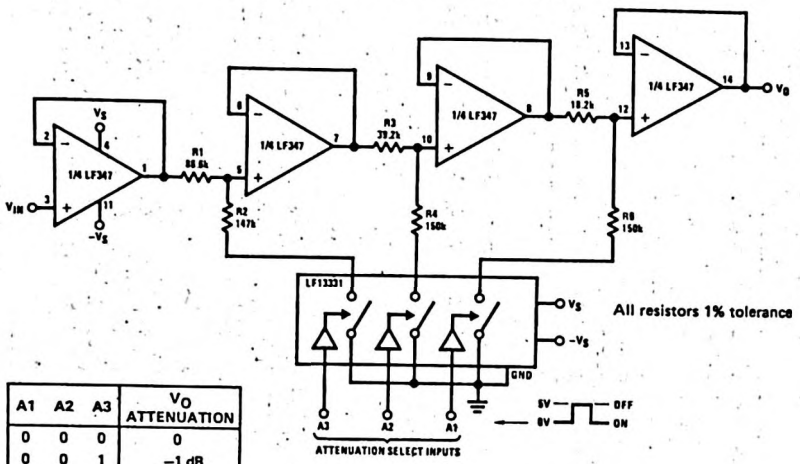
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

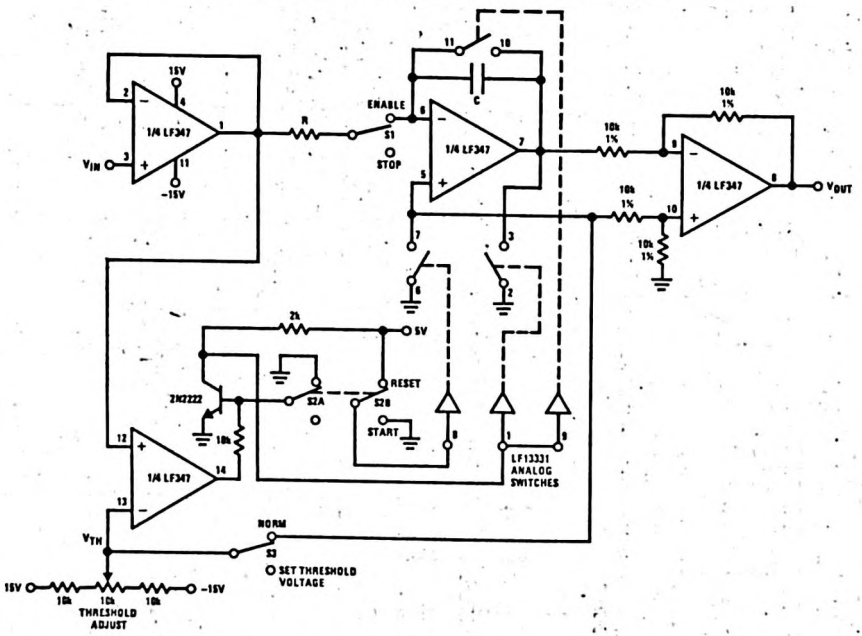
Digitally Selectable Precision Attenuator



A1	A2	A3	V_O ATTENUATION
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



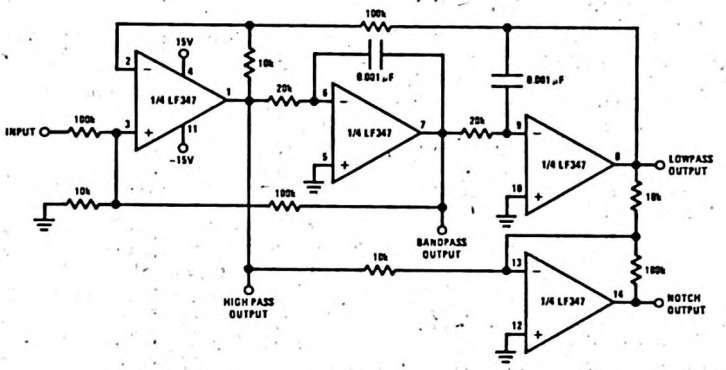
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

*Typical Applications (Continued)

Universal State Variable Filter

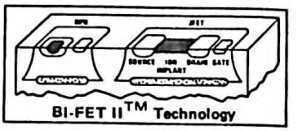


For circuit shown:
f_O = 3 kHz, f_{NOTCH} = 9.5 kHz
Q = 3.4
Passband gain:
- Highpass — 0.1
- Bandpass — 1
- Lowpass — 1
- Notch — 10

- $f_O \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM348 data sheet for design equations

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier



General Description

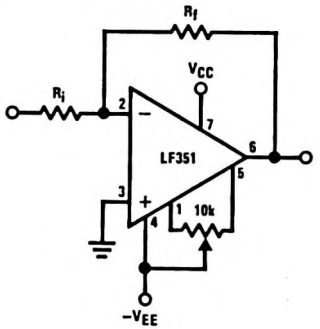
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

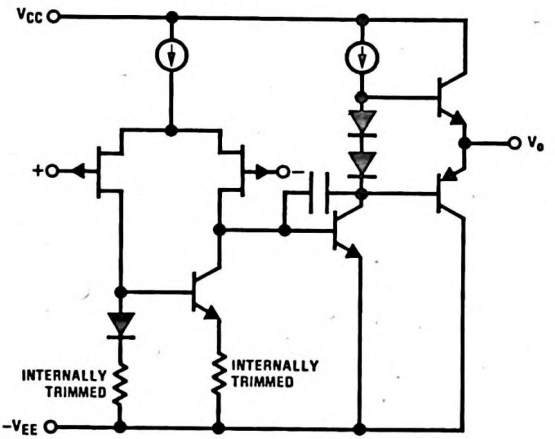
Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection

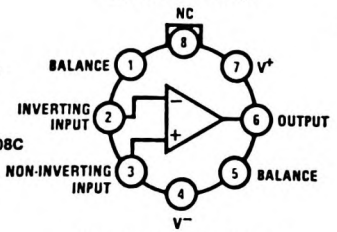


Simplified Schematic



Connection Diagrams (Top Views)

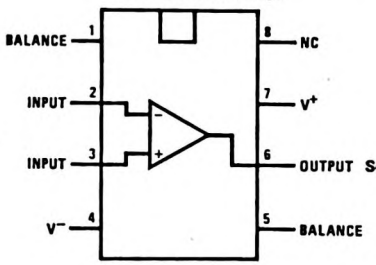
Metal Can Package



Order Number
LF351H
LF351AH
LF351BH
See NS Package H08C

Note. Pin 4 connected to case.

Dual-In-Line Package



Order Number
LF351N
LF351AN
LF351BN
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4)		25	50		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4)		50	100		50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I_S	Supply Current			1.8	2.8		1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

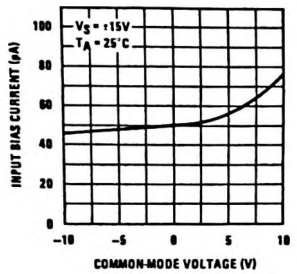
Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

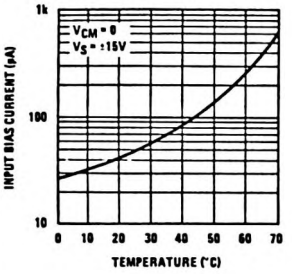
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

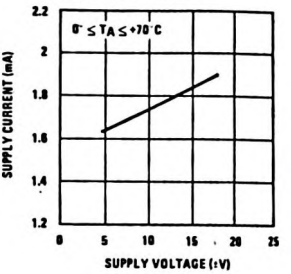
Input Bias Current



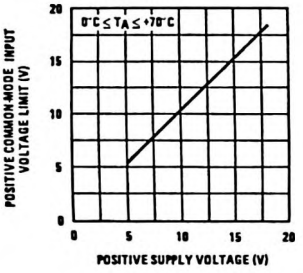
Input Bias Current



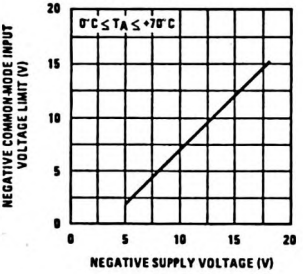
Supply Current



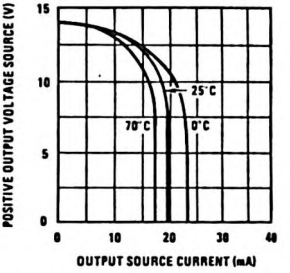
Positive Common-Mode Input Voltage Limit



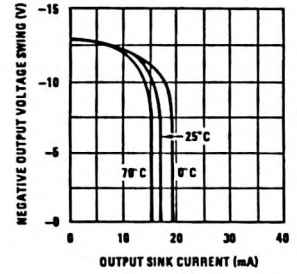
Negative Common-Mode Input Voltage Limit



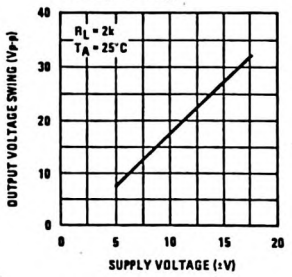
Positive Current Limit



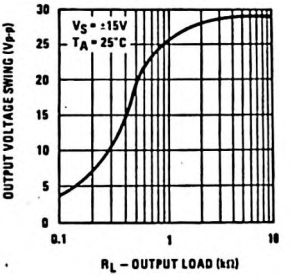
Negative Current Limit



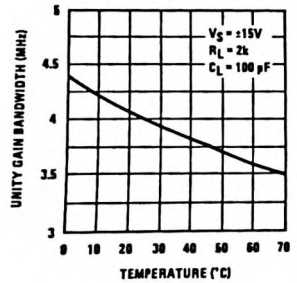
Voltage Swing



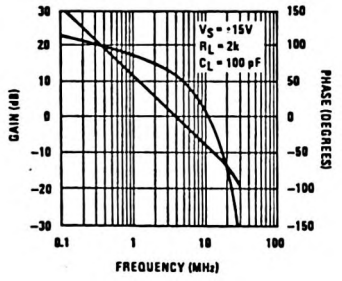
Output Voltage Swing



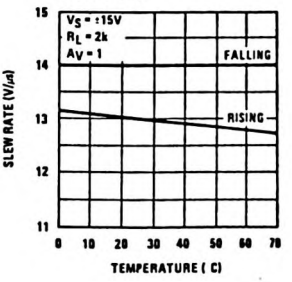
Gain Bandwidth



Bode Plot

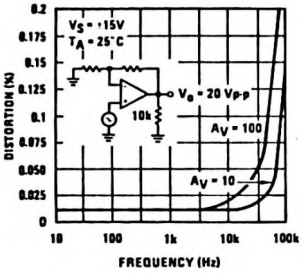


Slew Rate

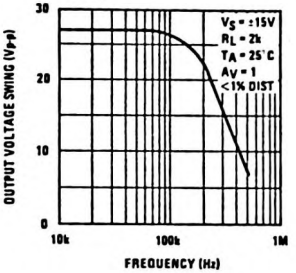


Typical Performance Characteristics (Continued)

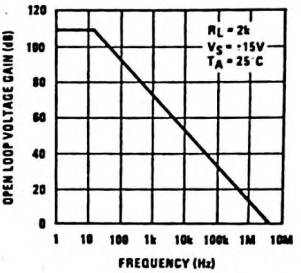
Distortion vs Frequency



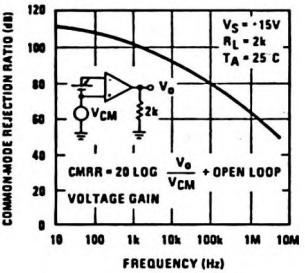
Undistorted Output Voltage Swing



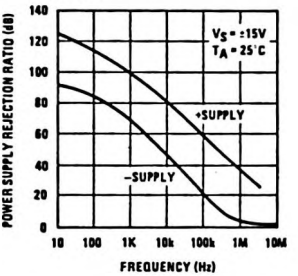
Open Loop Frequency Response



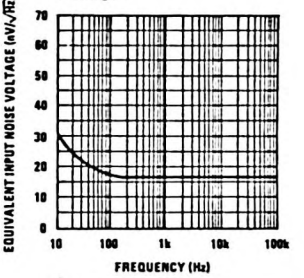
Common-Mode Rejection Ratio



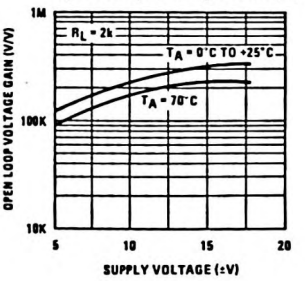
Power Supply Rejection Ratio



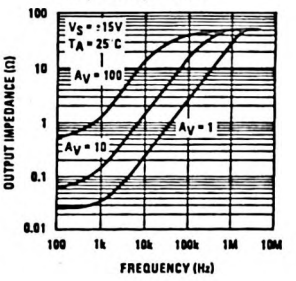
Equivalent Input Noise Voltage



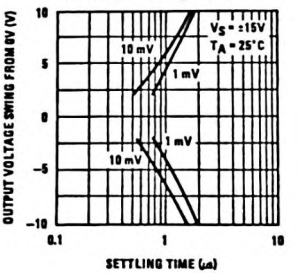
Open Loop Voltage Gain (V/V)



Output Impedance

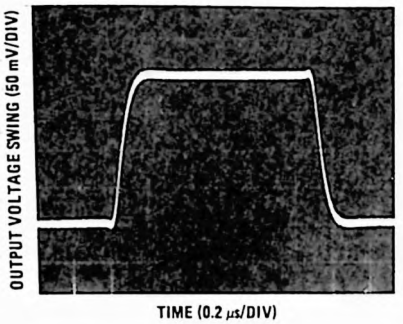


Inverter Settling Time

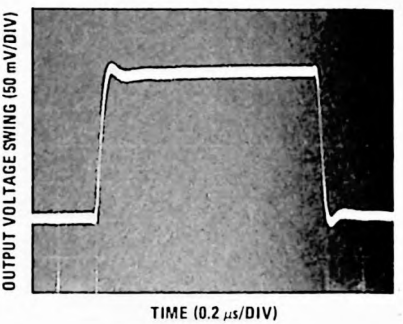


Pulse Response

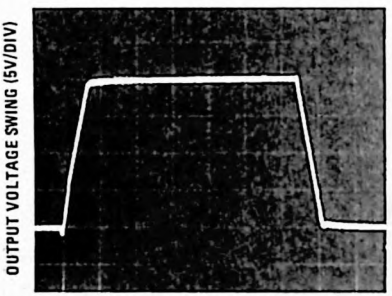
Small Signal Inverting



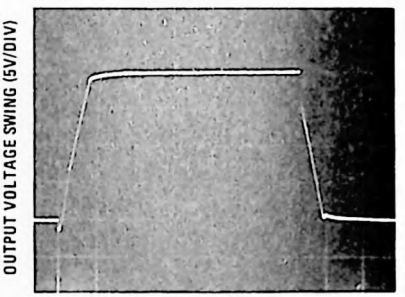
Small Signal Non-Inverting



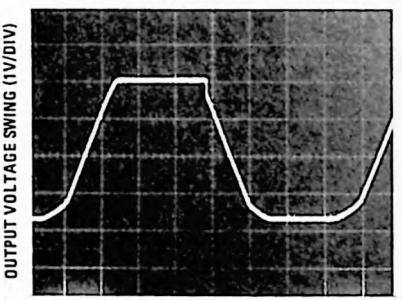
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

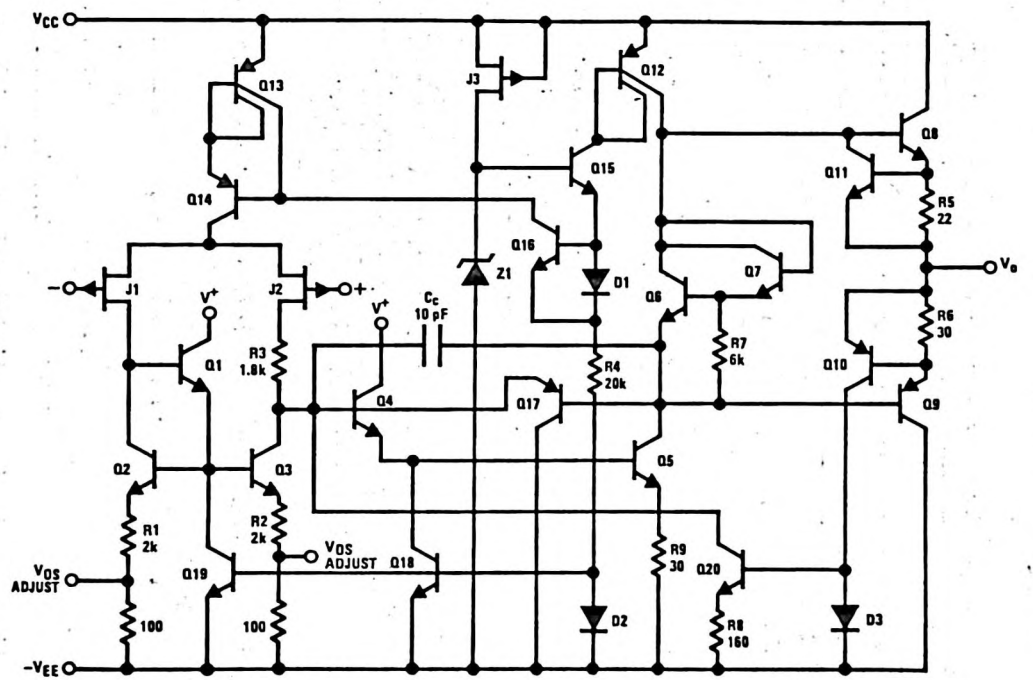
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

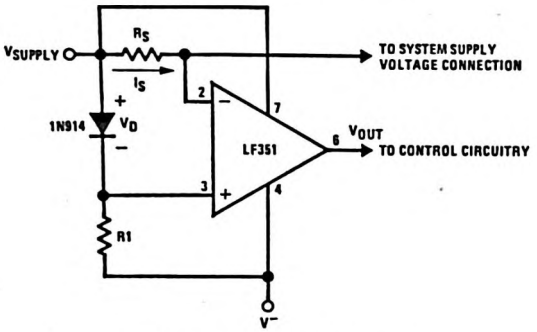
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



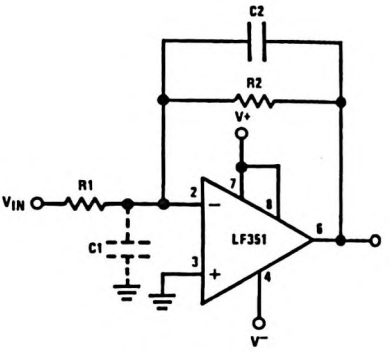
Typical Applications

Supply Current Indicator/Limiter



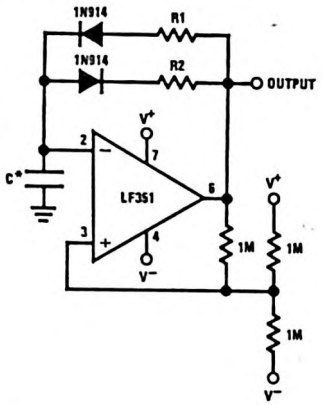
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

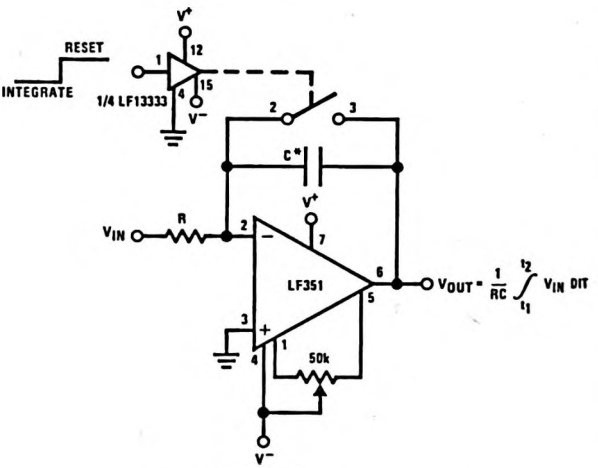


- $t_{OUTPUT\ HIGH} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

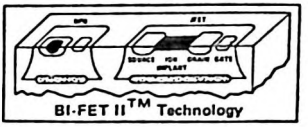


* Low leakage capacitor

- 50k pot used for less sensitive V_{OS} adjust

National Semiconductor

LF353, LF354 Wide Bandwidth Dual JFET Input Operational Amplifiers



General Description

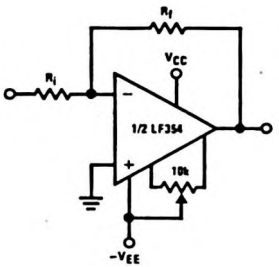
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs. The LF354 is pin compatible with the LM747 and is identical in performance to the LF353 with the additional feature of offset nulling capability.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

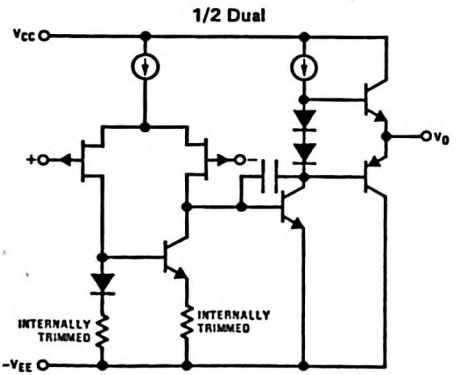
Features

■ Internally trimmed offset voltage	2 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

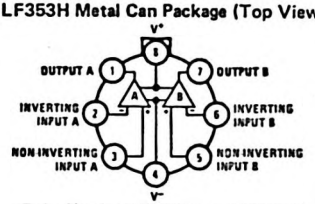


Simplified Schematic



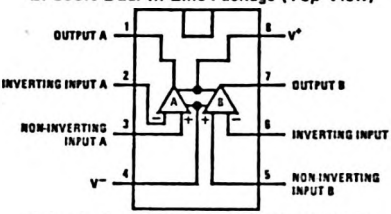
Connection Diagrams

LF353H Metal Can Package (Top View)



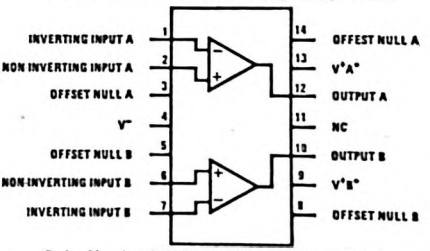
Order Number LF353AH or LF353BH
See NS Package H08C

LF353N Dual-In-Line Package (Top View)



Order Number LF353AN, LF353BN or LF353N
See NS Package N08A

LF354N Dual-In-Line Package (Top View)



Order Number LF354AN, LF354BN or LF354N
See NS Package N14A

*V^+A and V^+B are internally connected

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A, LF354A			LF353B, LF354B			LF353, LF354			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	50		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50	100		50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			3.6	5.6		3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A, LF354A			LF353B, LF354B			LF353, LF354			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 160°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

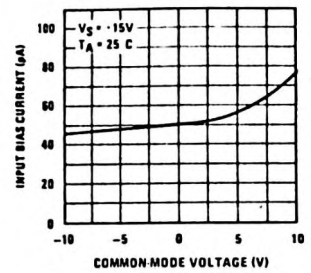
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

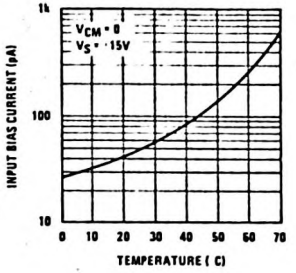
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

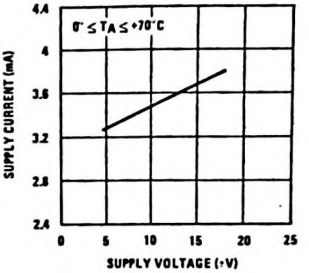
Input Bias Current



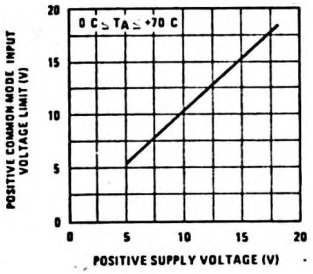
Input Bias Current



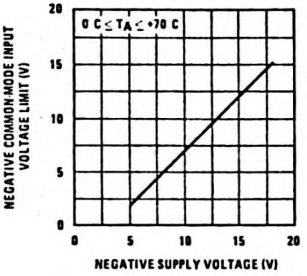
Supply Current



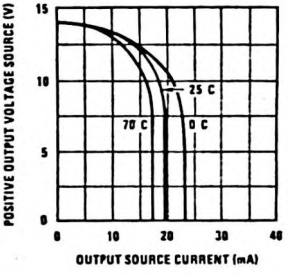
Positive Common-Mode Input Voltage Limit



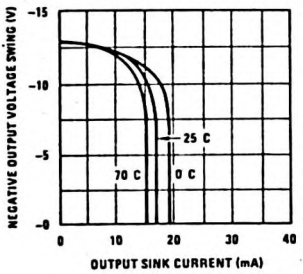
Negative Common-Mode Input Voltage Limit



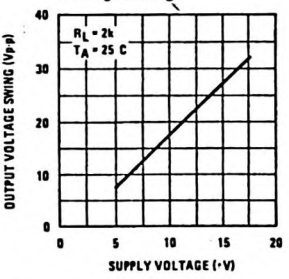
Positive Current Limit



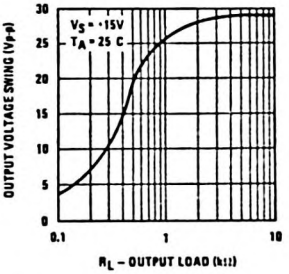
Negative Current Limit



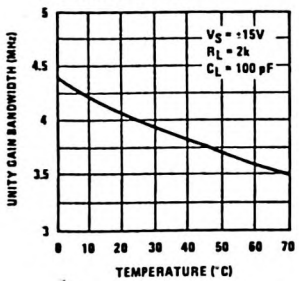
Voltage Swing



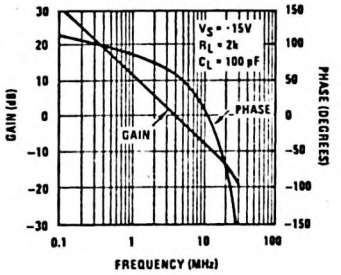
Output Voltage Swing



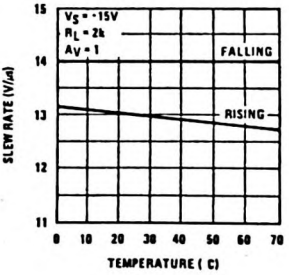
Gain Bandwidth



Bode Plot

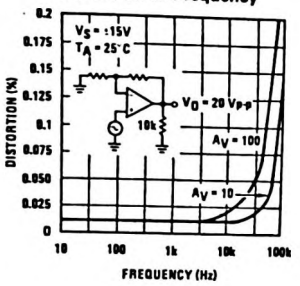


Slew Rate

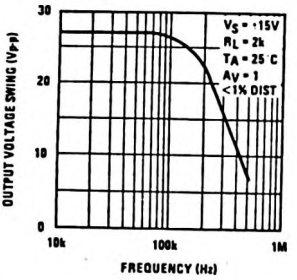


Typical Performance Characteristics (Continued)

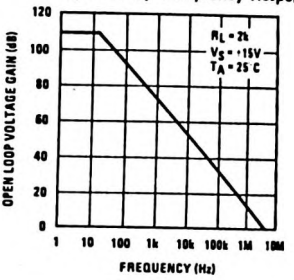
Distortion vs Frequency



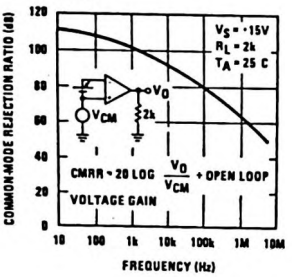
Undistorted Output Voltage Swing



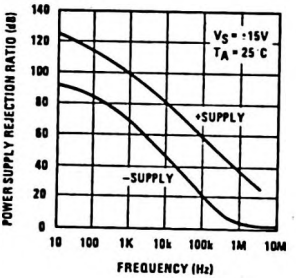
Open Loop Frequency Response



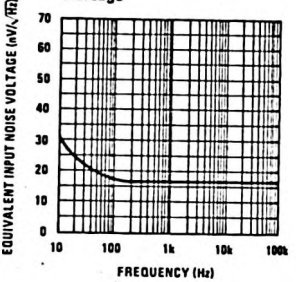
Common-Mode Rejection Ratio



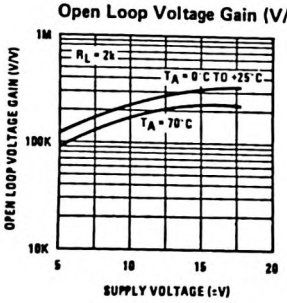
Power Supply Rejection Ratio



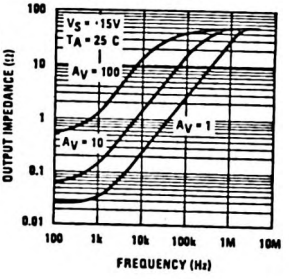
Equivalent Input Noise Voltage



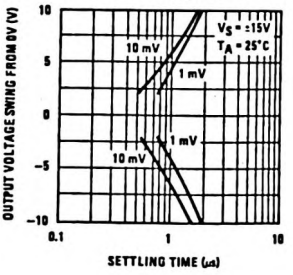
Open Loop Voltage Gain (V/V)



Output Impedance

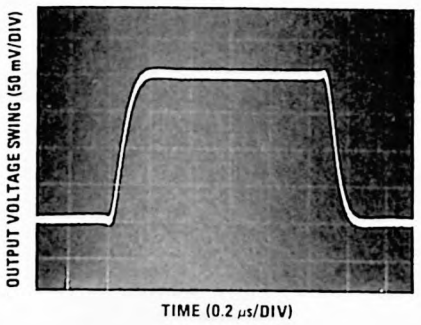


Inverter Settling Time

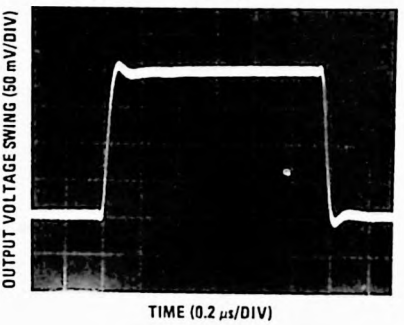


Pulse Response

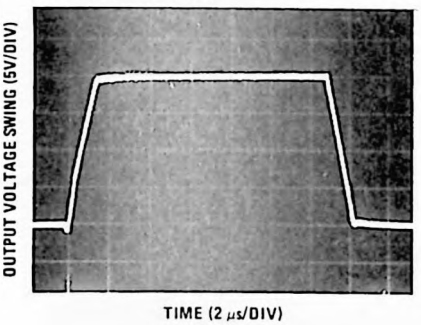
Small Signal Inverting



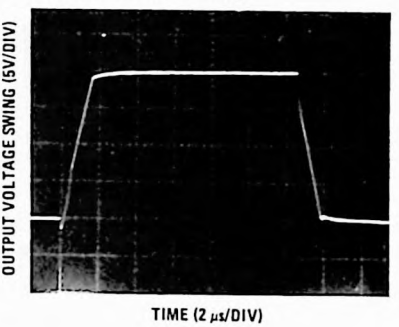
Small Signal Non-Inverting



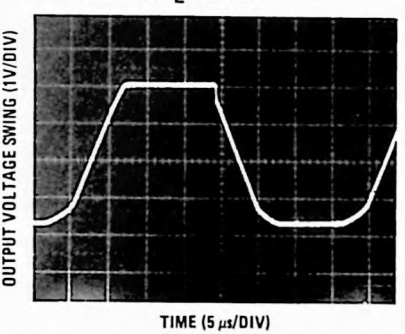
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

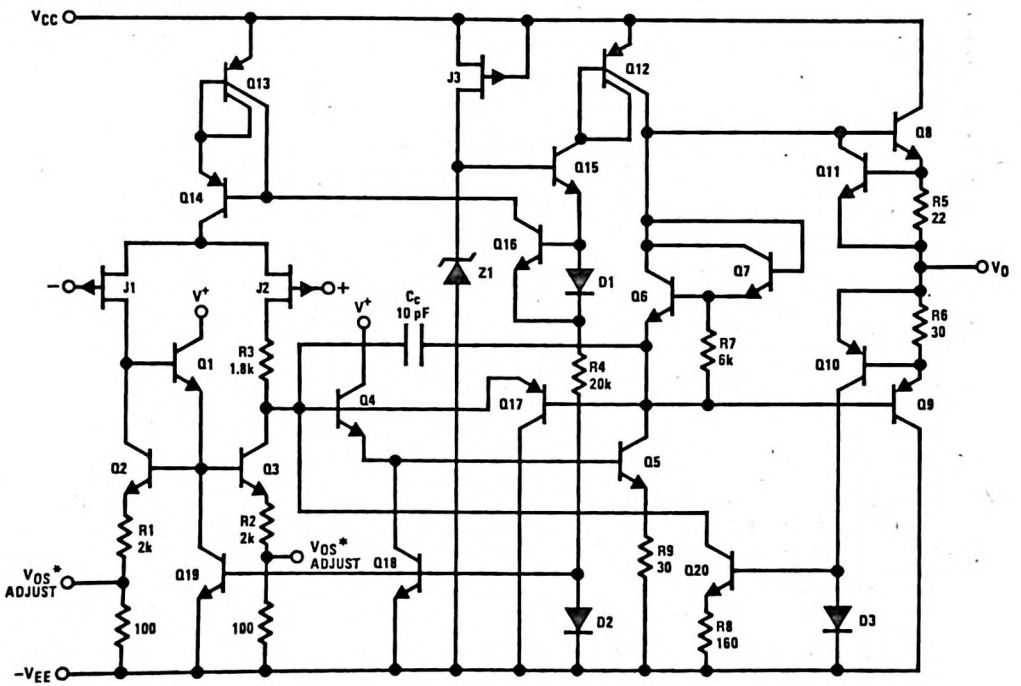
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

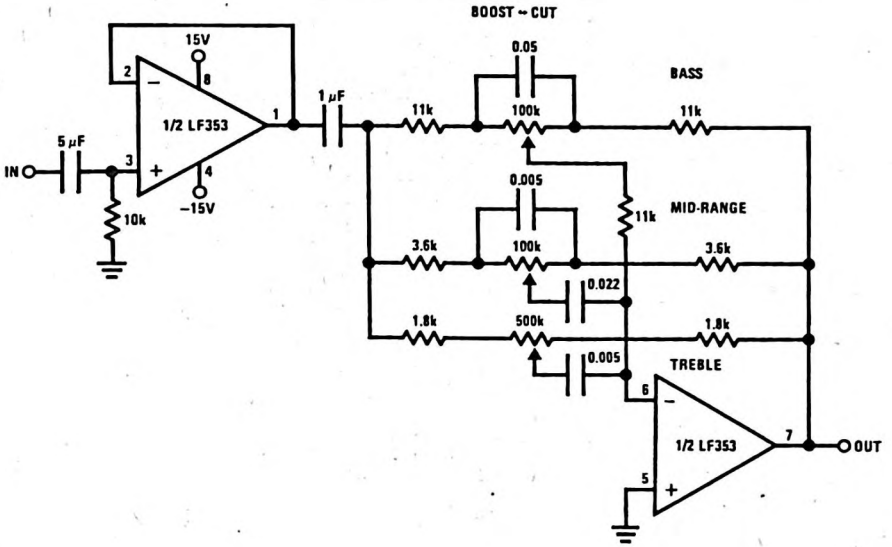
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

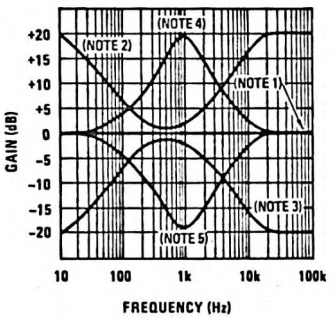
Detailed Schematic



Typical Applications

Three-Band Active Tone Control



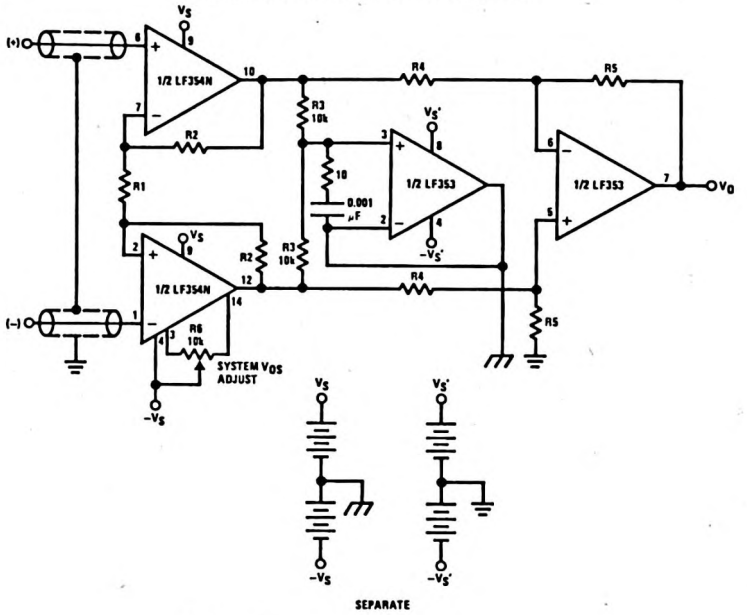


Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

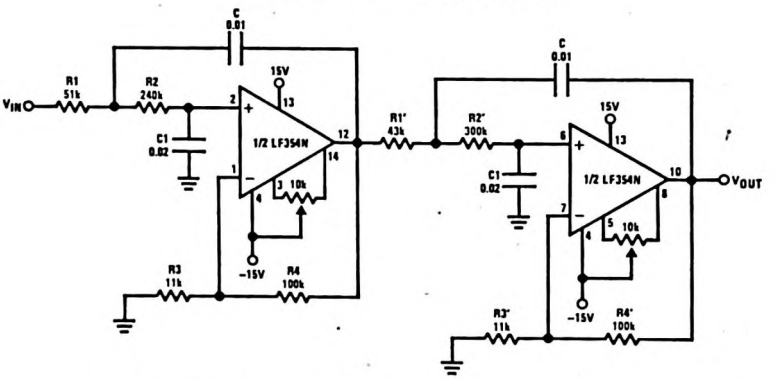
⏚ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

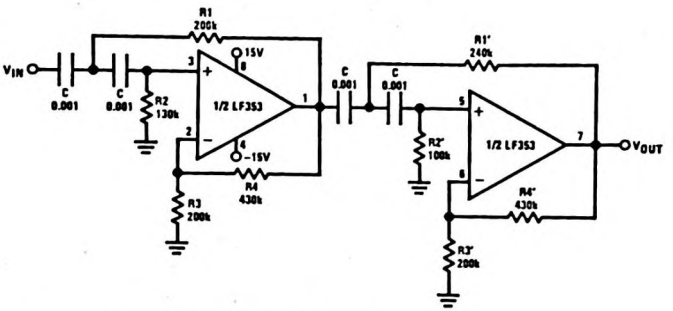
Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_C) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

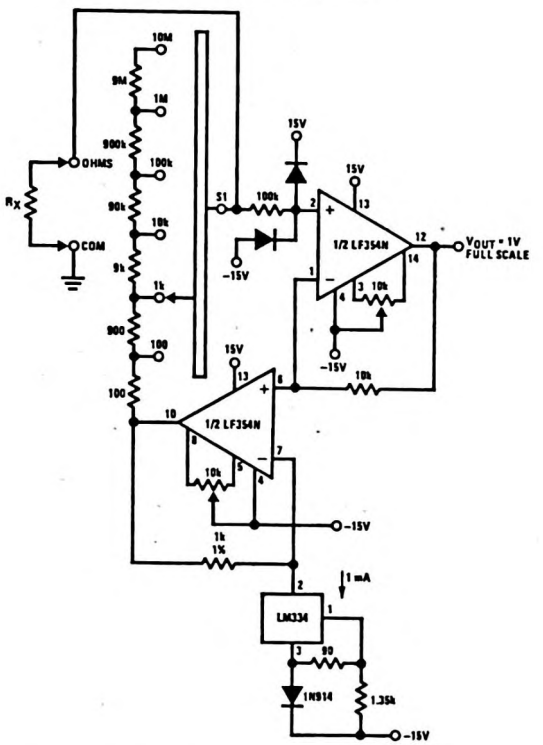
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency (f_C) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = $(1 + R4/R3)(1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

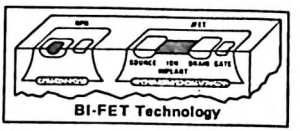
Ohms to Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 10 of the LF354.

National Semiconductor



LFT155/LFT156, LFT355/LFT356 Low Offset Monolithic JFET Input Operational Amplifiers

General Description

These monolithic JFET input operational amplifiers have guaranteed low offset voltage and offset voltage drift along with high common-mode rejection which allows their use in applications requiring precision to 0.01%. In addition, they have the same low bias and offset currents, high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and low 1/f corner as do the normal LF155/LF156 BI-FET operational amplifier families.

Advantages

- Ultra-low offset—12-bit accuracy without adjust
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Output amplifiers in 10 and 12-bit current mode D/A converters
- Data acquisition front-end amplifiers: (DC coupled difference amplifier, buffer)
- Output buffer in S/H circuits
- Low pass filters with DC gain
- Amplifier for auto-zeroing loops
- Long time integrators
- Precise analog computer amplifiers and integrators
- Replace op amps in existing systems requiring:
  - Offset voltage adjustment
  - Drift selection
  - Fast settling
  - Low noise
  - Low bias current

Features

LFT155/LFT156

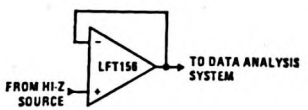
Low input offset voltage	0.5 mV max
Low input offset voltage temperature drift	5 $\mu V/^{\circ}C$ max
Low input bias current	50 pA max
Low input offset current	10 pA max
High common-mode rejection ratio	95 dB min
High input impedance	$10^{12}\Omega$
Low input noise current	0.01 $pA/\sqrt{Hz}$
Large DC voltage gain	106 dB

LFT156/LFT356

Fast slew rate	10 $V/\mu s$ min
Wide gain bandwidth	4 MHz min
Extremely fast settling	1.5 μs to 0.01%
Low input noise voltage	12 $nV/\sqrt{Hz}$

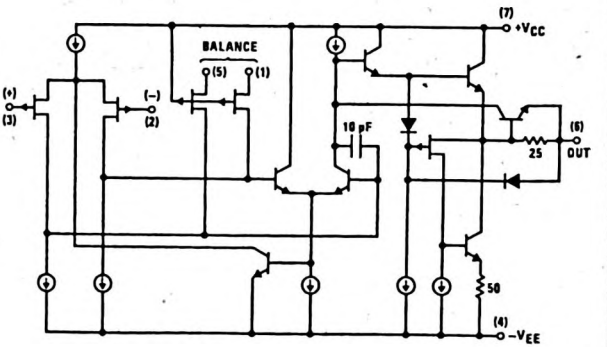
Typical Applications

12-Bit Accurate Buffer



Greater than 12-bit accuracy without adjustment

Simplified Schematic



Absolute Maximum Ratings

	LFT155/LFT156	LFT355/LFT356
Supply Voltage	±22V	±18V
Power Dissipation (P_d at 25°C)	670 mW	570 mW
and Thermal Resistance (θ_{jA}) (Note 1)	150°C/W	150°C/W
T_jMAX	150°C	115°C
Differential Input Voltage	±40V	±30V
Input Voltage Range (Note 2)	±20V	±16V
Output Short-Circuit Duration	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LFT155/LFT156 LFT355/LFT356			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$			0.5	mV
		Over Temperature			1.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10	pA
		$T_j \leq T_{HIGH}$			1	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5)		30	50	pA
		$T_j \leq T_{HIGH}$			5	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k$				
		Over Temperature	25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio		95			dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		dB

$T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	LFT155, LFT355			LFT156, LFT356			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current		2	4		5	7	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LFT155, LFT355			LFT156, LFT356			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	$A_V = 1$	3	5		10	12		V/µs
GBW	Gain Bandwidth Product			2.5		4	4.5		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$							
		f = 100 Hz		25			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		20			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3		pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LFT155/LFT156	LFT355/LFT356
Supply Voltage, V_S	$\pm 15V \leq V_S \leq \pm 20V$	$\pm 15V \leq V_S \leq \pm 18V$
T_A	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
T_{HIGH}	+125°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_j = T_A + \Theta_{JA} P_d$ where Θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

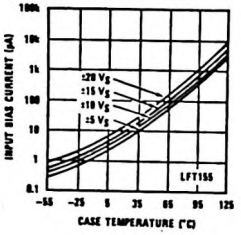
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

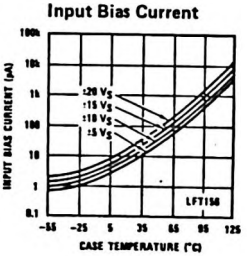
Typical DC Performance Characteristics

Curves are for LFT155 and LFT156 unless otherwise specified.

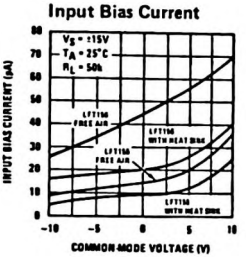
Input Bias Current



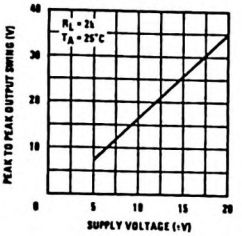
Input Bias Current



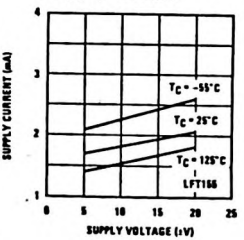
Input Bias Current



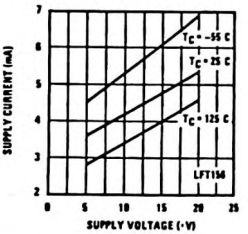
Voltage Swing



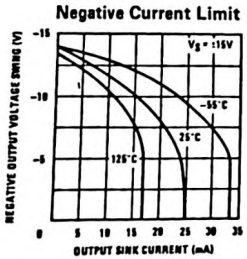
Supply Current



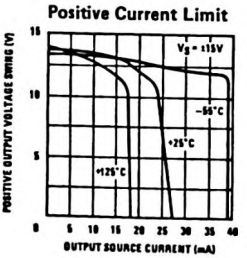
Supply Current



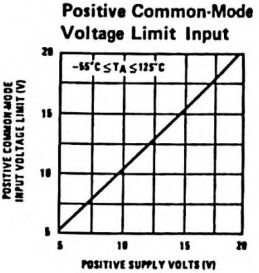
Negative Current Limit



Positive Current Limit

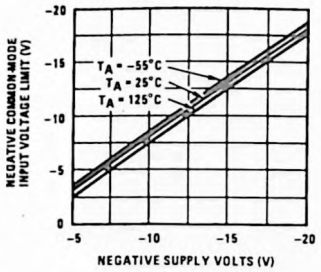


Positive Common-Mode Voltage Limit Input

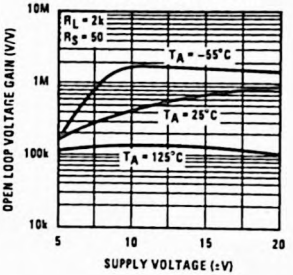


Typical DC Performance Characteristics (Continued)

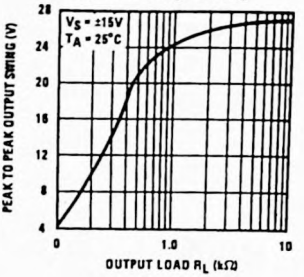
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

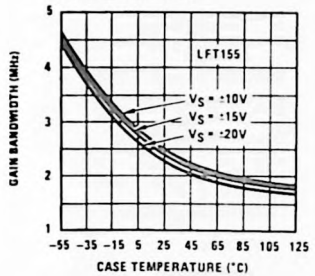


Output Voltage Swing

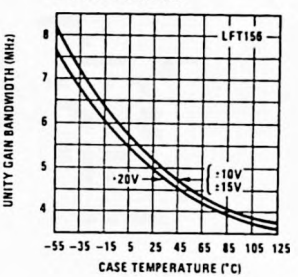


Typical AC Performance Characteristics

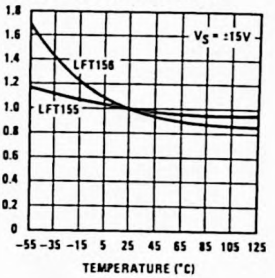
Gain Bandwidth



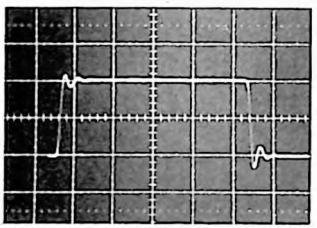
Gain Bandwidth



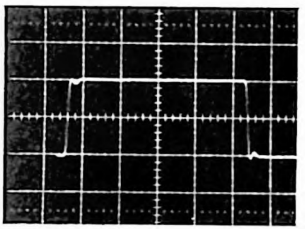
Normalized Slew Rate



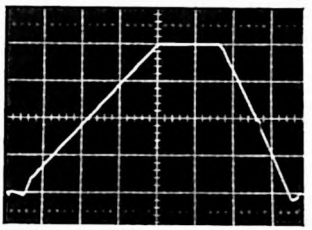
LFT155 Small Signal Pulse Response, A_V = 1



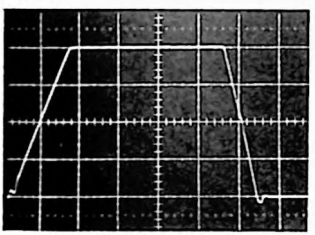
LFT156 Small Signal Pulse Response, A_V = 1



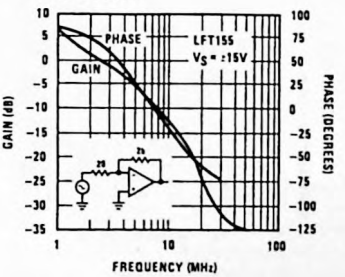
LFT155 Large Signal Pulse Response, A_V = 1



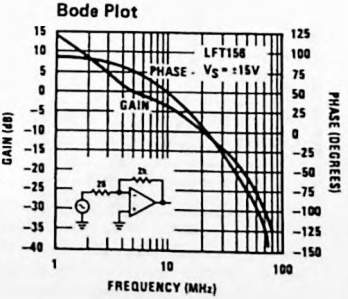
LFT156 Large Signal Pulse Response, A_V = 1



Bode Plot

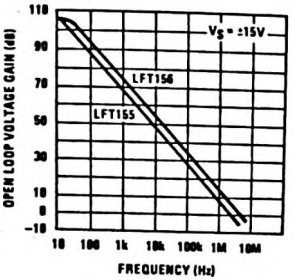


Bode Plot

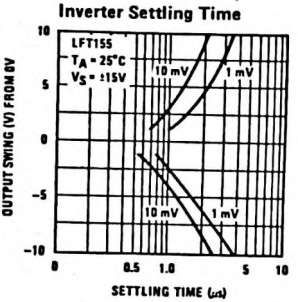


Typical AC Performance Characteristics (Continued)

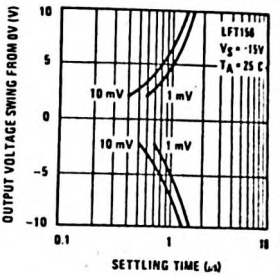
Open Loop Frequency Response



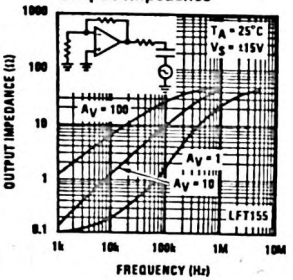
Inverter Settling Time



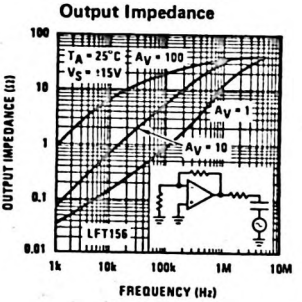
Inverter Settling Time



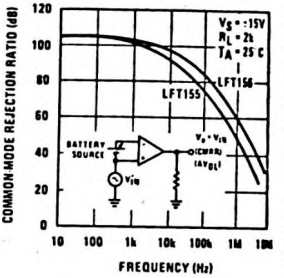
Output Impedance



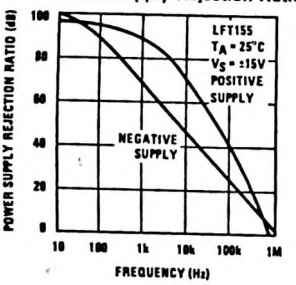
Output Impedance



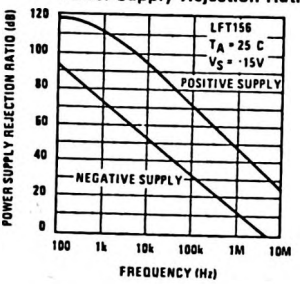
Common-Mode Rejection Ratio



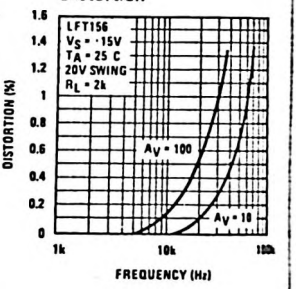
Power Supply Rejection Ratio



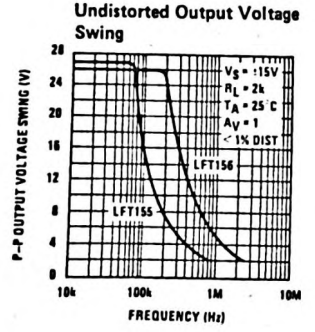
Power Supply Rejection Ratio



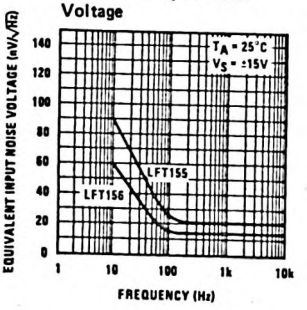
Distortion



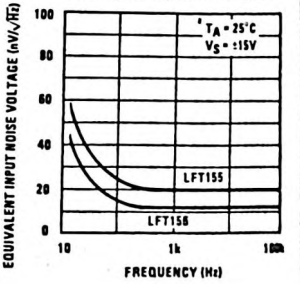
Undistorted Output Voltage Swing



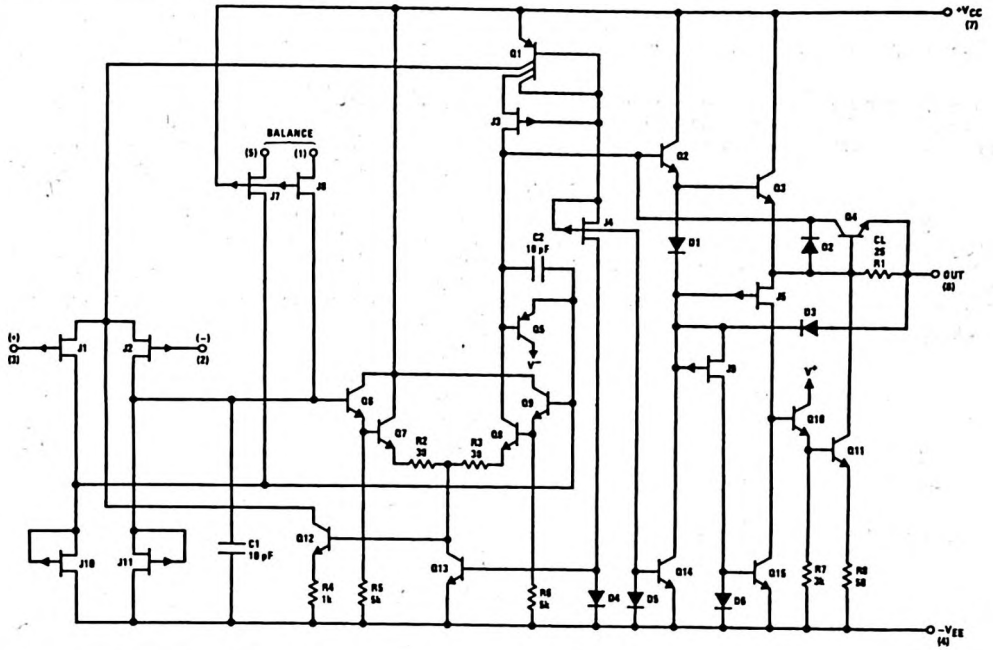
Equivalent Input Noise Voltage



Equivalent Input Noise Voltage (Expanded Scale)

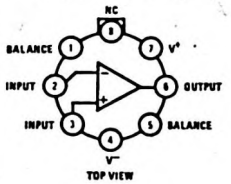


Detailed Schematic



Connection Diagram

Metal Can Package



Note. Pin 4 connected to case.

Order Number LFT155H, LFT156H, LFT355H or LFT356H
See NS Package H08B

Application Hints

The LFT155/6 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Application Hints (Continued)

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

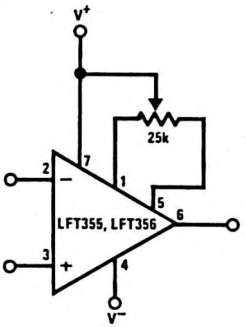
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

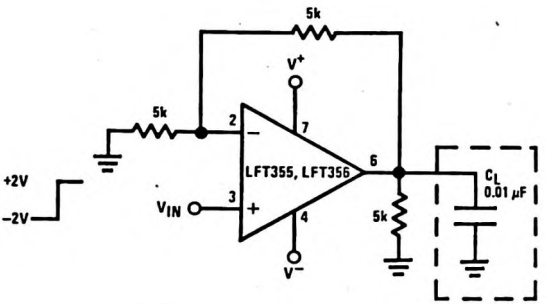
Typical Applications (Continued)

V_{OS} Adjustment (Usually Not Needed)



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



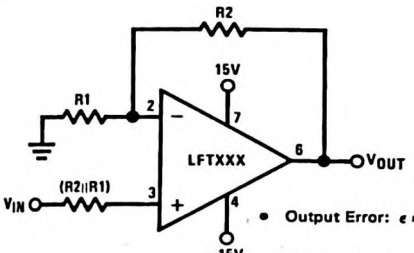
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot $\leq 20\%$

Settling time (t_s) $\cong 5\ \mu s$

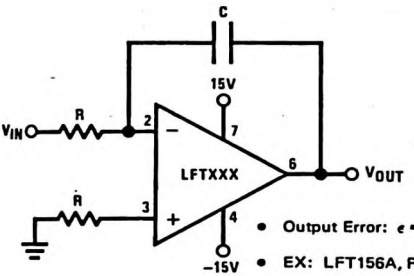
Typical Applications (Continued)

Errors Created by V_{OS}, I_B, I_{OS}, CMRR, A_{OL} in Some Basic Op Amp Circuits and How the LFTXXX Series Minimizes Them



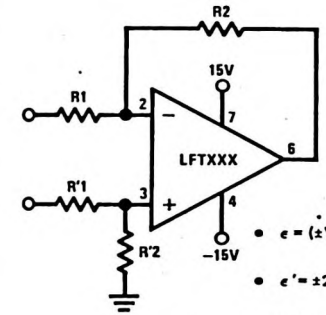
- Output Error: $\epsilon \propto (\pm V_{OS} \times A_V \pm R2\ I_{OS}) + \left[\left(1+\frac{A_V}{A_{OL}}\right)^{-1}\left(1+\frac{1}{CMRR}\right)-1\right]\frac{(V)}{V_{OUT}}$
- EX: LFT356A as unity gain follower $\left\{\begin{array}{l} A_V = 1,\ 0°C \le T_A \le 70°C \\ R2 = 10k \end{array}\right. \longrightarrow A_V = \frac{R2+R1}{R1}$

$$1.01\ mV - \frac{38\mu V}{V_{OUT}} \ge \epsilon \ge -1.01\ mV - \frac{58\mu V}{V_{OUT}}$$



- Output Error: $\epsilon = \pm V_{OS} - R\ (I_B \pm I_{OS}) \pm \frac{t}{RC}\ (V_{OS} \pm R I_{OS})$ t = Integration Time
- EX: LFT156A, R = 100k, C = 0.1μF

$$1.4\ mV + \frac{1.1\ mV}{10\ ms} > \epsilon > -1.6\ mV - \frac{1.1\ mV}{10\ ms}$$

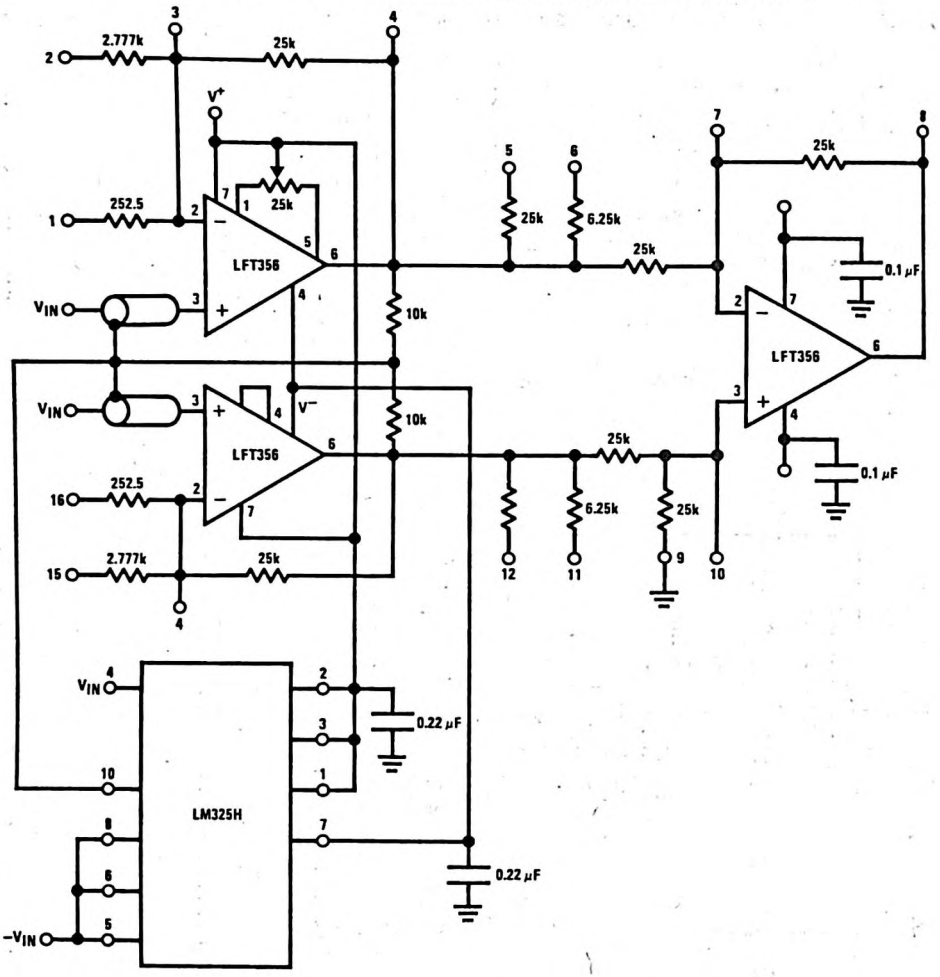


- $\epsilon = (\pm V_{OS}\ (1 + A_V) \pm R2\ I_{OS})\left(1+\frac{A_V}{A_{OL}}\right)^{-1}$:Output Error due to V_{OS}, I_{OS}, A_{OL}
- $\epsilon' = \pm 2\delta$ (%) :Error on A_V due to resistor tolerance
- CMR (Circuit) = $20 \log \left(1+\frac{a+1}{A_{OL}}\right)\left[\frac{a+1}{b+1}\left(1 \pm \frac{1}{CMRR}\right) - a\right]^{-1}$ $\quad a = \frac{R2 \pm \delta}{R1 \pm \delta} = \frac{A_V\ (100 \pm \delta)}{(100 \pm \delta)}$
- CMR (Circuit) $|_{MIN}$ occurs for a $|_{MAX}$, b $|_{MAX}$ $\quad b = \frac{R'1 \pm \delta}{R'2 \pm \delta} = \frac{(100 \pm \delta)}{A_V\ (100 \pm \delta)}$
- EX: LFT356A, A_V = 10, R2 = 10k, 0°C ≤ T_A ≤ 70°C, δ = 0.01%

  11.01 mV ≥ ε ≥ −11.01 mV, ε' = ±0.02%, CMR (Circuit) $|_{MIN}$ = 85.3 dB

Typical Applications (Continued)

High CMRR, Low Drift Instrumentation Amplifier with Floating Input Stage



- Input amplifier fully floating. Develop ± input voltage for the floating regulator, LM325, from a second center tapped secondary winding.
- All resistors, except the two 10k ones, are from National resistor array RA201.
- CMRR (instrum. amplifier) ≃ CMRR (difference amplifier) x A_{V_1}; A_{V_1} = gain of the input stage.

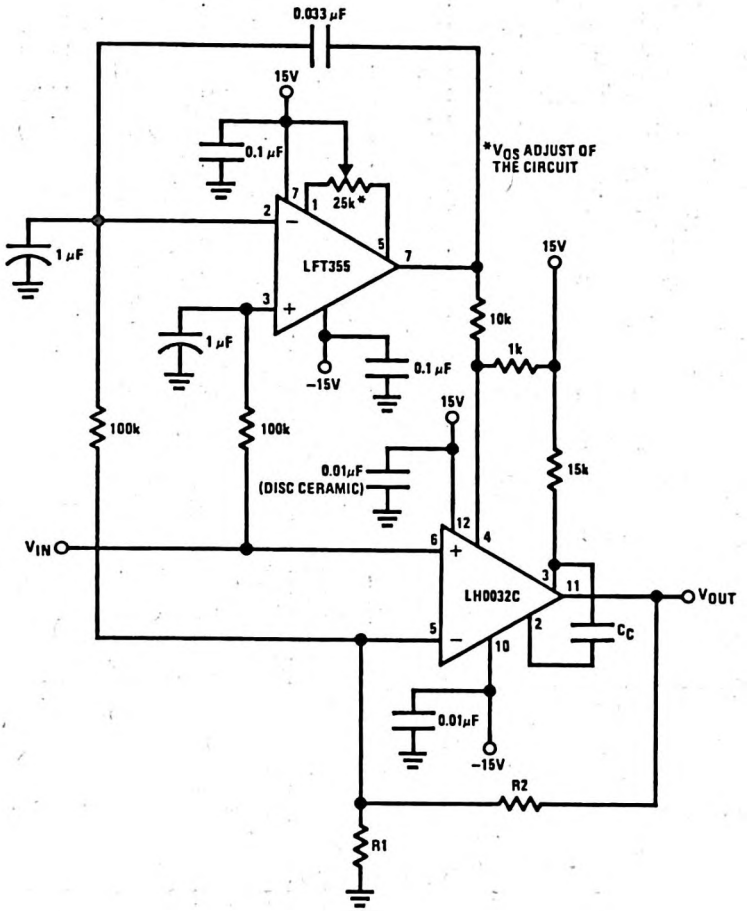
GAIN SET-UP

Input Stage Gain	Output Stage Gain	Overall Gain	Jumper Pins on RA201	Expected Minimum CMRR (Overall Circuit)
1	1	1		83.4
1	2	2	5 to 7, 12 to 10	82
1	5	5	6 to 7, 11 to 10	86
10	1	10	2 to 15	103.4
10	2	20	2 to 15, 5 to 7, 12 to 10	102
10	5	50	2 to 15, 6 to 7, 11 to 10	106
100	1	100	1 to 16	123.4
100	2	200	1 to 16, 5 to 7, 12 to 10	122
100	5	500	1 to 16, 6 to 7, 11 to 10	126
199	5	995	1 to 14, 6 to 7, 11 to 10	131 dB

- Gain error: ±0.01% on the output stage, ±0.01% on the input stage for a gain of 10, and ±1% for a gain of 199.

*Typical Applications (Continued)

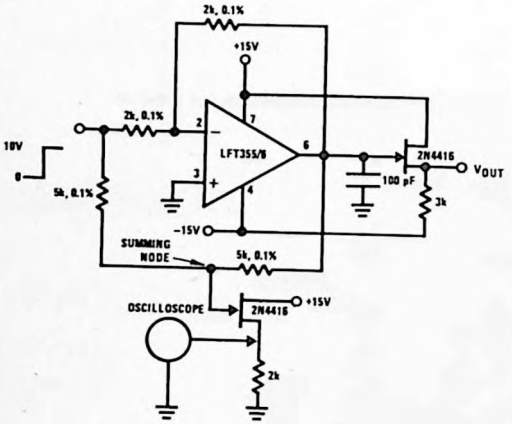
Using the LFTXXX Series to Auto-Zero Ultra Fast Hybrid Op Amps (General Scheme)



- V_{OS}, $\frac{\Delta V_{OS}}{\Delta T}$ of the circuit: The V_{OS} and drift of the LFT355.
- Speed of the circuit: The GBW product and t_s of the LH0032.
- The circuit can also be used for inverters and integrators applications.
- Due to the ultra high speed of the LH0032C proper layout is recommended.
- Compensation capacitor C_c is not needed for gains above 50. For more details see LH0032 data sheet.
- By adjusting of the V_{OS} of the LFT we adjust the V_{OS} of the whole circuit.

Typical Applications (Continued)

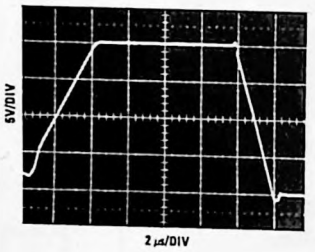
Settling Time Test Circuit



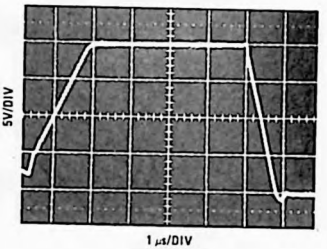
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

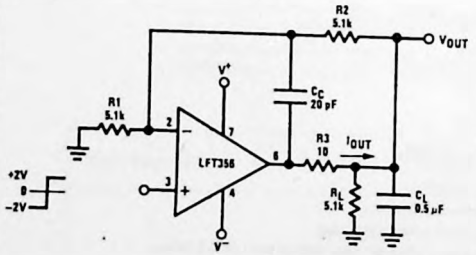
LFT355



LFT356



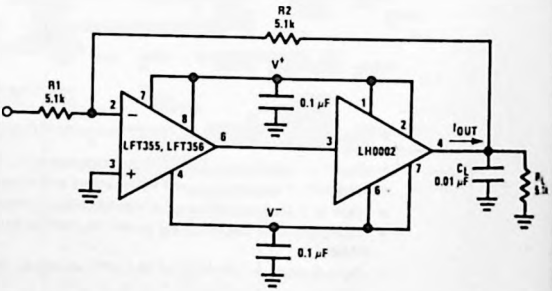
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \text{ V/μs} = 0.04 \text{ V/μs (with } C_L \text{ shown)}$$

Boosting the LFT156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/μs (with C_L shown)
- No additional phase shift added by the current amplifier

National Semiconductor

LH0036/LH0036C Instrumentation Amplifier

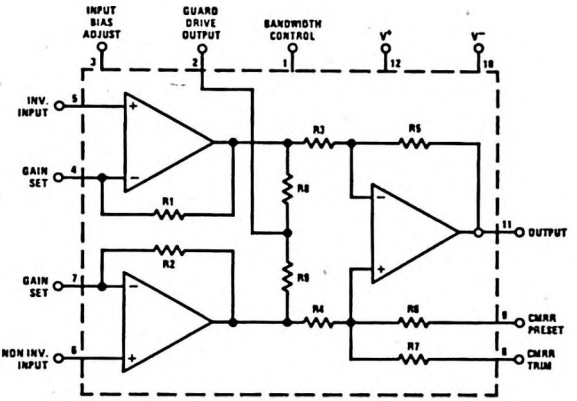
general description

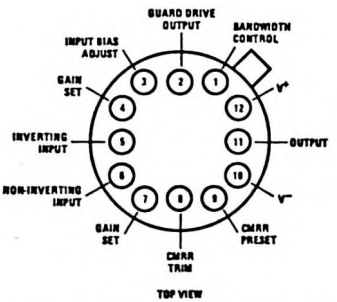
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 90μW
- Wide supply range — ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

equivalent circuit and connection diagrams





Order Number LH0036H or LH0036CH
See NS Package H12B

absolute maximum ratings

Supply Voltage	±18V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0036	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0036C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature, Soldering 10 seconds	300°C
Power Dissipation (Note 3)	1.5W		

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0036			LH0036C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		40	100		50	125	nA
				150			200	nA
Input Offset Current (I_{OS})	T_A = 25°C		10	40		20	50	nA
				80			100	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 10kΩ		350			350		kHz
	A_V = 10, R_L = 10kΩ		35			35		kHz
	A_V = 100, R_L = 10kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 10kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 10k, A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±10	±12		±10	±12		V
	Common Mode	±10	±12		±10	±12		V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1.0		±1.0	±3.0	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5.0	mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10	0.50	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	0.50	mV/V
	A_V = 100 ΔR_S = 1.0k		50	100		50	100	µV/V
Output Voltage	V_S = ±15V, R_L = 10kΩ,	±10	±13.5		±10	±13.5		V
	V_S = ±1.5V, R_L = 100kΩ	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	µA
Equivalent Input Noise Voltage			20			20		µV/p-p
Slew Rate	ΔV_{IN} = ±10V, R_L = 10kΩ, A_V = 1.0		0.3			0.3		V/µs
Settling Time	To ±10 mV, R_L = 10kΩ, ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

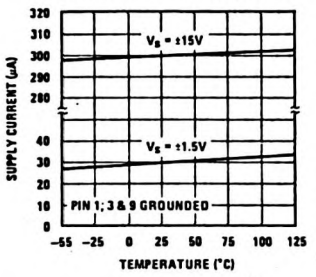
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for T_A = 25°C.

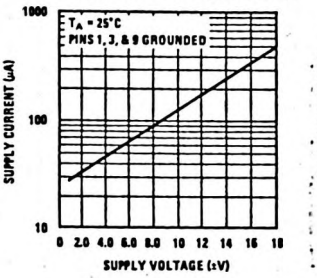
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

typical performance characteristics

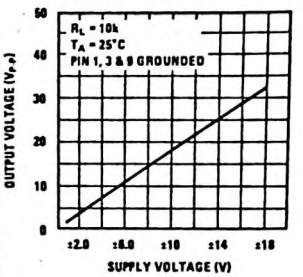
Supply Current vs Temperature



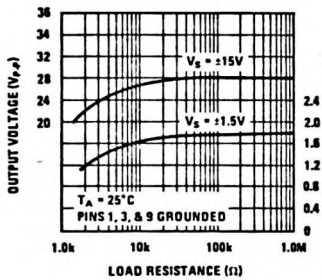
Supply Current vs Supply Voltage



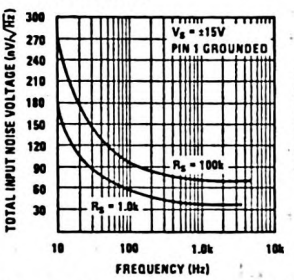
Output Voltage Swing vs Supply Voltage



Peak to Peak Output Voltage Swing vs R_L

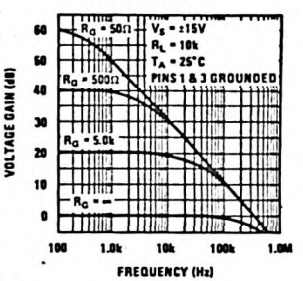


Total Input Noise Voltage* vs Frequency

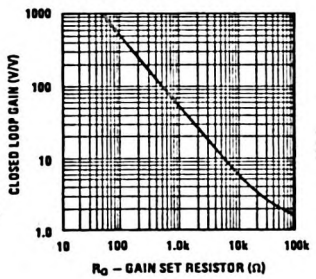


*Noise voltage includes contribution from source resistance

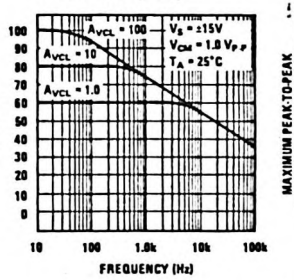
Closed Loop Voltage Gain vs Frequency



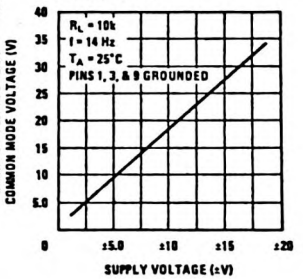
Closed Loop Voltage Gain



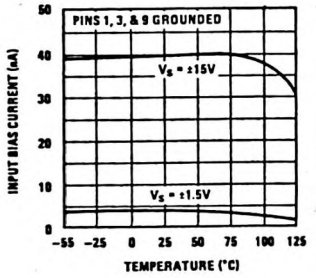
CMRR vs Frequency



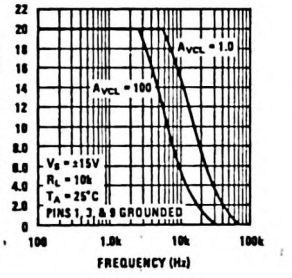
Common Mode Voltage vs Supply Voltage



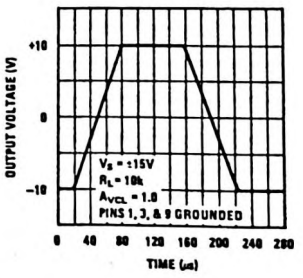
Input Bias Current



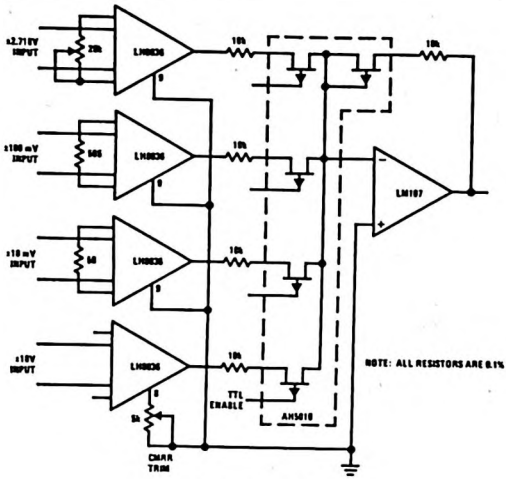
Output Voltage Swing vs Frequency



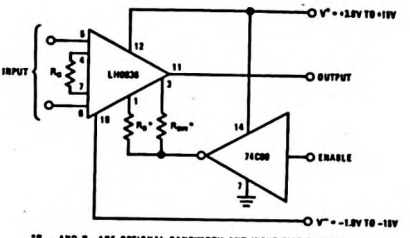
Large Signal Pulse Response



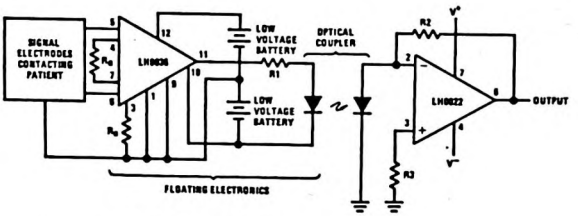
typical applications



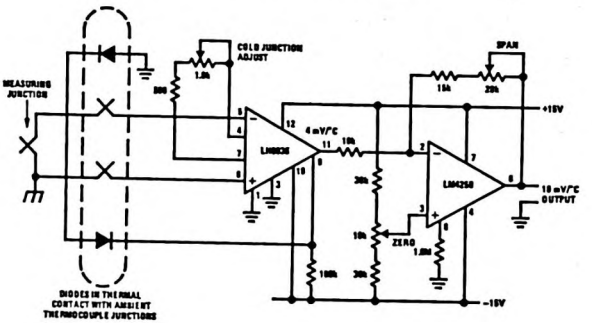
Pre MUX Signal Conditioning



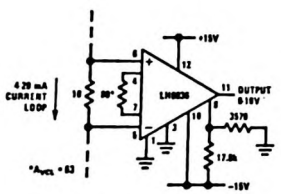
Instrumentation Amplifier with Logic Controlled Shut-Down



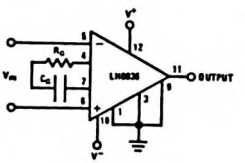
Isolation Amplifier for Medical Telemetry

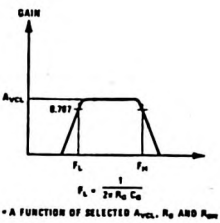


Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface





High Pass Filter

applications information

THEORY OF OPERATION

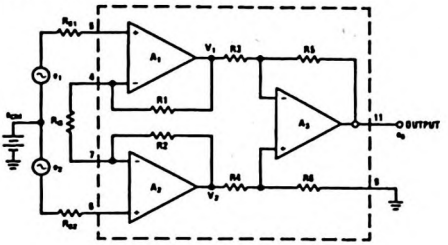


FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.
Hence:

$$V_1 = \frac{R1 + R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μs and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. Figure 2 shows typical small signal bandwidth versus R_{BW}.

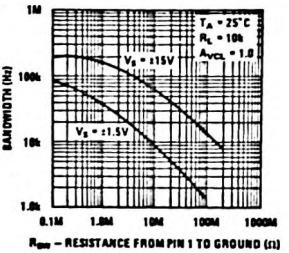


FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. Figure 3 is plot of slew rate versus R_{BW}. .

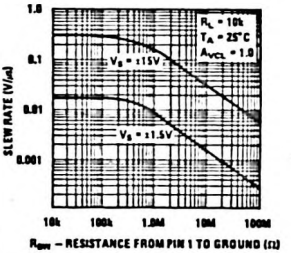


FIGURE 3. Output Slew Rate vs R_{BW}

CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in Figure 4.

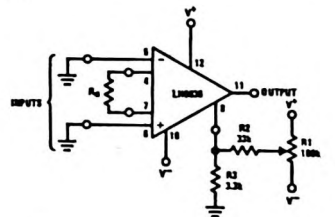


FIGURE 4. V_{OS} Adjustment Circuit

Pin 8 is also used to improve the common mode rejection ratio as shown in Figure 5. Null is

applications information (con't)

achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.

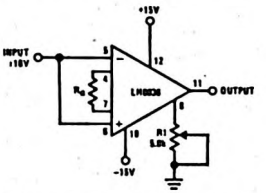


FIGURE 5. CMRR Adjustment Circuit

The circuits of Figure 4 and 5 may be combined as shown in Figure 6 to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

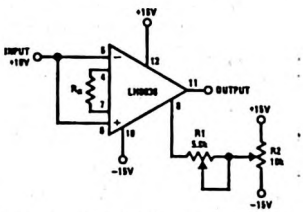
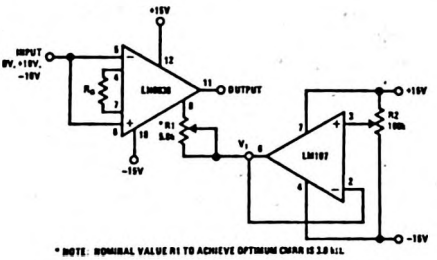


FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in Figure 7. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



* NOTE: NOMINAL VALUE R1 TO ACHIEVE OPTIMUM CMRR IS 2.0 kΩ.

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of Figure 8.

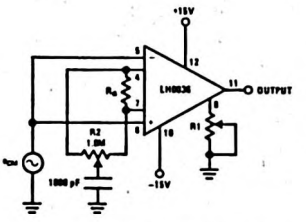


FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\ R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0\,5 - (4 \times 10^8)\ (I_{BIAS})}{800\ I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External Resistor connected between pin 3 and ground (Ohms)

V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.

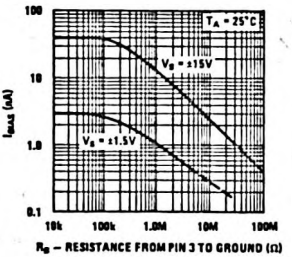


FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\ R_B}$$

applications information (con't)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\, I_{BIAS}} \quad (8)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External resistor connected between pin 3 and V^- (Ohms)

V^+ = Positive Supply Voltage (Volts)

V^- = Negative Supply Voltage (Volts)

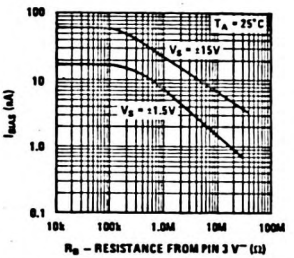


FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. Figure 11 is a plot of bandwidth versus R_B.

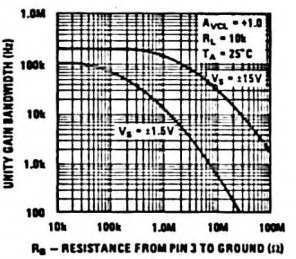


FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in Figure 12.

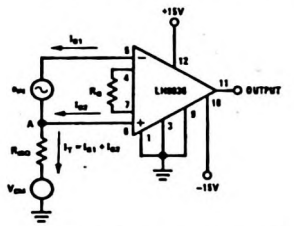


FIGURE 12. Bias Current Return Path

In a typical application, V_S = ±15V, $I_{B1} \cong I_{B2} \cong$ 40 nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

Where:

V_{CMR} = Common Mode Range (10V for the LH0036)

V_{CM} = Common Mode Voltage

$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in Figure 13.

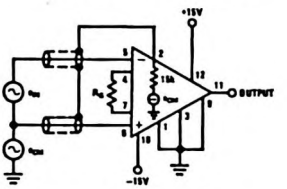


FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in Figure 14.

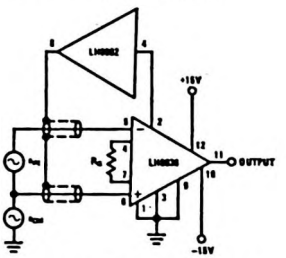


FIGURE 14. Guard Pin With Buffer

National Semiconductor

LH0037/LH0037C Low Cost Instrumentation Amplifier

general description

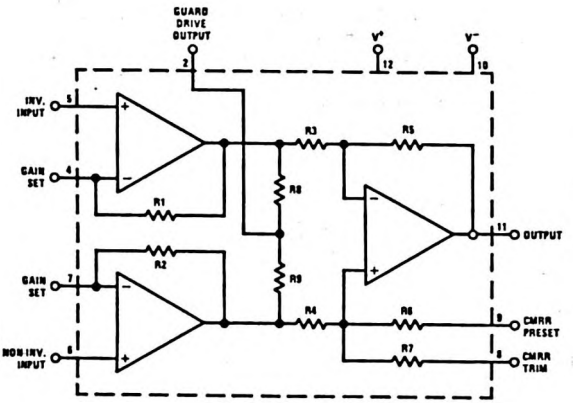
The LH0037/LH0037C is a true instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common-mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±5V and ±22V.

The LH0037 is specified for operation over the −55°C to +125°C temperature range and the LH0037C is specified for operation over the −25°C to +85°C temperature range.

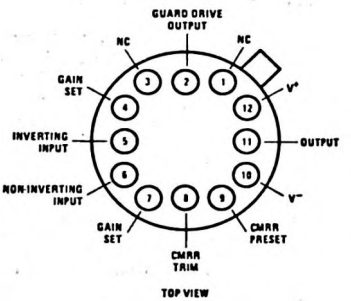
features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 250 mW
- Wide supply range — ±5V to ±22V
- Guard drive output

equivalent circuit and connection diagrams

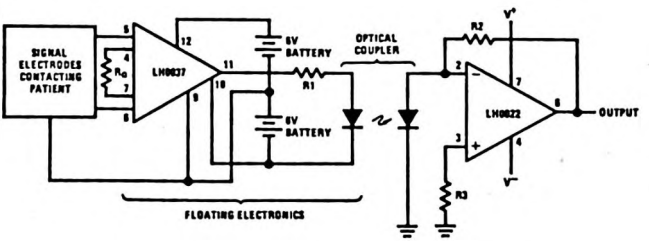


Metal Can Package



Order Number LH0037H or LH0037CH
See NS Package H12B

typical applications



Isolation Amplifier for Medical Telemetry

absolute maximum ratings

Supply Voltage	±22V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0037	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0037C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (Note 3)	1.5W		

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0037			LH0037C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0 kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0 kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0 kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0 kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0 kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		200	500		200	500	nA
				1.5			0.8	µA
Input Offset Current (I_{OS})	T_A = 25°C			200			250	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 2 kΩ		350			350		kHz
	A_V = 10, R_L = 2 kΩ		35			35		kHz
	A_V = 100, R_L = 2 kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 2 kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 2 kΩ A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±12			±12			V
	Common Mode	±12			±12			V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1		±1.0	±3	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5	mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10	0.25	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	1.0	mV/V
	A_V = 100 ΔR_S = 1.0k		25	100		25	100	µV/V
Output Voltage	R_L = 2 kΩ	10	13		10	13		V
Output Resistance			0.5			0.5		Ω
Supply Current			4.5	8.4		4.5	8.4	mA
Slew Rate	ΔV_{IN} = ±10V, R_L = 2 kΩ, A_V = 1.0		0.5			0.5		V/µs
Settling Time	To ±10 mV, R_L = 2 kΩ ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

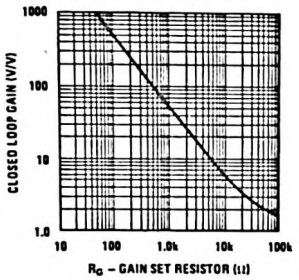
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, pin 9 grounded, −25°C to +85°C for the LH0037C and −55°C to +125°C for the LH0037.

Note 2: All typical values are for T_A = 25°C.

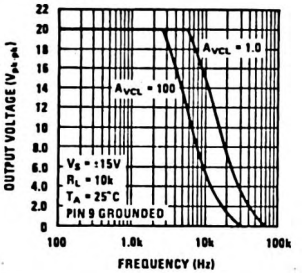
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 160°C/W, above 25°C.

typical performance characteristics

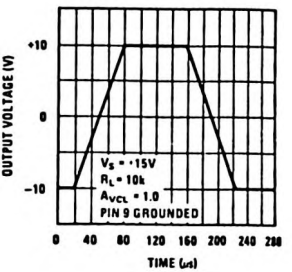
Closed Loop Voltage Gain



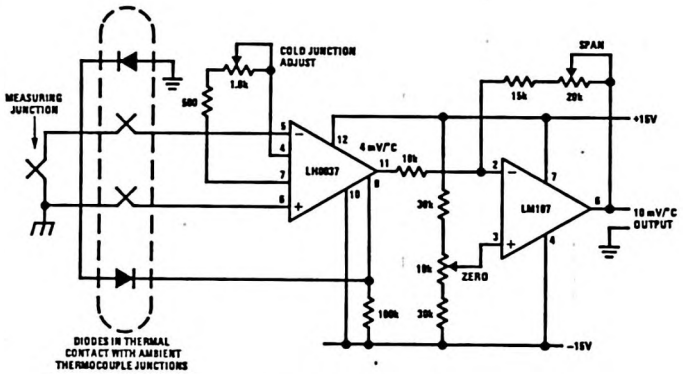
Output Voltage Swing vs Frequency



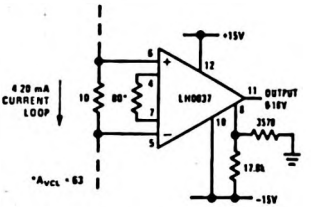
Large Signal Pulse Response



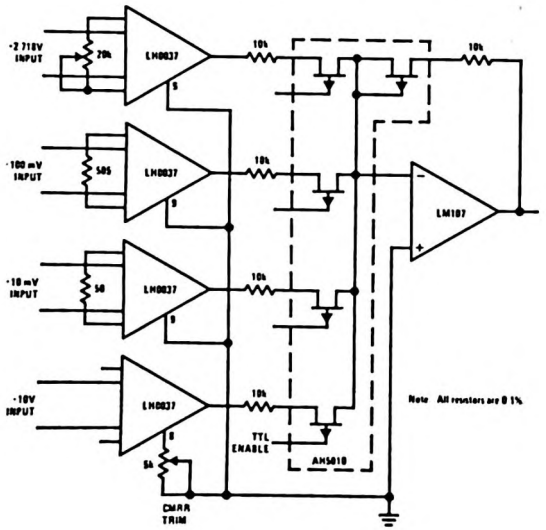
typical applications (con't)



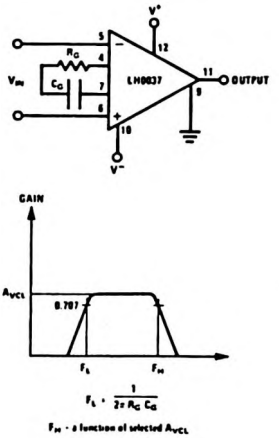
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



Pre MUX Signal Conditioning



High Pass Filter

National Semiconductor

LH0044 Series Precision Low Noise Operational Amplifiers

general description

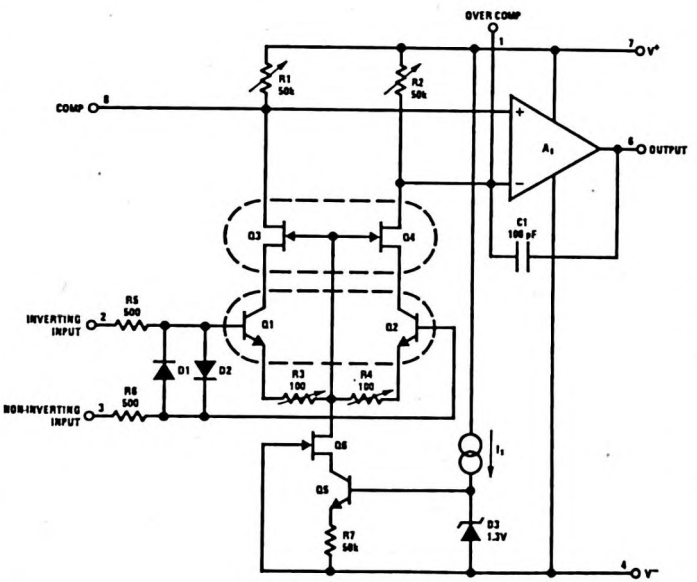
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 and LH0044A are guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

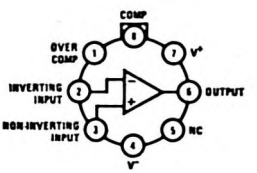
features

- Low input offset voltage 25μV max
- Excellent long-term stability ±1μV/month max
- Low offset drift 0.5μV/°C max
- Very low noise 0.7μVp-p max 0.1 Hz to 10 Hz
- High CMRR and PSRR 120 dB min
- High open loop gain 120 dB min
- Wide common-mode range ±13V min
- Wide supply voltage range ±2V to ±20V

equivalent circuit and connection diagram



Metal Can Package



TOP VIEW

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01 μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

TO-5 Metal Can Package (H)
Order Number LH0044AH or LH0044H (−55°C to +125°C)
Order Number LH0044ACH, LH0044BH or LH0044CH (−25°C to +85°C)
See NS Package H08B

absolute maximum ratings

Supply Voltage	±20V
Power Dissipation	600 mW
Differential Input Voltage (Note 4)	±15V
Input Voltage (Note 5)	±15V
Output Short-Circuit Duration	Continuous

Operating Temperature Range	
LH0044, LH0044A	−55°C to +125°C
LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0044A/LH0044AC			LH0044/LH0044B/LH0044C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$		8	25		12	50	µV
	LH0044C Only						100	µV
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$			50			150	µV
	LH0044A and LH0044B Only			75			75	µV
Average Input Offset Voltage Drift	$T_{MIN} \leq T_A \leq T_{MAX}$		0.1	0.5		0.2	1.3	µV/°C
	LH0044B Only						0.5	µV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	µV/month
Input Noise Voltage (Note 3)	BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$		0.35	0.7		0.35	0.8	µVp-p
	R_S = 10 kΩ Imbalance		0.50	0.9		0.50	1.0	µVp-p
Thermal Feedback Coefficient			0.005			0.005		µV/mW
Open Loop Voltage Gain	R_L = 10 kΩ	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \leq V_S \leq \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	R_L = 10 kΩ	±13	±13.7		±12	±13.5		V
Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		1.0	2.5		1.5	5.0	nA
	$T_{MIN} \leq T_A < 25°C$			5.0			10.0	nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	$25°C \leq T_A \leq T_{MAX}$		8.5	15		10	30	nA
	$T_{MIN} \leq T_A < 25°C$			50			100	nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common-Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	$I_L = 0$		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

ac electrical characteristics $T_A = 25°C$, $V_S = \pm 15V$

PARAMETER	CONDITIONS	TYP	UNITS
Input Noise Voltage	R_S = 1 kΩ, f_O = 10 Hz	11	$nV/\sqrt{Hz}$
	R_S = 1 kΩ, f_O = 1 kHz	9	$nV/\sqrt{Hz}$
Slew Rate	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	0.06	V/µs
Large Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100$, $V_{IN} = -100$ mV, ΔV_{IN} = 200 mV	5	µs
Small Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ	400	kHz
Small Signal Rise Time	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV	2.5	µs
Overshoot	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV, C_L = 100 pF	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{MIN} to T_{MAX} unless otherwise specified. T_{MIN} is −55°C and T_{MAX} is +125°C for the LH0044A and LH0044. T_{MIN} is −25°C and T_{MAX} is +85°C for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

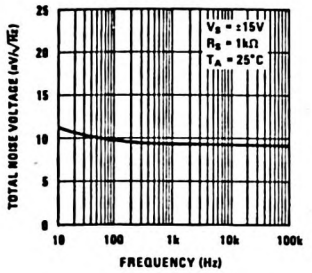
Note 3: Noise is 100% tested on the LH0044A, LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

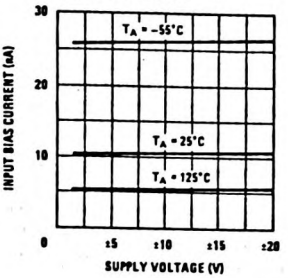
Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ttypical performance characteristics

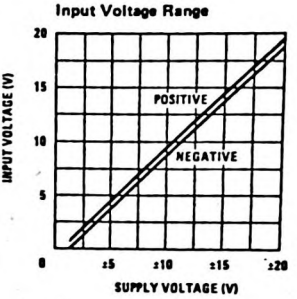
Total Input Noise Voltage vs Frequency



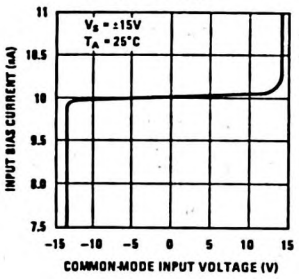
Input Bias Current



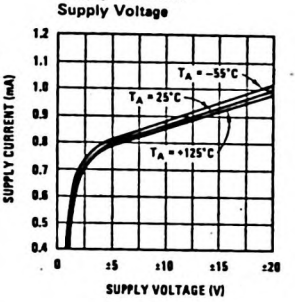
Input Voltage Range



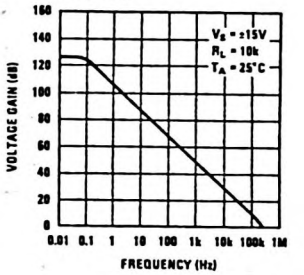
Input Bias Current vs Common-Mode Input Voltage



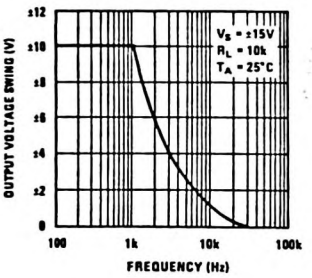
Supply Current vs Supply Voltage



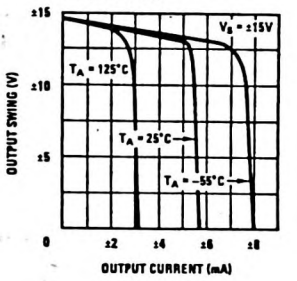
Open Loop Frequency Response



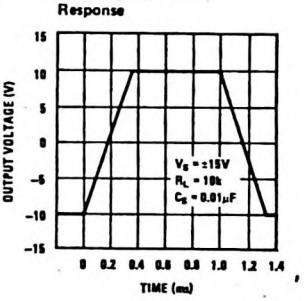
Large Signal Voltage Response



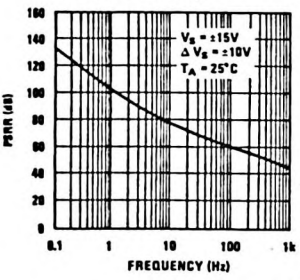
Output Swing



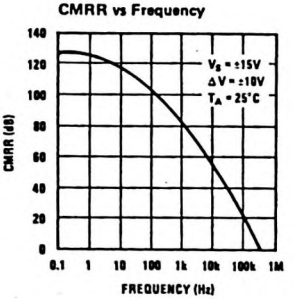
Large Signal Pulse Response



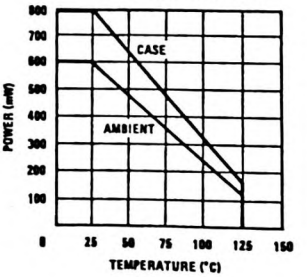
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



9

applications information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

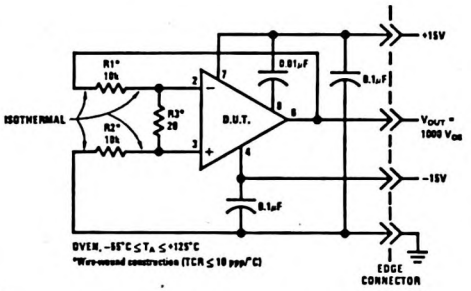


FIGURE 1. LH0044 Temperature Test Circuit

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ pF + C_{ext}\ pF}\ (Hz)$$

COMPENSATION

For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2*. Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2*.

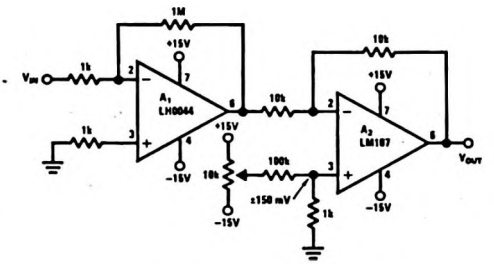
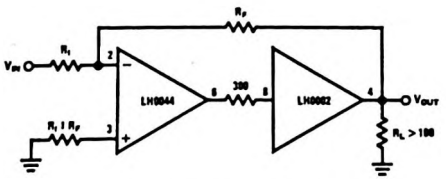
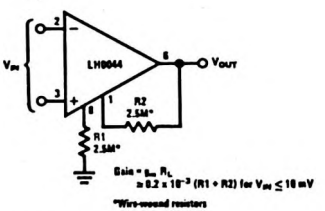


FIGURE 2. LH0044 Null Technique

typical applications

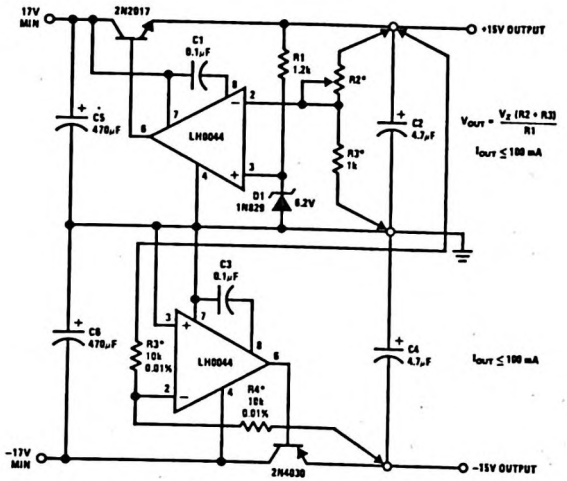


Buffered Output for Heavy Loads

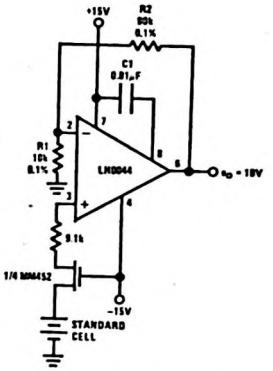


X1000 Instrumentation Amp

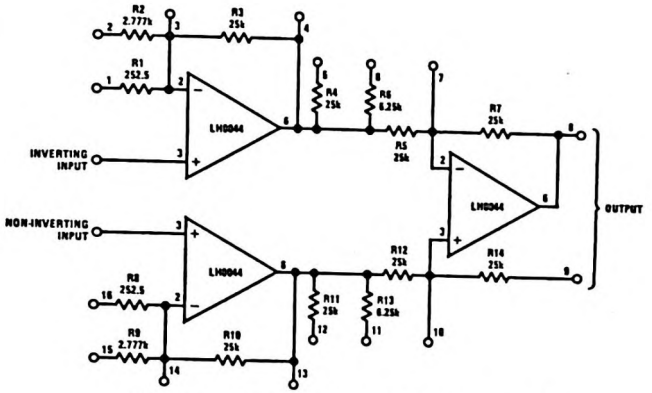
typical applications (con't)



Precision Dual Tracking Regulator



10V Reference Supply

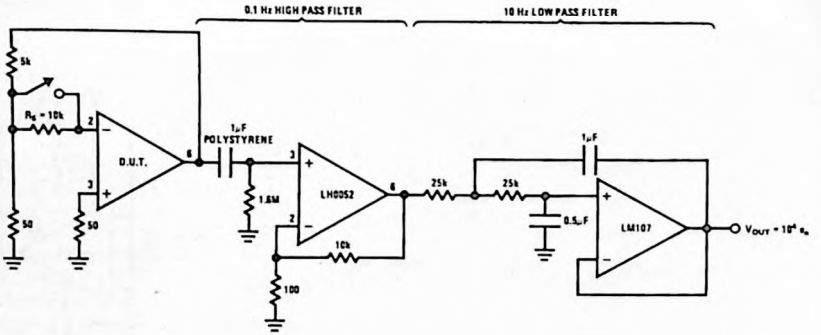


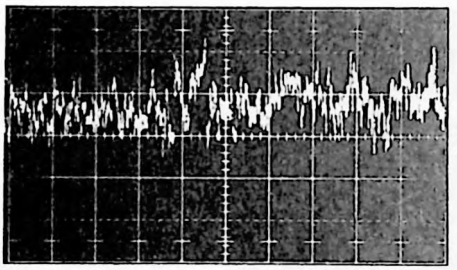
(All Resistors are Part of National's RA201 Resistor Array).

OVERALL GAIN	INPUT STAGE GAIN	OUTPUT STAGE GAIN	JUMPER PINS ON RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

noise test circuit





National Semiconductor

LM146/LM246/LM346
Programmable Quad Operational Amplifiers

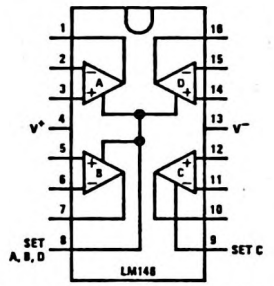
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

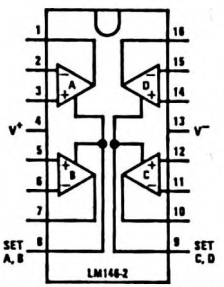
- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagrams (Dual-In-Line Packages, Top Views)



Order Number LM146J, LM246J or LM346J
See NS Package J16A

Order Number LM246N or LM346N
See NS Package N16A



Order Number LM146-2J, LM246-2J, LM346-2J
See NS Package J16A

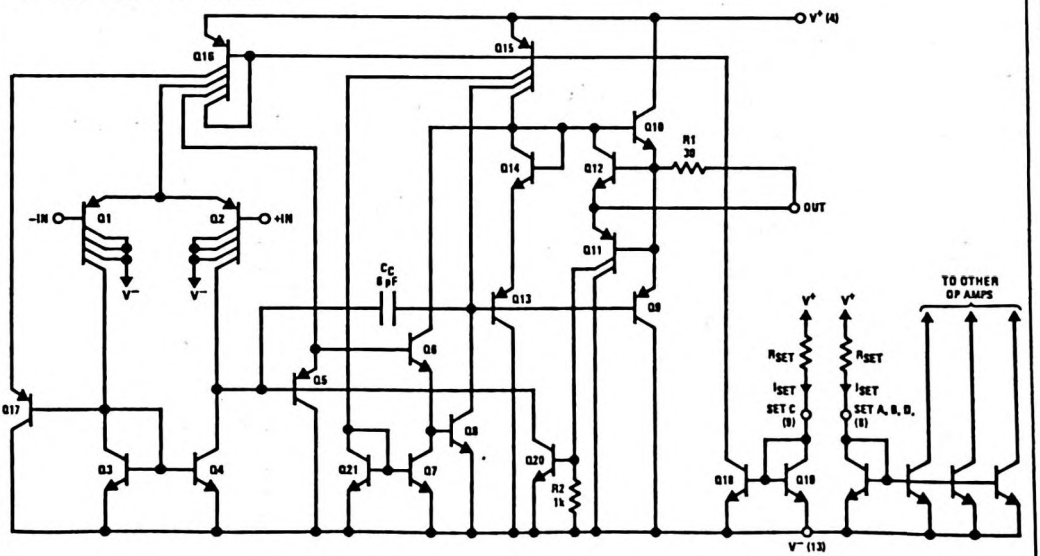
Order Number LM346-2N
See NS Package N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≈ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



Absolute Maximum Ratings (Note 1)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (D) (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W	90°C/W
Molded DIP (N) P_d			500 mW
θ_{jA}			140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	100	1000		50	1000		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short-Circuit Current	T_A = 25°C	5	20	30	5	20	30	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		nV/√Hz
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\ \Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

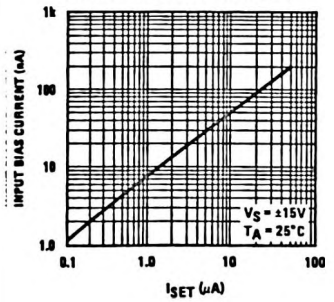
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

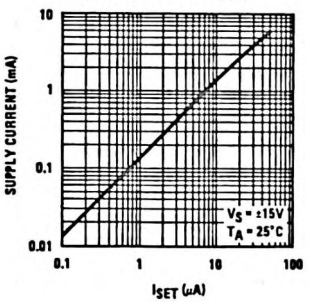
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

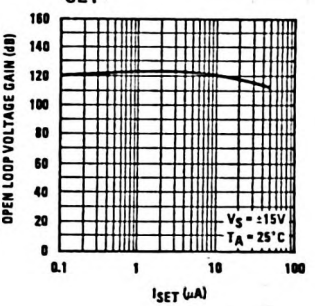
Input Bias Current vs I_{SET}



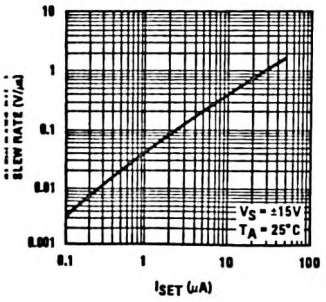
Supply Current vs I_{SET}



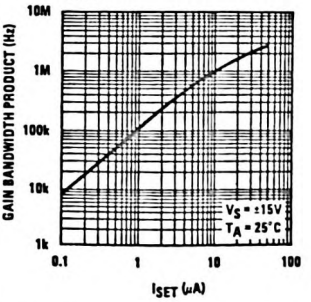
Open Loop Voltage Gain vs I_{SET}



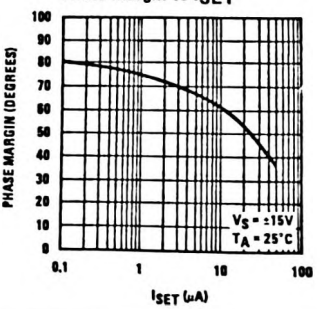
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

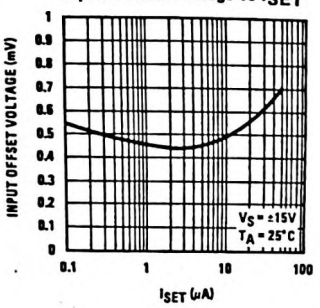


Phase Margin vs I_{SET}

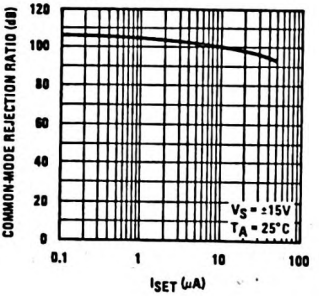


Typical Performance Characteristics (Continued)

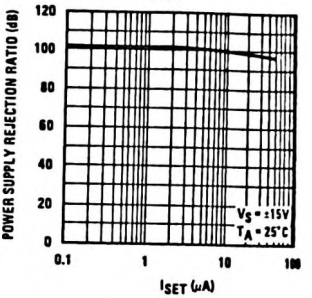
Input Offset Voltage vs I_{SET}



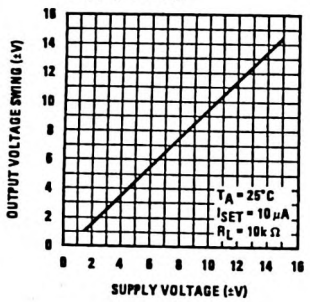
Common-Mode Rejection Ratio vs I_{SET}



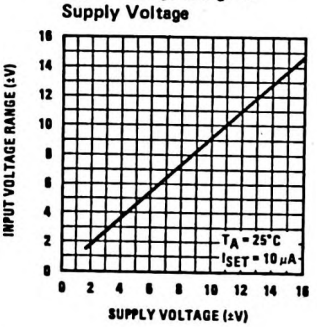
Power Supply Rejection Ratio vs I_{SET}



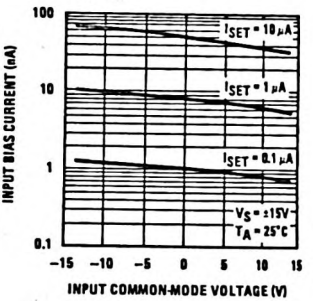
Output Voltage Swing vs Supply Voltage



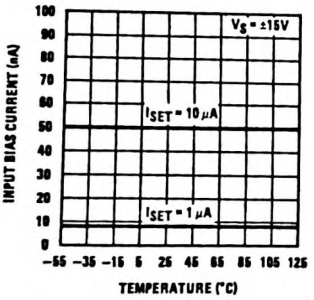
Input Voltage Range vs Supply Voltage



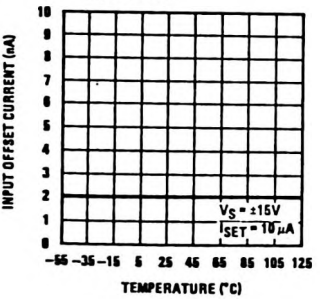
Input Bias Current vs Input Common-Mode Voltage



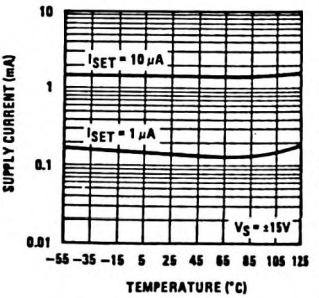
Input Bias Current vs Temperature



Input Offset Current vs Temperature

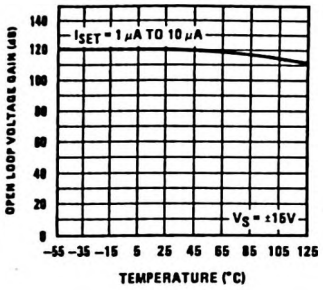


Supply Current vs Temperature

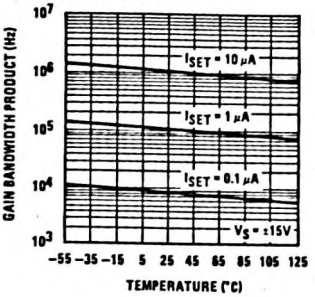


*Typical Performance Characteristics (Continued)

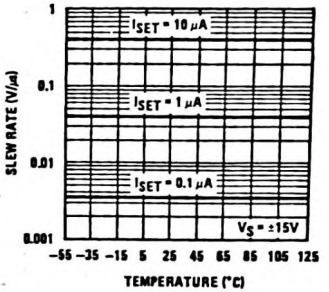
Open Loop Voltage Gain vs Temperature



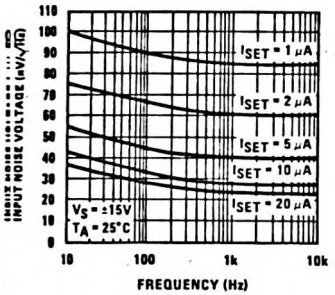
Gain Bandwidth Product vs Temperature



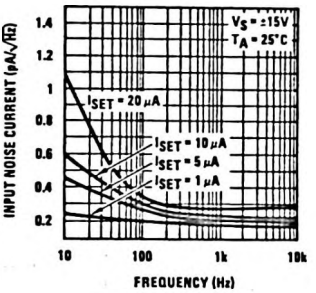
Slew Rate vs Temperature



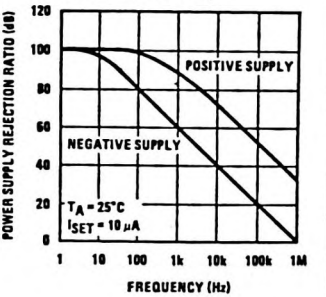
Input Noise Voltage vs Frequency



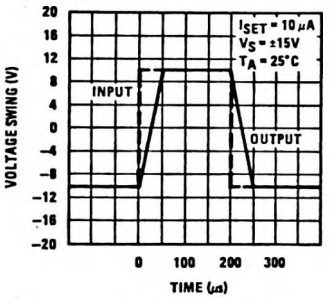
Input Noise Current vs Frequency



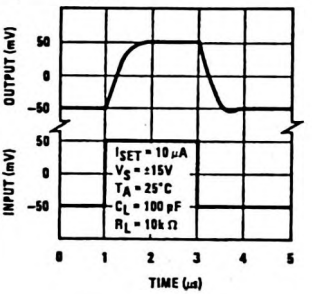
Power Supply Rejection Ratio vs Frequency



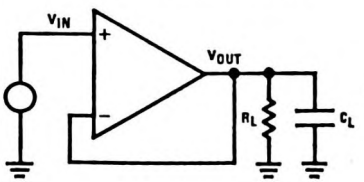
Voltage Follower Pulse Response



Voltage Follower Transient Response



Transient Response Test Circuit



Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.

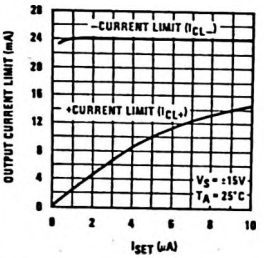


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.

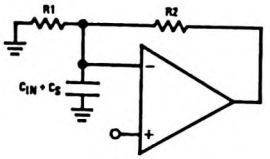


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

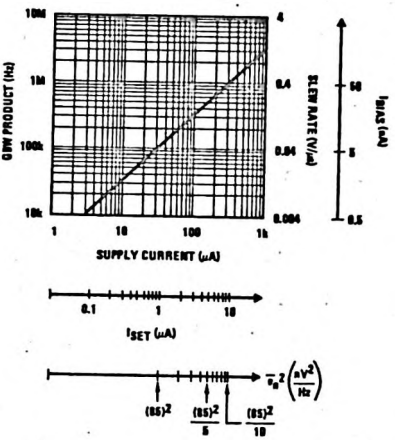


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

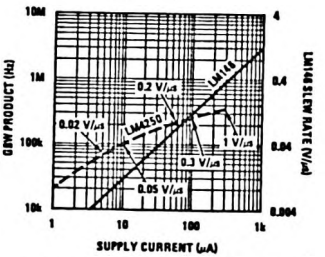
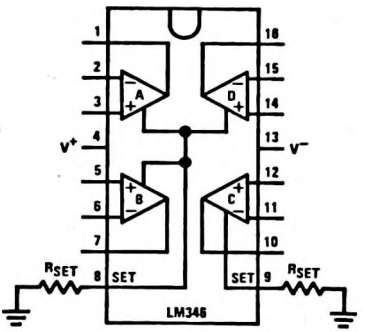


FIGURE 4. LM146 vs LM4250

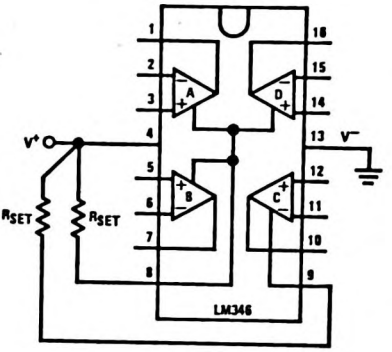
*Typical Applications

Dual Supply or Negative Supply Biasing



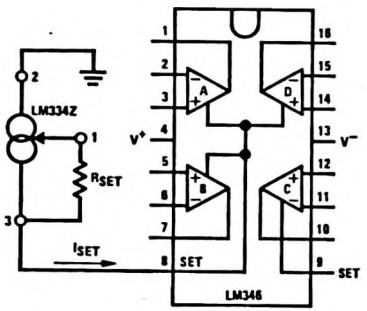
$$I_{SET} \simeq \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



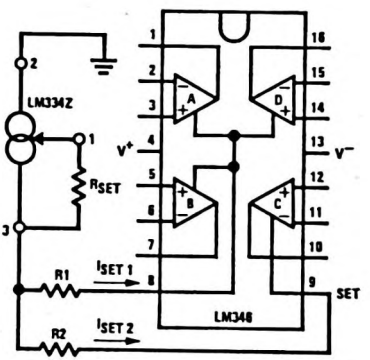
$$I_{SET} \simeq \frac{V^+ - 0.6V}{R_{SET}}$$

Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

Biasing all 4 Amplifiers with Single Current Source

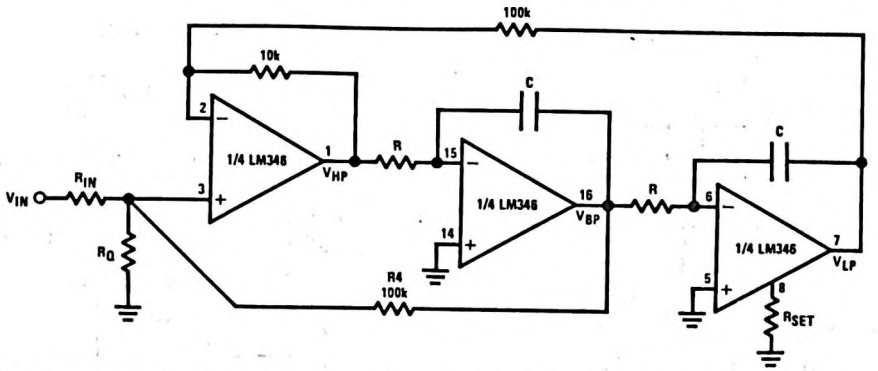


$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product temperature coefficient of the LM346.
- For $I_{SET1} \simeq I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

  Circuit synthesis equations (for circuit analysis equations, consult with the AF100 and LM148 data sheet).

  Need to know desired: f_o = center frequency measured at the BP output
  Q_o = quality factor measured at the BP output
  H_o = gain at the output of interest (BP or HP or LP or all of them)

  ▲ Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$

  ▲ $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)

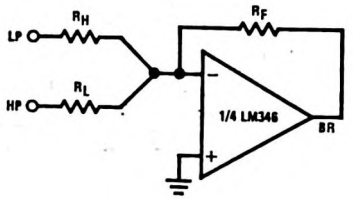
  ▲ For BP output: $R_Q = \left(\dfrac{3.478\,Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.478 \times Q_o}\right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\,Q_o}{H_{o(BP)}} - 1\right)}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For HP output: $R_Q = \dfrac{1.1 \times 10^5}{3.478\,Q_o\,(1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  Note. All resistor values are given in ohms.

  ▲ For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\,Q_o\,(11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\ \frac{f_{notch}}{f_o}$$

Determine R_F according to the desired gains: $H_{o(BR)}\ _{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\ _{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\,\mu A} \times \frac{1}{f_o \times H_o}\ \text{(Volts)}$$

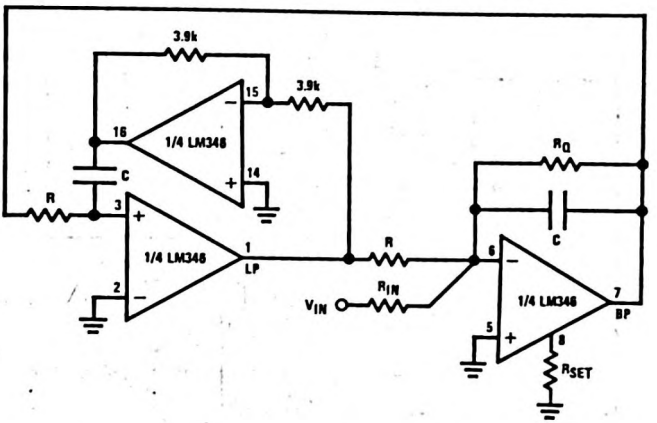
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \simeq \frac{f_o}{1 + \dfrac{2\,f_o}{GBW}}\ ,\ Q_{real} \simeq \frac{Q_o}{1 - \dfrac{3.2\,f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



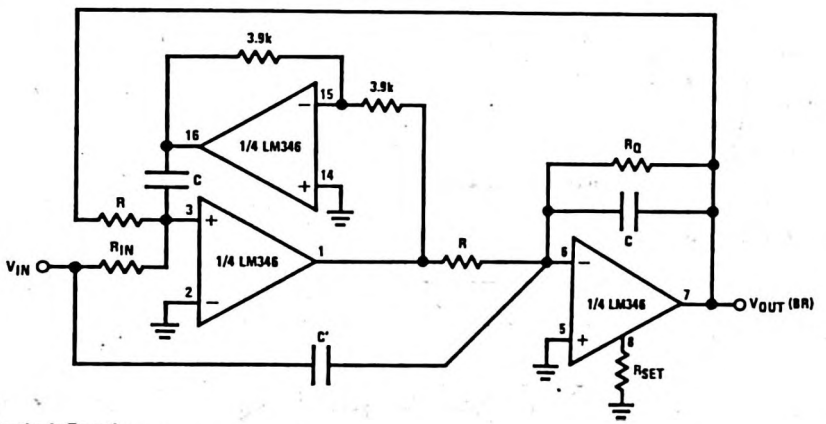
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



Circuit Synthesis Equations

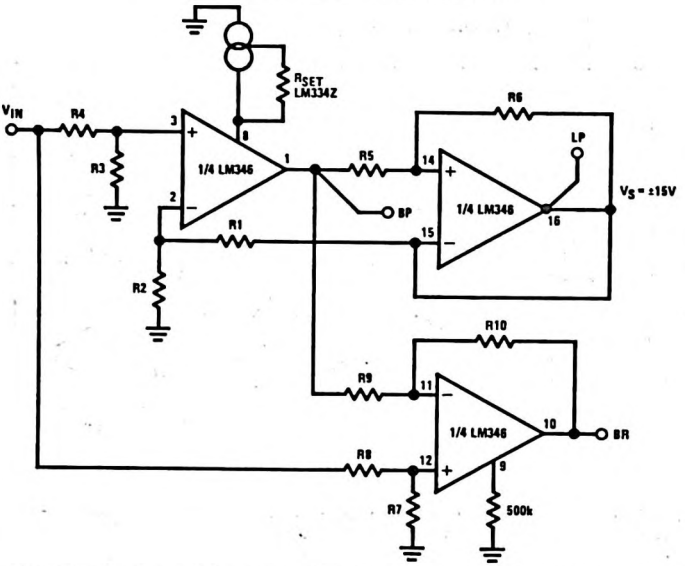
$$R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}}\ H_{o(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)

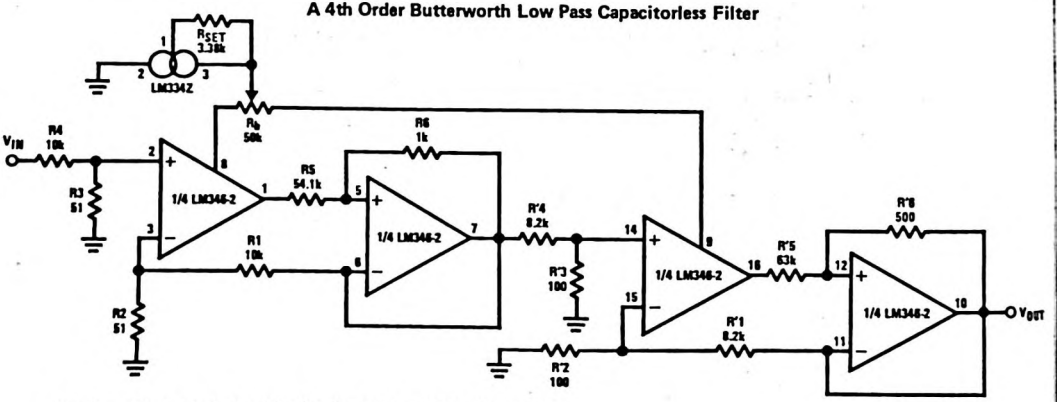


- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- Limitations: $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $V_{peak(out)} \leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}\ (\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R9 + R10}$, $f_{o(BP)} = f_u \sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$,

  $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)} \left(1 - \frac{c}{b}\right) \simeq f_{o(BP)}$ $(C << 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.
- Advantage: f_o, Q_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}

A 4th Order Butterworth Low Pass Capacitorless Filter

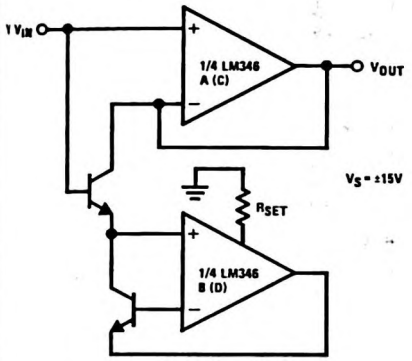


Ex: f_c = 20 kHz, H_o (gain of the filter) = 1, Q_{o1} = 0.541, Q_{o2} = 1.306.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

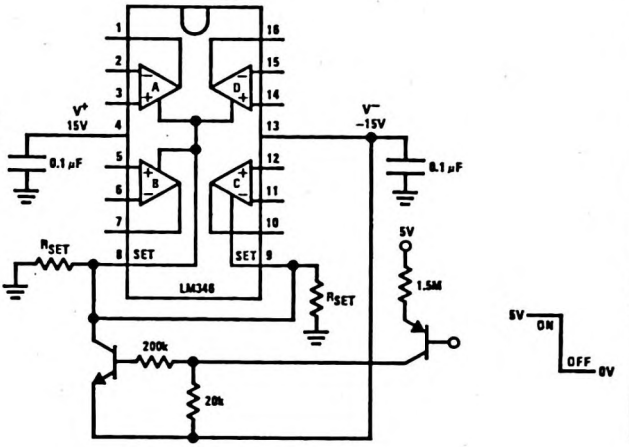
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



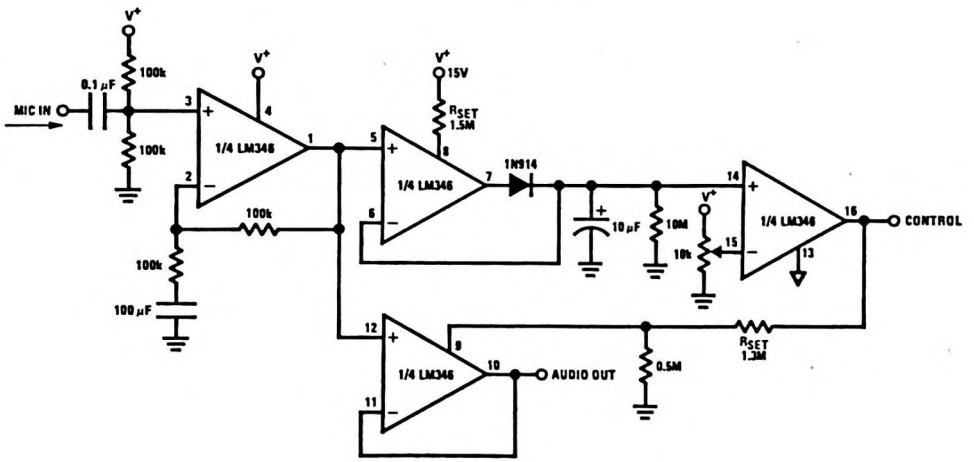
•• For better performance, use a matched NPN pair.

Circuit Shutdown



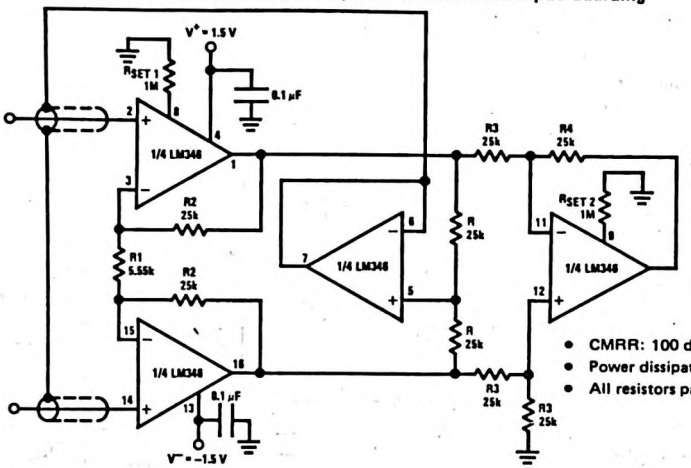
• By pulling the SET pin(s) to V⁻ the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier



Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW
- All resistors part of RA201 array

Section 10

Resistor Arrays

10

National Semiconductor

RA201 Precision Instrumentation Amplifier Resistor Network

General Description

The RA201 is a family of precision instrumentation amplifier networks. This device, when combined with 3 operational amplifiers, provides a precision instrumentation amplifier with common-mode rejection up to 100 dB. All gain setting resistors are provided within the device. This feature assures excellent thermal tracking and thermal matching of all resistors. This network is manufactured using a high stability thin-film technology. Thin-film resistors provide tracking temperature coefficients of better than 5 ppm/°C. The thin-film resistors are laser trimmed to guarantee resistor matching to 0.05% for the RA201-2, and 0.1% for the RA201-1.

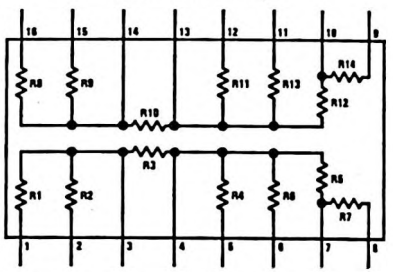
Other applications include process control interfacing and precision decade dividers.

Features

- Gain programmable
- Matching accuracies to 0.05%.
- Matching temperature coefficient to 5 ppm/°C
- Absolute temperature coefficient to 80 ppm/°C
- Close thermal proximity of all resistors
- Standard dual-in-line package
- Low-cost

Connection Diagram

Dual-In-Line Package



TOP VIEW

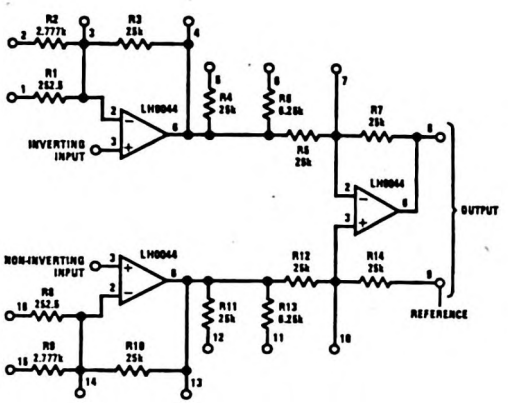
Order Number RA201D
See NS Package D16C

Order Number RA201N
See NS Package N16A

R1 = 252.525 . . Ω
R2 = 2.777 . . . kΩ
R3 = 25k
R4 = 25k
R5 = 25k
R6 = 6.25k
R7 = 25k
R8 = 252.525 . . . Ω
R9 = 2.777 . . . kΩ
R10 = 25k
R11 = 25k
R12 = 25k
R13 = 6.25k
R14 = 25k

R3:R2 = 9:1
R3:R1 = 99:1
R3||R2 = 2.50k
R3||R1 = 250.0Ω
R5||R6 = 5.0k

Typical Application



Overall Gain	Input Stage Gain	Output Stage Gain	Jumper Pins on RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Absolute Maximum Ratings

Rated Voltage Between Sections	200V
Rated Voltage Across Resistors	(Note 1)
Package Power Dissipation at 25°C (See Curve)	2.0W
Individual Resistor Power at 25°C	0.25W
Operating Temperature Range	
RA201-1N, RA201-2N	−25°C to +85°C
RA201-1D, RA201-2D	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A = 25°C (Note 2)

PARAMETER	CONDITIONS; RESISTORS TESTED	TYP	RA201-2 MAX	RA201-1 MAX	UNITS
Input Stage x10	R2:R3	1:9	±0.05	±0.1	%
	(R2||R9):(R3||R10)	1:9	±0.05	±0.1	%
Input Stage x100	R1:R3	1:99	±1	±1	%
	(R8||R1):(R3||R10)	1:99	±1	±1	%
Output Stage x1	R7:R5	1:1	±0.05	±0.1	%
	R14:R12	1:1	±0.05	±0.1	%
Output Stage x2	(R4||R5):R7	1:2	±0.05	±0.1	%
	(R12||R11):R14	1:2	±0.05	±0.1	%
Output Stage x5	(R6||R5):R7	1:5	±0.05	±0.1	%
	(R12||R13):R14	1:5	±0.05	±0.1	%
Output Stage CMRR	(R7:R5):(R14:R12), (Note 3)	1:1	±0.05	±0.1	%
Absolute Tolerance	R3	25 kΩ	±5	±5	%
Absolute Tempco		80			ppm/°C

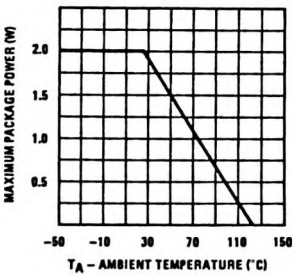
Note 1: Rated voltage is limited by the individual resistor power rating of 0.25W. For example, a 25k resistor could withstand a maximum of $V = \sqrt{(0.25)(25{,}000)} = 79V$. This rating may need to be reduced to be consistent with maximum package power if several resistors are dissipating power simultaneously.

Note 2: Resistor ratios shown apply at T_A = 25°C; for $T_{MIN} \leq T_A \leq T_{MAX}$ the ratio tolerances are double the specifications shown.

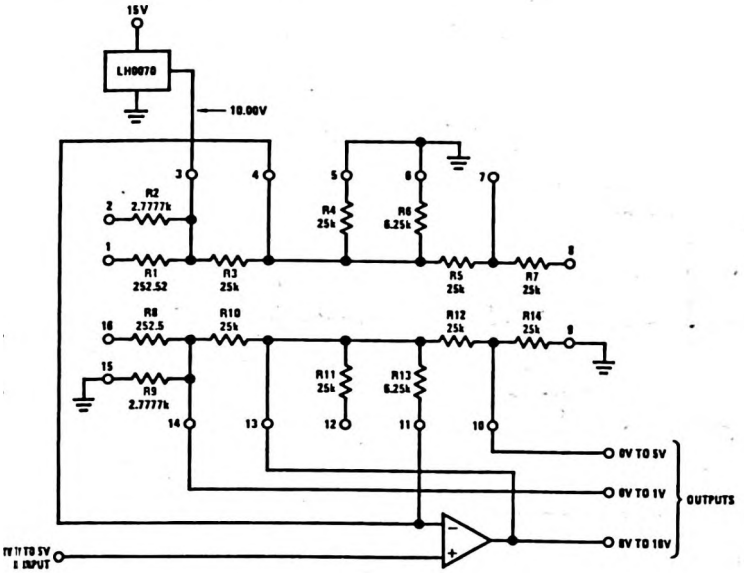
Note 3: This test guarantees the CMRR contributed by resistance mismatch. In low gain applications, all 3 amplifiers contribute strongly to the overall CMRR. In high gain applications, the degradation due to resistor mismatch and output stage CMRR are divided by the gain of the input stage.

Typical Performance Characteristics

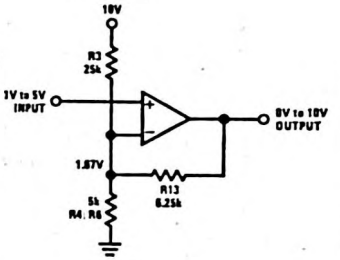
Power Derating



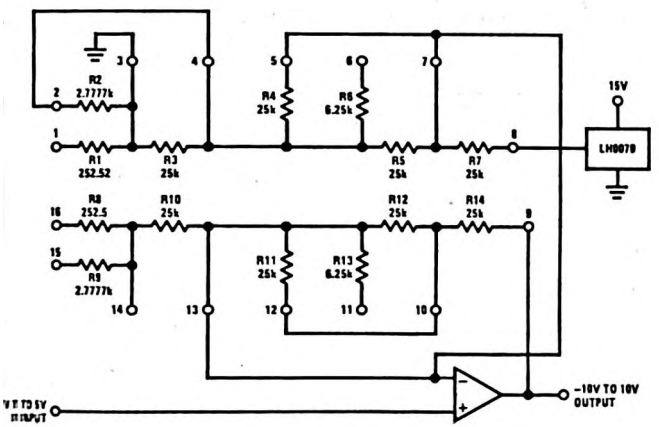
Applications Information



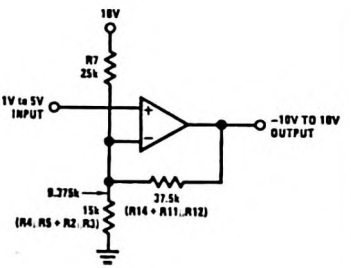
RA201 Process Control Interface No. 1



Equivalent Circuit



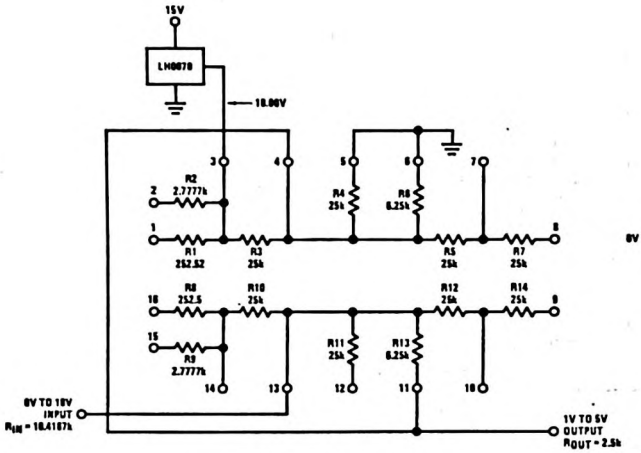
RA201 Process Control Interface No. 2



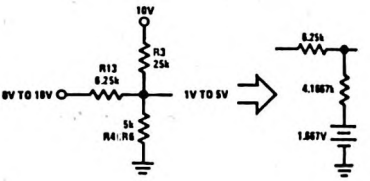
Equivalent Circuit

10

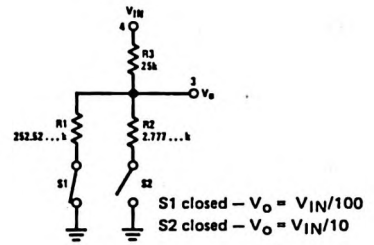
Applications Information (Continued)



RA201 Process Control Interface No. 3



Equivalent Circuit



Precision Decade Divider

Section 11

Active Filters

11

AF100 Universal Active Filter

general description

The AF100 state variable active filter is a general second order lumped RC network. Only four external resistors program the AF100 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs in the uncommitted output summing amplifier. Higher order systems are realized by cascading AF100 active filters with appropriate programming resistors.

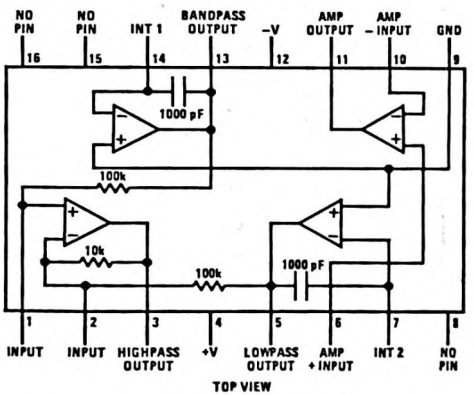
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be formed.

features

- Military or commercial specifications
- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using uncommitted amplifier
- Operates to 10 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- Frequency accuracy ±1% unadjusted
- Q frequency product $\leq$ 50,000

connection diagrams

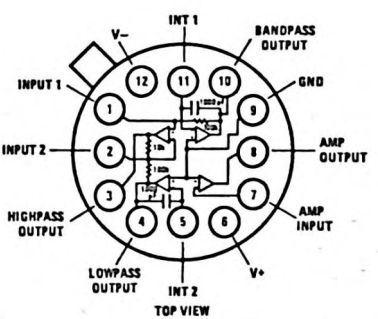
Dual-In-Line Package



TOP VIEW

Order Number AF100HY
See NS Package HY13A

Metal Can Package



TOP VIEW

Order Number AF100HY
See NS Package H12A

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short Circuit Duration (Note 1)	Infinite
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature	
AF100-1CJ/AF100-2CJ/AF100-1CG/AF100-2CG	−25°C to +85°C
AF100-1G, AF100-2G	−55°C to +125°C
Storage Temperature	
AF100-1G, AF100-2G, AF100-1CG, AF100-2CG	−65°C to +125°C
AF100-1CJ, AF100-2CJ	−25°C to +100°C

electrical characteristics (Complete Active Filter) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_C \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_C \times Q \leq 50{,}000$			500	Hz/Hz
f_O Accuracy					
AF100-1, AF100-1C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±2.5	%
AF100-2, AF100-2C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±1.0	%
f_O Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	$V_S = ±15V$		2.5	4.5	mA

electrical characteristics (Internal Op Amp) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$, $V_{OUT} = ±10V$	25	160		V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range		±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely, however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for $V_S = ±15V$, over −25°C to +85°C for the AF100-1C and AF100-2C and over −55°C to +125°C for the AF100-1 and AF100-2, unless otherwise specified.

Note 3: Specifications apply for $V_S = ±15V$, $T_A = 25°C$.

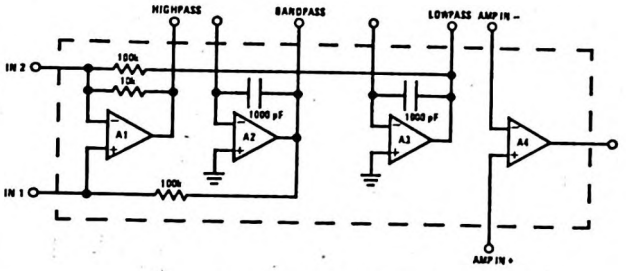


FIGURE 1. AF100 Schematic

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF100 is shown in *Figure 1.* Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_0 = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_0}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(highpass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(bandpass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(lowpass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and allpass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals 1, and a_3 equals ω_Z^2. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_Z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(notch)}$$

In the allpass transfer function $a_1 = 1$, $a_2 = -\omega_0/Q$ and $a_3 = \omega_0^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(allpass)}$$

COMMON CONFIGURATIONS

The specific transfer functions for some of the most useful circuit configurations using the AF100 are illustrated in *Figures 2 through 8.* Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation.

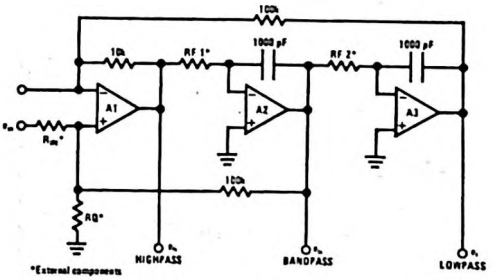


FIGURE 2. Non-inverting Input (Q > Q_{MIN}. See Q Tuning Section)

applications information (con't)

a) Non-inverting input *(Figure 2)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \omega_1\omega_2\left[\frac{\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}}{\Delta}\right] \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}\right)}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left(\frac{1+\dfrac{10^5}{R_{IN}}+\dfrac{10^5}{RQ}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)}$$

$$RQ = \frac{10^5}{\left(\dfrac{1.1Q}{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}\right) - 1 - \dfrac{10^5}{R_{IN}}}$$

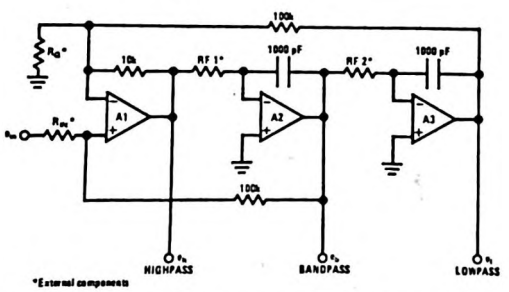


FIGURE 3. Non-Inverting Input (Q < Q_{MIN}. See Q Tuning Section)

b) Non-inverting input *(Figure 3)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{\omega_1\omega_2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s\to 0} = \frac{1.1+\dfrac{10^4}{RQ}}{0.1\left(1+\dfrac{R_{IN}}{10^5}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{1+\dfrac{10^5}{R_{IN}}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1+\dfrac{10^5}{R_{IN}}}{1.1+\dfrac{10^4}{RQ}}\right]\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^4}{\left(1+\dfrac{10^5}{R_{IN}}\right)\left(\dfrac{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}{Q}\right) - 1.1}$$

applications information (con't)

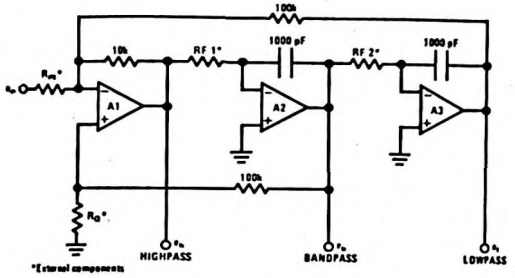


FIGURE 4. Inverting Input

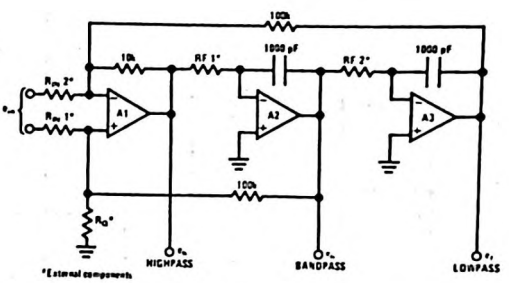


FIGURE 5. Differential Input

c) Inverting input *(Figure 4)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2 \frac{10^4}{R_{IN}}}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1 \frac{10^4}{R_{IN}}}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{-\omega_1\,\omega_2 \frac{10^4}{R_{IN}}}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \frac{10^4}{R_{IN}}}{1 + \frac{10^5}{R_Q}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = -\frac{10^5}{R_{IN}} \quad \text{(lowpass)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = -\frac{10^4}{R_{IN}} \quad \text{(highpass)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\frac{10^4}{R_{IN}}\left(1 + \frac{10^5}{RQ}\right)}{1.1 + \frac{10^4}{R_{IN}}} \quad \text{(bandpass)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \frac{10^5}{RQ}}{1.1 + \frac{10^4}{R_{IN}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\frac{Q}{\sqrt{0.1 \frac{\omega_2}{\omega_1}}} \left(1.1 + \frac{10^4}{R_{IN}}\right) - 1}$$

d) Differential input *(Figure 5)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \frac{10^4}{R_{IN2}}}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \frac{10^4}{R_{IN2}}}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \frac{10^4}{R_{IN2}}}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \frac{10^4}{R_{IN2}}}{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN1}}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = \frac{10^5}{R_{IN2}}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{10^4}{R_{IN2}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\frac{10^4}{R_{IN2}}\left(1 + \frac{10^5}{R_{IN1}} + \frac{10^5}{RQ}\right)}{\left(1.1 + \frac{10^4}{R_{IN2}}\right)}$$

$$Q = \left[\frac{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN1}}}{1.1 + \frac{10^4}{R_{IN2}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\frac{Q}{\sqrt{0.1 \frac{\omega_2}{\omega_1}}} \left(1.1 + \frac{10^4}{R_{IN2}}\right) - 1 - \frac{10^5}{R_{IN1}}}$$

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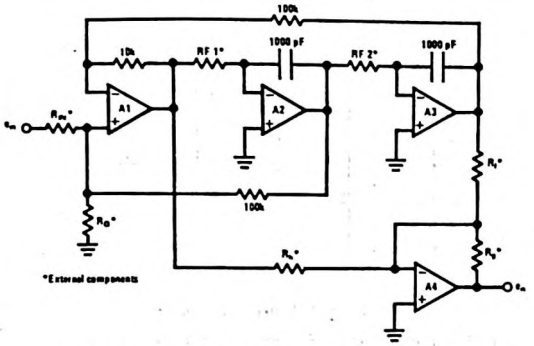

FIGURE 6. Output Notch Using All Four Amplifiers

e) Output notch *(Figure 6)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_z^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_z = \omega_0\sqrt{\frac{10\,R_h}{R_Q}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_Q}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_h}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_z} = 0$$

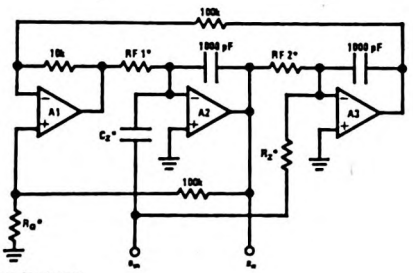

FIGURE 7. Input Notch Using Three Amplifiers

j) Input notch *(Figure 7)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{\frac{-C_z}{10^{-9}}\left[s^2 + \omega_z^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,RQ}{10^5 + RQ}\right] + \omega_0^2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_z = \omega_0\sqrt{\frac{RF2 \times 10^{-9}}{R_z\,C_z}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = -\frac{R_{F2}}{R_z}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_z}{10^{-9}}$$

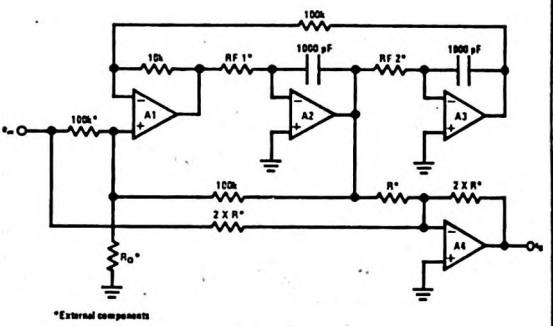

FIGURE 8. Allpass

g) Allpass *(Figure 8)* transfer function equations are:

$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0^2}\right]$$

$$Q = \frac{2 + \frac{10^5}{RQ}}{1.1}\sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at $\omega_0 = \frac{2Q}{\omega_0}$ seconds

FREQUENCY TUNING

To tune the AF100 two resistors are required for frequencies between 200 Hz and 10 kHz. For lower frequencies "T" tuning or addition of external capacitors

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is required. Using external capacitors allows the user to go as low in frequency as he desires. "T" tuning and external capacitors can be used together.

Two resistor tuning for 200 Hz to 10 kHz

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega$$

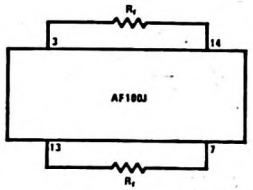
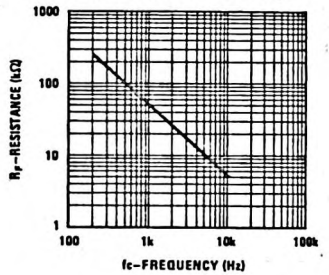


FIGURE 9. Resistive Tuning

GRAPH A. Resistive Tuning



"T" resistive tuning for $f_O < 200$ Hz

$$R_s = \frac{R_t^2}{R_f - 2R_t} \qquad R_t < \frac{R_F}{2}$$

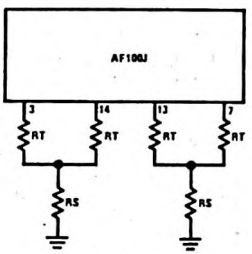
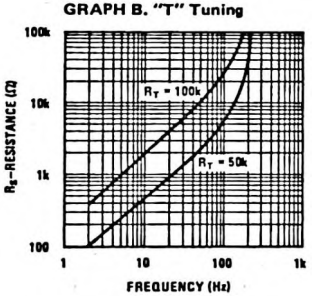


FIGURE 10. T Tuning

GRAPH B. "T" Tuning



RC tuning for $f_O < 200$ Hz

$$R_f = \frac{0.05033}{f_o\,(C + 1 \times 10^{-9})}$$

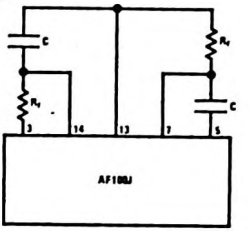
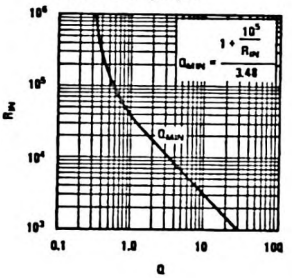


FIGURE 11. Low Frequency RC Tuning

Q TUNING

To tune the Q of an AF100 requires one resistor from pins 1 or 2 to ground. The value of the Q tuning resistor depends on the input connection and input resistance as well as the value of the Q. The Q of the unit is inversely proportional to resistance to ground at pin 1 and directly proportional to resistance to ground from pin 2.

GRAPH C. Q_{MIN}, Non-Inverting Input



For $Q > Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}}$$

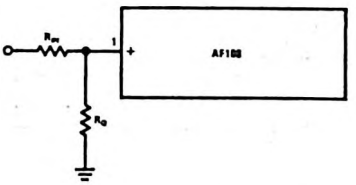


FIGURE 12. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

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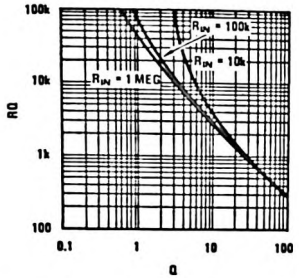
GRAPH D. Q > Q_{MIN}, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^4}{0.3162 \frac{\left(1 + \frac{10^5}{R_{IN}}\right)}{Q} - 1.1}$$

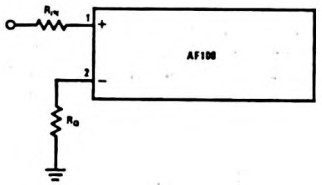
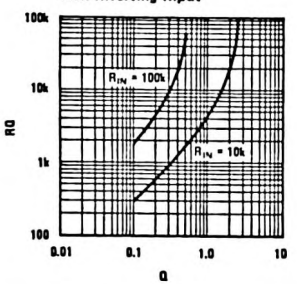


FIGURE 13. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. $Q < Q_{MIN}$, Non-Inverting Input



For any Q in inverting mode:

$$RQ = \frac{10^5}{3.16Q \left(1.1 + \frac{10^4}{R_{IN}}\right) - 1}$$

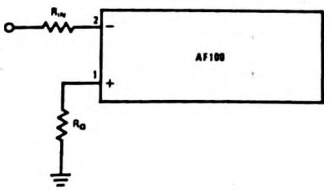
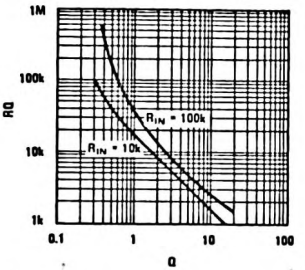


FIGURE 14. Q Tuning Inverting Input

GRAPH F. Q Tuning, Inverting Input



NOTCH TUNING

Two methods to generate notches are the RC input and lowpass/highpass summing. The RC input method requires adding a capacitor and resistor connected to the two integrator inputs. The capacitor connects to "Int 1" and the resistor connects to "Int 2." The output summing requires two resistors connected to the lowpass and highpass output.

For input RC notch tuning:

$$R_Z = C_Z \, R_F \times 10^9 \left(\frac{f_O}{f_Z}\right)^2$$

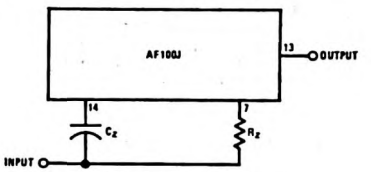
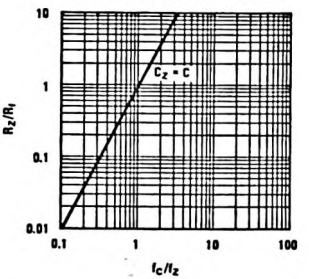


FIGURE 15. Input RC Notch

GRAPH G. Input RC Notch



For output notch tuning:

$$R_{HP} = \left(\frac{f_Z}{f_O}\right)^2 \frac{R_{LP}}{10}$$

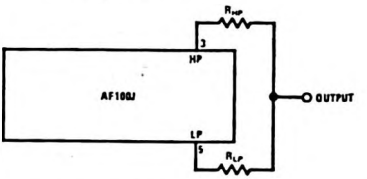


FIGURE 16. Output Notch

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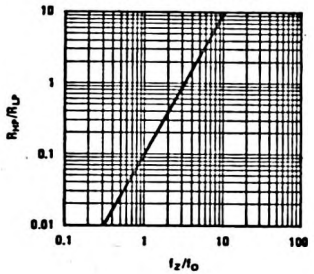
GRAPH H. Output Notch



TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF100 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the bandpass (pin 13) output.

Before any tuning is attempted the lowpass (pin 7) output should be checked to see that the output is not clipping. At the center frequency of the section the lowpass output is 10 dB higher than the bandpass output and 20 dB higher than the highpass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

"Q" Tuning

The "Q" is tuned by adjusting the resistance between pin 1 or 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

where f_o = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (lowpass/highpass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE (See *Figure 17*)

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the lowpass output pin 5 (AF100J).

Adjust the resistance between pins 13 and 7 until the phase shift between input and bandpass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

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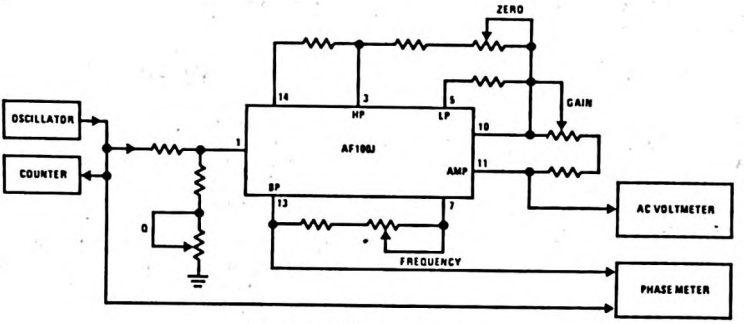


FIGURE 17. Filter Tuning Setup

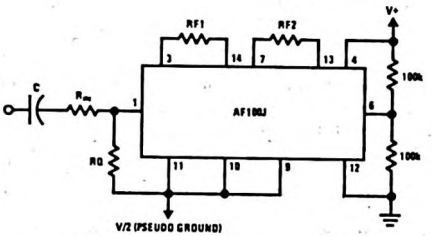


FIGURE 18. Single Power Supply Connection Using Uncommitted Amplifier to Split Supply

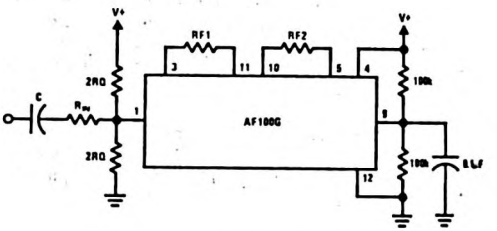
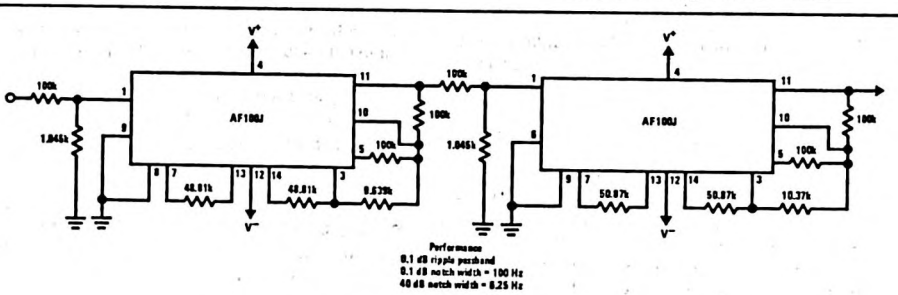


FIGURE 19. Single Power Supply Connection Using Resistive Dividers



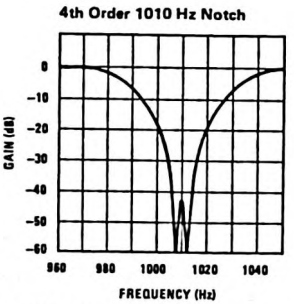


FIGURE 20. 1010 Hz Notch—Telephone Holding Tone Reject Filter

FILTER DESIGN

Since most filter tables are in terms of a normalized lowpass prototype, the filter to be designed is usually reduced to a lowpass prototype. After the lowpass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. *Graph I* shows the lowpass amplitude response which can be defined by four quantities.

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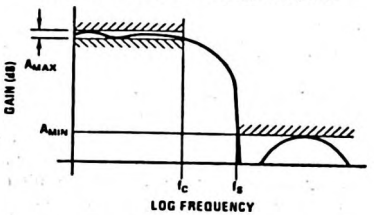
GRAPH I. Lowpass Prototype Response



A_{MAX} = the maximum peak to peak ripple in the passband.

A_{MIN} = the minimum attenuation in the stopband.

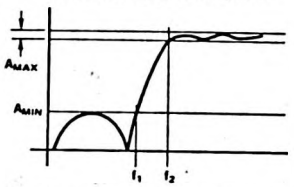
f_C = the passband cutoff frequency.

f_S = the stopband start frequency.

By defining these four quantities for the lowpass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the lowpass prototype for the highpass filter (*Graph J*) A_{MAX} and A_{MIN} are the same as for the lowpass case but $f_C = 1/f_2$ and $f_S = 1/f_1$.

GRAPH J. Highpass Response



To obtain the lowpass prototype for a bandpass filter (*Graph K*) A_{MAX} and A_{MIN} are the same as for the lowpass case but

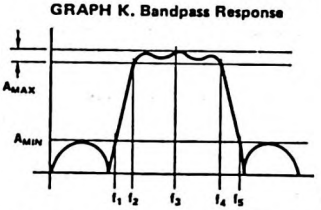
$$f_C = 1 \quad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$ i.e. geometric symmetry

$f_5 - f_1$ = A_{MIN} bandwidth

$f_4 - f_2$ = Ripple bandwidth

GRAPH K. Bandpass Response

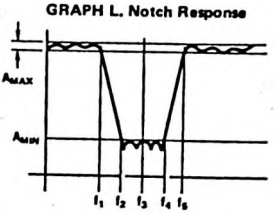


To obtain the lowpass prototype for the notch filter (*Graph L*) A_{MAX} and A_{MIN} are the same as for the lowpass case and

$$f_C = 1 \qquad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$

GRAPH L. Notch Response



Normalized Lowpass Transformed To Un-Normalized Lowpass

The normalized lowpass filter has the passband edge normalized to unity. The un-normalized lowpass filter instead has the passband edge at f_C. The normalized and un-normalized lowpass filters are related by the transformation $s = s\omega_c$. This transforms the normalized passband edge $s = j$ to the un-normalized passband edge $s = j\omega_C$.

Normalized Lowpass Transformed To Un-Normalized Highpass

The transformation that can be used for lowpass to highpass is $S = \omega_C/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized lowpass $1/(S^2 + S/Q+1)$ transforms to the un-normalized highpass

$$\frac{s^2}{s^2 + \frac{\omega_C}{Q}s + \omega_C{}^2}$$

Normalized Lowpass Transformed To Un-Normalized Bandpass

The transformation that can be used for lowpass to bandpass is $S = (s^2 + \omega_0{}^2)/BWs$ where $\omega_0{}^2$ is the center frequency of the desired bandpass filter and BW is the ripple bandwidth.

Normalized Lowpass Transformed To Un-Normalized Bandstop (Or Notch)

The bandstop filter has a reciprocal response to a bandpass filter. Therefore a bandstop filter can be obtained by first transforming the lowpass prototype to a highpass and then performing the bandpass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Tschebycheff, Elliptic, and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

applications information (con't)

The Tschebycheff function is a min/max approximation in the passband. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the passband. The Tschebycheff approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the passband and stopband and have a steeper transition region than the Butterworth or the Tschebycheff.

For a specific lowpass filter three quantities can be used to determine the degree of the transfer function: the maximum passband ripple, the minimum stopband attenuation, and the transition ratio ($tr = \omega_S/\omega_C$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers," Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs," John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis," McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design," McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Lowpass, highpass, bandpass, notch, allpass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability

   Insertion loss/gain plus tolerance and stability

   Source impedance

   Load impedance

   Maximum output noise

   Power consumption

   Power supply voltage

   Dynamic range

   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

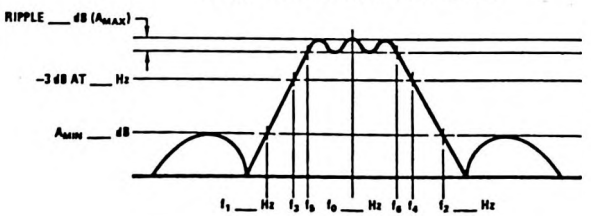
First Order	Second Order	
$\frac{K}{s + \omega_R}$	$\frac{K}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	(low pass)
$\frac{Ks}{s + \omega_R}$	$\frac{Ks^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	(highpass)
	$\frac{Ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	(bandpass)
	$\frac{K(s^2 + \omega_Z^2)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	(notch)
	$\frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	(allpass)

Each of the second order functions is realizable by tuning an AF100 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

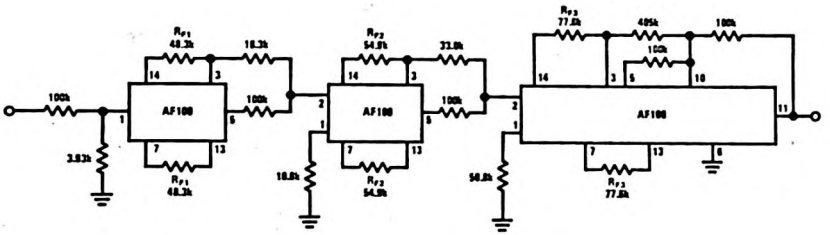
The primary concern in cascading second order stages is to minimize the maximum difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

GRAPH M. Generalized Model Response



applications information (con't)

1. The highest "Q" pole pair should be paired with the zero pair closest in frequency.
2. If highpass and lowpass stages are cascaded the lowpass sections should be the higher frequency and highpass sections the lower frequency.
3. In cascaded filters of more than two sections the first section should be the section with "Q" closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.



Lowpass Elliptic Filter

$F_C = 1$
$F_S = 1.3$
$A_{MAX} = 0.1$ dB
$A_{MIN} = 40$ dB
$N = 6$

$f_{O1} = 1.0415 \quad Q_1 = 7.88 \quad f_{Z1} = 1.329 \quad f_Z/f_O = 1.28 \quad \left(\frac{f_Z}{f_O}\right)^2 = 1.63$

$f_{O2} = 0.9165 \quad Q_2 = 1.79 \quad f_{Z2} = 1.664 \quad f_Z/f_O = 1.82 \quad \left(\frac{f_Z}{f_O}\right)^2 = 3.30$

$f_{O3} = 0.649 \quad Q_3 = 0.625 \quad f_{Z3} = 4.1285 \quad f_Z/f_O = 6.36 \quad \left(\frac{f_Z}{f_O}\right)^2 = 40.5$

$$R_{F1} = \frac{(503.3)}{f_{O1} \times f_C} \times 10^5 \qquad R_{F2} = \frac{(503.3)}{f_{O2} \times f_C} \times 10^5 \qquad R_{F3} = \frac{(503.3)}{f_{O3} \times f_C}$$

at 1000 Hz = f_C

$R_{F1} = 48.3k \qquad R_{F2} = 54.9k \qquad R_{F3} = 77.6k$

6th Order Elliptic Filter

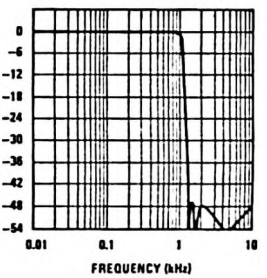
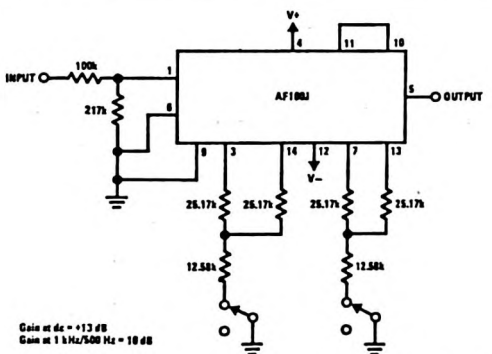


FIGURE 21. Lowpass Elliptic Filter Example



500/1000 Hz Switchable Butterworth Lowpass Filter

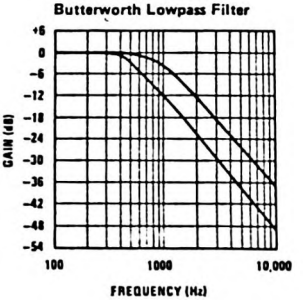
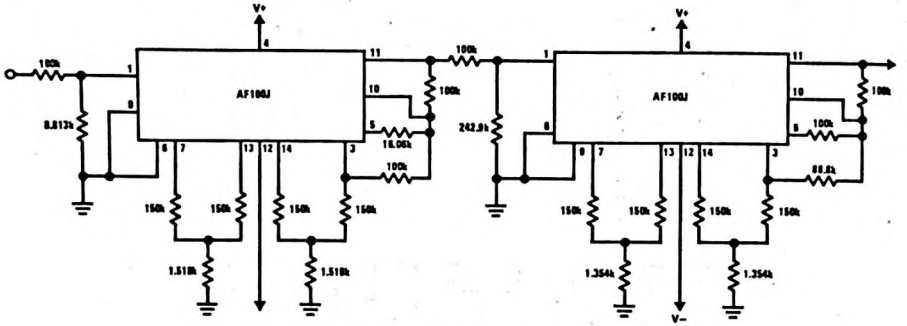


FIGURE 22. Switchable Filter Example: 500 Hz/1000 Hz Butterworth Lowpass

applications information (con't)



EEG Delta Filter

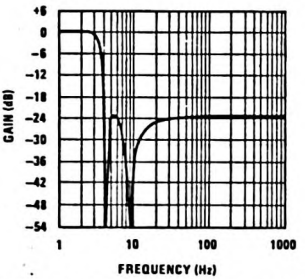


FIGURE 23. EEG Delta Filter—3 Hz Lowpass

Limits and Conditions for Use with Test Circuit

TEST	CONDITION	LIMIT	SWITCH POSITION
f_C	Phase Shift 180°	503.3 Hz ±1%	2
Q	$Q = \frac{f_C}{BW}$	20 ±7.5%	2
	$BW = f_{-45°} - f_{+45°}$		
A_{HP}	Measured at f_C 2k load	−10 dB ±0.15 dB	1
A_{BP}	Measured at f_C 2k load	0 ±0.15 dB	2
A_{LP}	Measured at f_C 2k load	+10 dB ±0.15 dB	3
A_{AMP}	Measured at f_C 2k load	0 ± 0.1 dB	4
DC Offset	Input Level 0V	±200 mV max	3
Power Supply Current	No Input Signal	4.5 mA max	–

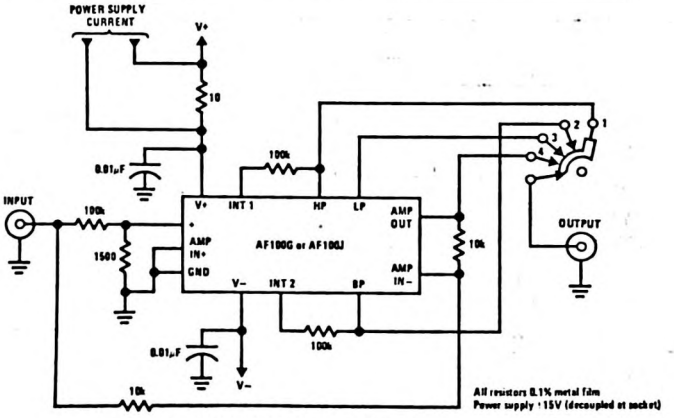


FIGURE 24. Device Test Fixture

applications information (con't)

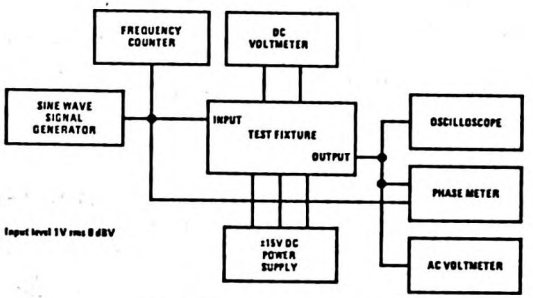


FIGURE 25. Test Circuit Block Diagram

COMPUTER AIDED DESIGN EXAMPLE*

This design is an example of a 60 Hz notch filter. The response is to have the following specifications:

Maximum passband ripple 0.1 dB

Minimum rejection 35 dB

0.1 dB bandwidth 15 Hz max

−35 dB bandwidth 1.5 Hz min

The steps in the design of this filter are:

1. Design a lowpass "prototype" for the filter.
2. Transformation of the lowpass prototype into a notch filter design.
3. Using the pole and zero locations found in step two calculate the value of the resistors required to build the filter.
4. Draw a schematic of filter using values obtained in step three.

*Computer programs shown are user interactive. Underlined copy is user input, non-underlined copy is computer response, and line indications in parenthesis are included for easy identification of data common to several programs.

PROGRAM NO. 1

```
RUN

THIS PROGRAM DESIGNS BUTTERWORTH CHEBYCHEFF OR ELLIPTIC NORMALIZED
LOWPASS FILTERS
WHAT TYPE OF FILTER ? B-C-E

ELLIPTIC
 DO YOU KNOW THE ORDER OF THE FILTER ? Y/N
? NO
INPUT FC,FS,AMAX,AMIN
? 1, 10, .1, 35
     FC                1.000
     FS               10.000
     AMAX               .100
     AMIN             35.000
     N                 2.000
     ATT AT FS       −35.671    (ATTENUATION IN dB)
IS THIS SATISFACTORY ? Y/N
? YES

   F                 Q
    1.823 (Line 1.1)      .775 (Line 1.2)
   Z
   14.124 (Line 1.3)
```

applications information (con't)

PROGRAM NO. 2
(DETERMINES UN-NORMALIZED
POLE + ZERO LOCATIONS OF FIRST SECTION)
(DATA ENTERED FROM PROGRAM NO. 1)

```
RUN
WHAT TYPE FILTER BANDPASS OR NOTCH
? NOTCH
ENTER # OF POLE PAIRS? 1

ENTER # OF JW AXIS ZEROS? 1

  ENTER # OF REAL POLES? 0

  ENTER # OF ZEROS AT ZERO? 0

  ENTER # OF COMPLEX ZEROS? 0

ENTER # OF REAL ZEROS? 0

   ENTER F & Q OF EACH POLE PAIR
? 1.823, .775  (FROM LINE 1.1 AND LINE 1.2)

ENTER VALUES OF JW AXIS ZEROS
? 14.124  (FROM LINE 1.3)

ENTER FREQUENCY SCALING FACTOR
? 1
  ENTER THE # OF FILTERS TO BE DESIGNED
? 1
  ENTER THE C.F. AND BW OF EACH FILTER
? 60, 15
```

OUTPUT OF PROGRAM NO. 2
TRANSFORMED POLE/ZERO LOCATIONS
FIRST SECTION

```
                POLE LOCATIONS
CENTER FREQ.                    Q

56.93601   (From Line 2.3)     11.31813  (From Line 2.4)
63.228877  (From Line 2.5)     11.31813  (From Line 2.6)
              JW AXIS ZEROS

59.471339  (From Line 2.1)
60.533361  (From Line 22
```

PROGRAM NO. 3
(CHECK OF FILTER RESPONSE USING
PROGRAM NO. 2 DATA BASE)

```
RUN

NUMERATOR (ZEROS)
A(I)S^2+R(I)S+Z(I)^2
 1     0     59.471339     (From Line 2.1)
 1     0     60.533361     (From Line 2.2)

REAL POLE

COMPLEX POLE PAIRS

        F          Q
1       56.93601   11.31813   (From Lines 2.3 and 2.4)
2       63.228877  11.31813   (From Lines 2.5 and 2.6)
```

RUN

FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY
40.000	.032	347.69	.002275	5.847169
45.000	.060	342.20	.004107	8.749738
50.000	.100	330.70	.009983	21.268142
55.000	-.795	290.54	.046620	99.324027
56.000	-2.298	270.61	.063945	136.234562
57.000	-5.813	245.51	.072894	155.299278
58.000	-12.748	220.19	.065758	140.096912
58.200	-14.740	215.54	.063369	135.006390
58.400	-17.032	211.06	.060979	129.914831
58.600	-19.722	206.76	.058692	125.043324
58.800	-22.983	202.61	.056588	120.561087
59.000	-27.172	198.60	.054724	116.589928
59.200	-33.235	194.72	.053139	113.212012
59.400	-46.300	190.94	.051856	110.478482
59.600	-42.909	7.24	.050888	108.417405
59.800	-36.897	3.60	.050242	107.040235
60.00	-35.567	360.00	.049916	106.346516
60.200	-36.887	356.41	.049907	106.326777
60.400	-42.757	352.81	.050206	106.963750
60.600	-47.102	169.17	.050801	108.232021
60.800	-33.650	165.48	.051677	110.096278
61.000	-27.577	161.72	.052809	112.508334
61.200	-23.418	157.87	.054167	115.403169
61.400	-20.198	153.92	.055712	118.694436
61.600	-17.554	149.85	.057391	122.270065
61.800	-15.308	145.65	.059136	125.989157
62.000	-13.362	141.33	.060869	129.681052
63.000	-6.557	118.23	.065975	140.559954
64.000	-2.936	95.30	.059402	126.556312
65.000	-1.215	76.38	.045424	96.774832
66.000	-.463	62.43	.032614	69.484719
67.000	-.138	52.44	.023498	50.062947
70.000	.091	35.43	.010452	22.267388
75.000	.085	23.44	.004250	9.054574
80.000	.060	17.80	.002310	4.921727
85.000	.043	14.50	.001460	3.110433
90.000	.032	12.31	.001011	2.154297

PROGRAM NO. 4
DESIGN OF FIRST SECTION

```
)RUN
WHICH FILTER AF100 –J OR G ?
? J
WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 56.93601, 11.31813  (FROM LINES 2.3 AND 2.4)
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 59.471339      (FROM LINE 2.1)
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES
```

TUNING INSTRUCTION

PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 56.93601 HZ.
IF TUNING IS REQUIRED, RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED.
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 59.506798HZ.
OR 225 DEG. AT 54.476284 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 59.471339 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 56.93601 Q= 11.31813 F(L–3DB) = 54.476284 F(H–3DB) = 59.506798

GAIN AT F)) FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	883960.996
RF2	7	13	883960.996
RLP	5	10	100000.000
RHP	3	10	10910.418
RG	10	11	357910.697
+V		4	
–V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

applications information (con't)

PROGRAM NO. 4
DESIGN OF SECOND SECTION

```
WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 63.228877, 11.31813  (FROM LINES 2.5 AND 2.6)
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 60.533361  (FROM LINE 2.2)
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES
```

TUNING INSTRUCTION

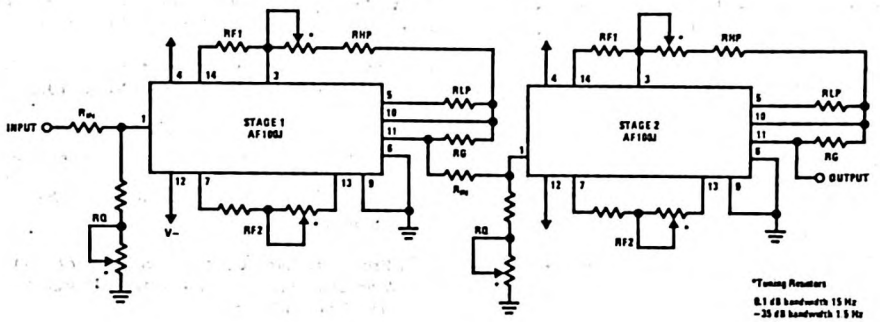
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 63.228877 HZ.
IF TUNING IS REQUIRED RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 66.083802 HZ.
OR 225 DEG. AT 60.497289 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 60.533361 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 63.228877 Q= 11.31813 F(L-3DB)= 60.497289 F(H-3DB)= 66.083802

GAIN AT F((FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	795984.596
RF2	7	13	795984.596
RLP	5	10	100000.000
RHP	3	10	9165.552
RG	10	11	328044.920
+V		4	
−V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

applications information (con't)



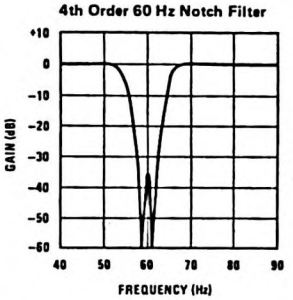


FIGURE 26. Implementation of a 60 Hz Notch From Computer Calculations

TEST PROCEDURE (Ref. *Figure 24*)

Center Frequency

The center frequency is measured by adjusted the signal generator for a 180° phase shift and then reading the input frequency on the counter.

Q

The Q is measured by measuring the bandwidth and dividing by the center frequency. To measure the bandwidth, increase the frequency of the signal generator until the phase shift reads 180°–45° (135°) and read the frequency on the frequency counter. This is $f_{-45°}$. Decrease the frequency of the signal generator until the phase meter reads 180° + 45 (225°) and read the frequency on the frequency counter. This is $f_{+45°}$.

To calculate the Q:

$$Q = \frac{f_O \text{ (center frequency)}}{f_{-45°} - f_{+45°} \text{ (BW)}}$$

Gain

To measure the gain, set the amplitude of the signal generator to 1V RMS (0 dBV) and set the frequency to the center frequency of the filter. Then read the output on the ac voltmeter. The output amplitude at highpass output is −10 dBV ±0.15 dB, which equals 0.316V ±0.006V RMS. The output amplitude at bandpass output is 0 dBV ±0.15 dB, which equals 1.000V ±0.017V RMS. The output amplitude at lowpass output is +10 dBV ±0.15 dB, which equals 3.16V ±0.06V RMS. The output at the amplifier output is 0 dBV ±0.1 dB, which equals 1V ±0.01V RMS.

DC Offset

The dc offset is measured with the DVM connected to the lowpass output by setting the input signal level to zero and reading the DVM.

PS Current

The power supply current is measured by connecting the DVM across a 10Ω resistor in the positive power supply lead with the input level set to zero. The DVM should read less than 45 mV.

applications information (con't)

DEFINITION OF TERMS

A_{MAX}	Maximum passband peak-to-peak ripple
A_{MIN}	Minimum stopband loss
f_Z	Frequency of jw axis pair
f_O	Frequency of complex pole pair
Q	Quality of pole
f_C	Passband edge
f_S	Stopband edge
A_{HP}	Gain from input to highpass output
A_{BP}	Gain from input to bandpass output
A_{LP}	Gain from input to lowpass output
A_{AMP}	Gain from input to output of amplifier
R_f	Pole frequency determining resistance
R_Z	Zero Frequency determining resistance
R_Q	Pole Quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a bandpass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a bandpass filter
BW	The bandwidth of a bandpass.filter
N	Order of the denominator of a transfer function

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G. J. Estep, *"The State Variable Active Filter Configuration Handbook,"* Second Edition, Agoura, Ca., 1974.

AF150 Universal Wideband Active Filter

General Description

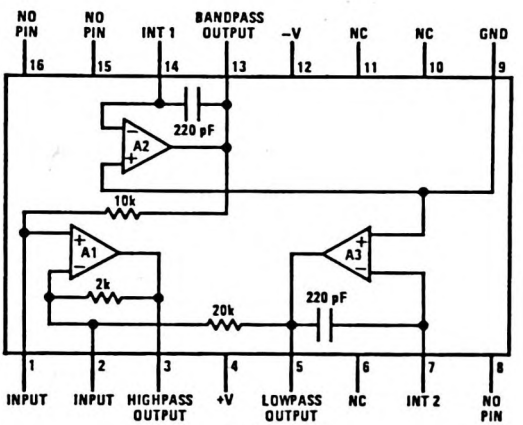
The AF150 wide band active filter is a general second order lumped RC network. Only four external resistors are required to program the AF150 for specific second order functions. Low pass, high pass and band pass functions are available simultaneously at separate outputs. Notch and all pass functions can be formed by summing the outputs with an external amplifier. Higher order filters are realized by cascading AF150 active filters with appropriate programming resistors.

Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be formed.

Features

- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate low pass, high pass, band pass outputs
- Inputs may be differential, inverting or non-inverting
- All pass and notch outputs may be formed
- Operates to 100 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- High accuracy ±1% unadjusted
- Q frequency product 2×10^5

Connection Diagram



TOP VIEW

Order Number AF150HY
See NS Package HY13A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Specifications apply for $V_S = \pm 15V$, over −25°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Frequency Range	$f_c \times Q \leq 2 \times 10^5$	100k			Hz
	Q Range	$f_c \times Q \leq 2 \times 10^5$	500			Hz/Hz
	f_o Accuracy					
	AF150-1C	$f_c \times Q \leq 5 \times 10^4$, $T_A = 25°C$			±2.5	%
	AF150-2C	$f_c \times Q \leq 5 \times 10^4$, $T_A = 25°C$			±1.0	%
$\Delta f_o/\Delta T$	f_o Temperature Coefficient			±50	±150	ppm/°C
	Q Accuracy	$f_c \times Q \leq 5 \times 10^4$, $T_A = 25°C$			±7.5	%
$\Delta Q/\Delta T$	Q Temperature Coefficient			±300	±750	ppm/°C
PSRR	Power Supply Rejection Ratio		80	100		dB
CMRR	Common-Mode Rejection		80	100		dB
I_{os}	Input Offset Current	$T_j = 25°C$		3	50	pA
I_B	Input Bias Current	$T_j = 25°C$		30	200	pA
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	±12		V
I_s	Power Supply Current	$V_S = \pm 15V$, $T_A = 25°C$		15	30	mA

Note 1: Any of the amplifier's outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum package power dissipation will be exceeded.

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF150 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input.

By adding external resistors the circuit can be used to generate the second order transfer function:

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

Applications Information (Continued)

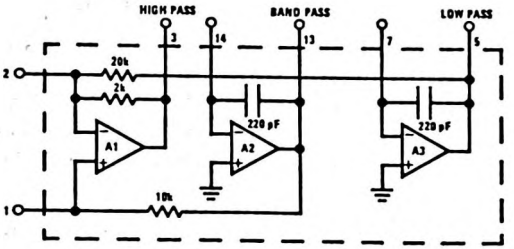


FIGURE 1. AF150 Schematic

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(low pass)}$$

Using an external op amp and the proper input and output connections, the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(notch)}$$

In the all pass transfer function $a_3 = 1$, $a_2 = -\omega_o/Q$ and $a_1 = \omega_o^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(all pass)}$$

The relationships between the generalized coefficients and the external resistors will be found in the appendix. It is not, however, necessary to use these theoretical, if not "messy", equations to solve for the proper external resistor values. In general, it is assumed that the user has knowledge of the frequency and Q of the specific filter he is designing. For higher order filters of various types, the reader is directed to any of the available texts on filters (see bibliography) for information and tables concerning the location of the poles and zeros. Once the specifics of the filter are found from the tables, it is simply a matter of cascading the sections with proper attention to some general guidelines which are included later in the application section.

The following discussion gives a step-by-step procedure for designing filters with several examples given for clarity.

FREQUENCY TUNING

Two equal value frequency setting resistors are required for frequencies above 1 kHz. For lower frequencies, T tuning or the addition of external capacitors is required. Using external capacitors allows the user to go as low in frequency as he desires. T tuning and external capacitors can be used together.

Two resistor tuning for 1 kHz to 100 kHz

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \quad (1)$$

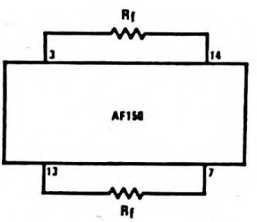
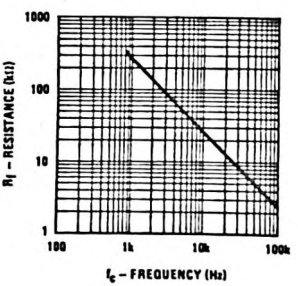


FIGURE 2. Resistive Tuning

GRAPH A. Resistive Tuning



Applications Information (Continued)

T resistive tuning for $f_o < 1$ kHz

$$R_S = \frac{R_T^2}{R_f - 2R_T} \quad (2)$$

R_f from equation 1.

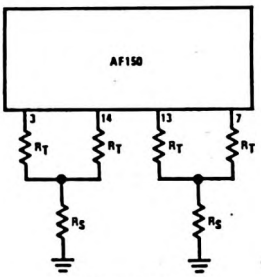
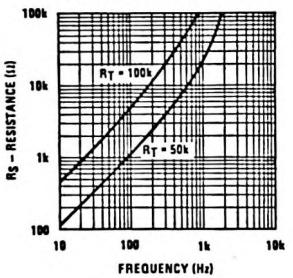


FIGURE 3. T Tuning

GRAPH B. T Tuning



If external capacitors are used for $f_o < 1$ kHz, then equation 3 should be used.

$$R_f = \frac{0.05033}{f_o\,(C + 220 \times 10^{-12})}\ \Omega \quad (3)$$

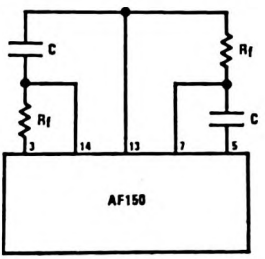


FIGURE 4. Low Frequency RC Tuning

Q DETERMINATION

Setting the Q requires one resistor from either pin 1 or pin 2 to ground. The value of the Q setting resistor depends on the input connection and input resistance as well as the value of the Q. The Q will be inversely proportional to the resistance from pin 1 to ground and directly proportional to resistance from pin 2 to ground.

NON-INVERTING CONNECTION*

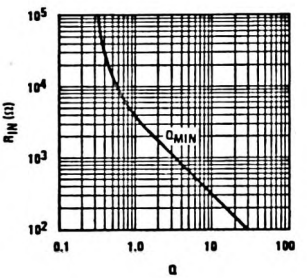
To determine the Q resistor, choose a value of input resistor, R_{IN}, *(Figures 5 and 6)* and calculate Q_{MIN} (graph C).

$$Q_{MIN} = \frac{1 + \frac{10^4}{R_{IN}}}{3.48}$$

If the Q required in the circuit is greater than Q_{MIN}, use the circuit configuration shown in *Figure 5* and equation 4 to calculate R_Q, the Q resistor. If the Q of the circuit is less than Q_{MIN}, use the circuit configuration shown in *Figure 6* and equation 5.

*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

GRAPH C. Q_{MIN}, Non-Inverting Input



Applications Information (Continued)

For $Q > Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} \ \Omega \qquad (4)$$

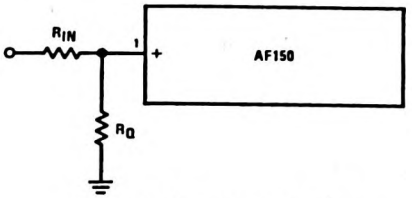
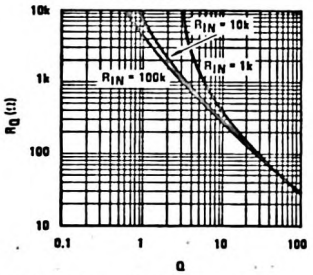


FIGURE 5. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

GRAPH D. R_Q for $Q > Q_{MIN}$, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{2 \times 10^3}{\left(1 + \frac{10^4}{R_{IN}}\right)} \ \Omega \qquad (5)$$
$$0.3162 \ \frac{}{Q} - 1.1$$

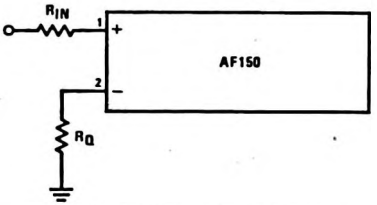
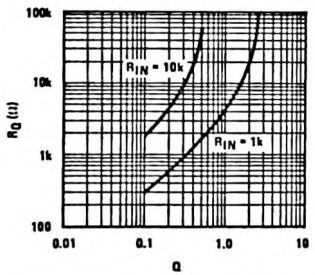


FIGURE 6. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. R_Q for $Q < Q_{MIN}$, Non-Inverting Input



INVERTING CONNECTION*

For any Q in inverting mode:

$$R_Q = \frac{10^4}{3.16Q\left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1} \ \Omega \qquad (6)$$

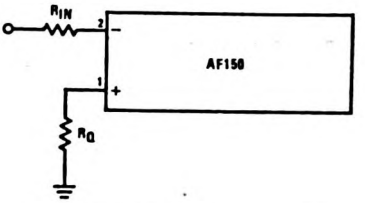
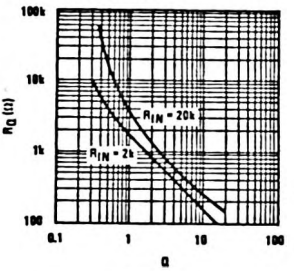


FIGURE 7. Q Tuning, Inverting Input

GRAPH F. Q Tuning, Inverting Input

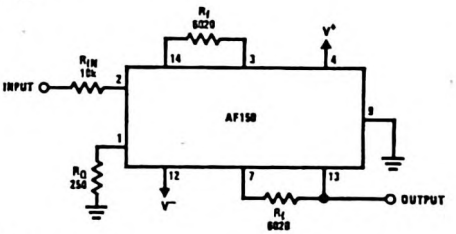


*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

DESIGN EXAMPLE

Non-Inverting Band Pass Filter

Center frequency 38 kHz = f_o, 10 Hz/Hz = Q, 10k = R_{IN}.



Using equation 1

$$R_f = \frac{228.8 \times 10^6}{f_o} \ \Omega$$

$$R_f = \frac{228.8 \times 10^6}{38 \times 10^3} = 6020\Omega$$

Applications Information (Continued)

Using equation 6

$$R_Q = \frac{10^4}{3.16Q\left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1}\ \Omega$$

$$R_Q = 250\Omega$$

From equation 33, the center frequency gain is found to be 6.3 V/V (16 dB). If the center frequency gain is to be adjusted, equation 33 can be solved for R_Q in terms of R_{IN} and this substituted into equation 6 to find the required R_{IN} and R_Q.

NOTCH FILTERS

Notches can be generated by two simple methods: using RC input *(Figure 8)* or low pass/high pass summing *(Figure 9)*. The RC input method requires adding a capacitor to pin 14 and a resistor connects to pin 7. The summing method requires two resistors connected to the low pass and high pass output.

The difference between the two possible methods of generating a notch is that the capacitor connection requires a high quality precision capacitor and the gain of the circuit is difficult to adjust because the gain and zero location are both dependent on C_Z and R_Z. The amplifier summing method requires 3 precision resistors and an external operational amplifier. However, the gain can be adjusted independent of the notch frequency.

For input RC notch tuning:

$$R_Z = \frac{C_Z R_f \times 10^{12}}{220}\left(\frac{f_o}{f_z}\right)^2\ \Omega \qquad (7)$$

f_z = frequency of notch (zero location)

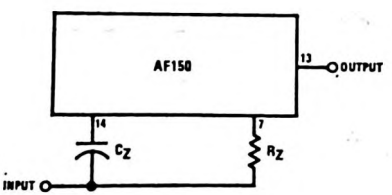
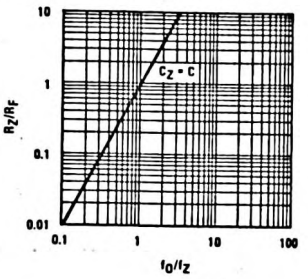


FIGURE 8. Input RC Notch

GRAPH G. Input RC Notch



For the low pass/high pass summing technique,

$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} \qquad (8)$$

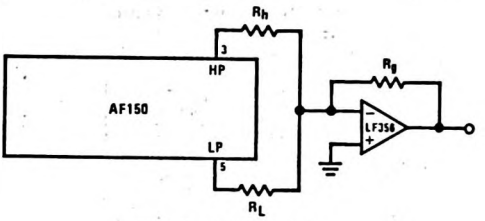
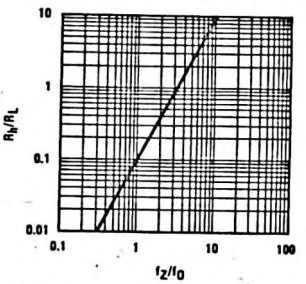


FIGURE 9. Output Notch

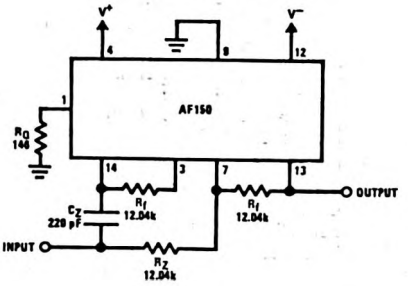
GRAPH H. Output Notch



DESIGN EXAMPLE

19 kHz notch using RC input.

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q



Applications Information

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega$$

$R_f = 12{,}040\Omega$

Using equation 4 with $R_{IN} = \infty$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega$$

$R_Q = 146\Omega$

Using equation 7:

$$R_Z = \left(\frac{C_Z R_F \times 10^{12}}{220}\right)\left(\frac{f_o}{f_z}\right)^2\ \Omega$$

$R_Z = 12{,}040\Omega$

DESIGN EXAMPLE

19 kHz notch using low pass/high pass summing

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega$$

$R_f = 12{,}040\Omega$

Using equation 4, choose $R_{IN} = 10\ k\Omega$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega$$

$R_Q = 148\Omega$

Using equation 8:

$$R_h = \left(\frac{f_Z}{f_o}\right)^2 \frac{R_L}{10}$$

Choose $R_L = 20k$, then $R_h = 2k$

TRIALS, TRIBULATIONS AND TRICKS

Certainly, there is no substitute for experience when applying active filters, working with op amps or riding a bicycle. However, the following section will discuss some of the finer points in more detail, and hopefully alleviate some of the fears and problems that might be encountered.

TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF150 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass (pin 13) output.

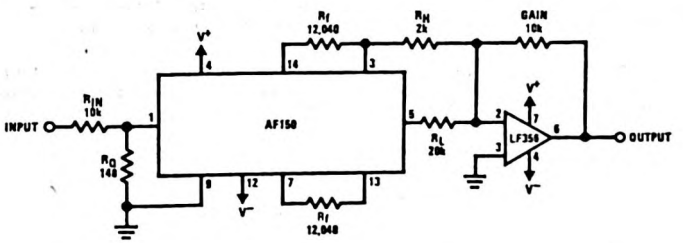
Before any tuning is attempted the low pass (pin 5) output should be checked to see that the output is not clipping. At the center frequency of the section the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the resistance between pin 1 or pin 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since



Applications Information (Continued)

the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

where f_o = center frequency

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output pin 5.

Adjust the resistance between pins 13 and 7 until the phase shift between input and band pass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

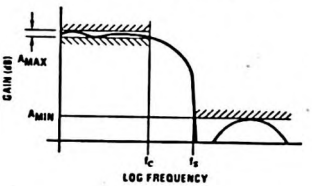
Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

FILTER DESIGN

Since most filter tables are in terms of a normalized low pass prototype, the filter to be designed is usually reduced to a low pass prototype. After the low pass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. The low pass amplitude response which can be defined by four quantities, defined below:

Low Pass Response



A_{MAX} = the maximum peak-to-peak ripple in the pass band

A_{MIN} = the minimum attenuation in the stop band

f_c = the pass band cutoff frequency

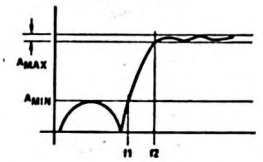
f_s = the stop band start frequency

By defining these four quantities for the low pass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the high pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but $f_c = 1/f_2$ and $f_s = 1/f_1$.

Applications Information (Continued)

High Pass Response



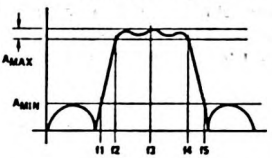
To obtain the band pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but:

$$f_c = 1 \qquad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$ i.e., geometric symmetry

$f_5 - f_1 = A_{MIN}$ bandwidth
$f_4 - f_2$ = Ripple bandwidth

Band Pass Response

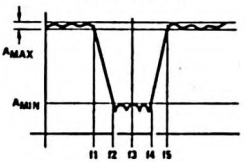


To obtain the notch from the low pass filter tables, A_{MAX} and A_{MIN} are the same as the low pass case and

$$f_c = 1, \quad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$

Notch Response



Normalized Low Pass Transformed to Un-Normalized Low Pass

The normalized low pass filter has the pass band edge normalized to unity. The un-normalized low pass filter instead has the pass band edge at f_c. The normalized and un-normalized low pass filters are related by the transformation $s = s\omega_c$. This transforms the normalized pass band edge $s = j$ to the un-normalized pass band edge $s = j\omega_c$.

Normalized Low Pass Transformed to Un-Normalized High Pass

The transformation that can be used for low pass to high pass is $S = \omega_c/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized low pass $1/(S^2 + S/Q + 1)$ transforms to the un-normalized high pass:

$$\frac{s^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$$

Normalized Low Pass Transformed to Un-Normalized Band Pass

The transformation that can be used for low pass to band pass is:

$$S = \frac{s^2 + \omega_o^2}{BW \cdot s}$$

where ω_o^2 is the center frequency of the desired band pass filter and BW is the ripple bandwidth.

Normalized Low Pass Transformed to Un-Normalized Band Stop (Or Notch)

The bandstop filter has a reciprocal response to a band pass filter. Therefore, a bandstop filter can be obtained by first transforming the low pass prototype to a high pass and then performing the band pass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases, it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Chebychev, Elliptic and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

The Chebychev function is a min/max approximation in the pass band. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the pass band. The Chebychev approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the pass band and stop band and have a steeper transition region than the Butterworth or the Chebychev.

For a specific low pass filter three quantities can be used to determine the degree of the transfer function: the maximum pass band ripple, the minimum stop band attenuation, and the transition ratio ($tr = \omega_s/\omega_c$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for

Applications Information (Continued)

the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers", Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs", John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis", McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design", McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Low pass, high pass, band pass, notch, all pass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

First Order	Second Order	
$\frac{K}{s+\omega_r}$	$\frac{K}{s^2+\frac{\omega_o}{Q}s+\omega_o{}^2}$	(low pass)
$\frac{Ks}{s+\omega_r}$	$\frac{Ks^2}{s^2+\frac{\omega_o}{Q}s+\omega_o{}^2}$	(high pass)
	$\frac{Ks}{s^2+\frac{\omega_o}{Q}s+\omega_o{}^2}$	(band pass)
	$\frac{K(s^2+\omega_z{}^2)}{s^2+\frac{\omega_o}{Q}s+\omega_o{}^2}$	(notch)
	$\frac{s^2-\frac{\omega_o}{Q}s+\omega_o{}^2}{s^2+\frac{\omega_o}{Q}s+\omega_o{}^2}$	(all pass)

Each of the second order functions is realizable by using an AF150 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

The primary concern in cascading second order stages is to minimize the difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

1. The highest Q pole pair should be paired with the zero pair closest in frequency.
2. If high pass and low pass stages are cascaded, the low pass sections should be the higher frequency and high pass sections the lower frequency.
3. In cascaded filters of more than two sections, the first section should be the section with Q closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.

DESIGN EXAMPLES OF CASCADE CONNECTIONS

Example 1.

Consider a 4th order Butterworth low pass filter with a 10 kHz cutoff (−3 dB) frequency and input impedance $\geq 30\ k\Omega$.

From tables, the normalized filter parameters are:

F1 = 1.0 Q1 = 0.541
F2 = 1.0 Q2 = 1.306

Thus, relative to the design required

F1 = (1.0)(10 kHz) = 10 kHz
F2 = (1.0)(10 kHz) = 10 kHz

Section 1

F = 10 kHz, Q = 1.306

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \qquad \text{(Using equation 1)}$$

$R_f = 22{,}880\Omega$

Select input resistor 31.6 kΩ

$$Q_{MIN} = \frac{1+\frac{10^4}{R_{IN}}}{3.48}$$

$Q_{MIN} = 0.378$

Applications Information (Continued)

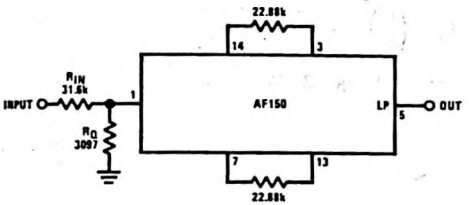
Thus, $Q > Q_{MIN}$

Therefore:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 3097\Omega$

First Stage



Section 2

$f_o = 10k$, $Q = 0.541$

Since f_o is the same as for the first section:

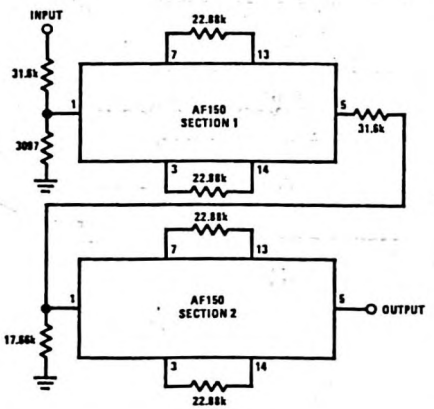
$R_f = 22.88\ k\Omega$

Select $R_{IN} = 31.6\ k\Omega$

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 17{,}661\Omega$

Complete Filter, Example 1



Example 2.

Consider the design of a low pass filter with the following performance:

$f_c = 10$ kHz
$f_s = 11$ kHz
$A_{MAX} = 1$ dB
$A_{MIN} = 40$ dB

It is found that a 6th order elliptic filter will satisfy the above requirements. The parameters of the design are:

STAGE	f_o (kHz)	Q	f_z (kHz)
1	5.16	0.82	29.71
2	8.83	3.72	13.09
3	10.0	20.89	11.15

Stage 1

a) From equation 1, R_F is found to be 44.34k
b) From equation 4, R_Q is found to be 11.72k, assuming R_{IN} (arbitrary) is 10 kΩ.

To create the transmission zero, f_z, at 29.71 kHz, use equation 8.

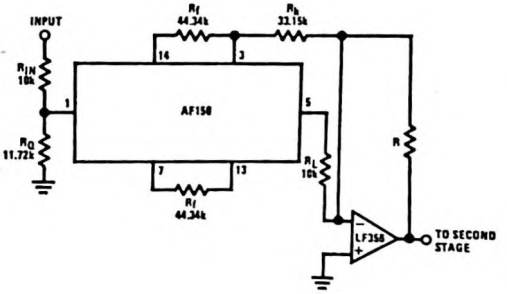
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10}, \text{ or } R_h = \left(\frac{29.71}{5.16}\right)^2 \frac{R_L}{10}$$

Thus,

$R_h = 3.315\ R_L$

If R_L is arbitrarily chosen as 10 kΩ, R_h = 33.15k.

Thus, the design of the first stage is:



where the feedback resistor, R, around the external op amp may be used to adjust the gain.

Applications Information (Continued)

Stage 2

The second stage design follows exactly the same procedure as the first stage design. The results are:

a) From equation 1, $R_f = 25.91k$
b) From equation 4, $R_Q = 913.6\Omega$, again assuming R_{IN} is arbitrarily 10k.

c) $R_h = \left(\frac{13.09}{8.83}\right)^2 \frac{R_L}{10}$ or $R_h = 0.22\ R_L$

Selecting $R_L = 10k$, then $R_h = 2.2k$, the second stage design is shown below.

Stage 3

The third stage design, again, is identical to the first 2 stages and the results are (for $R_{IN} = 10k$):

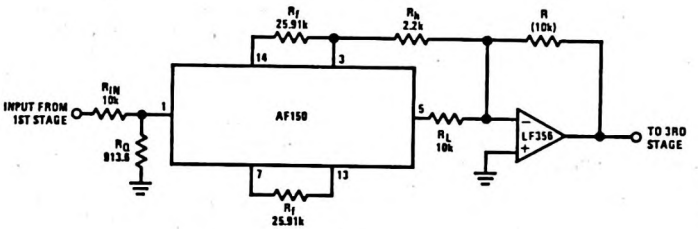
$$R_f = \frac{228.8 \times 10^6}{f_o} = 22.88k$$

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} = 141.4\Omega$$

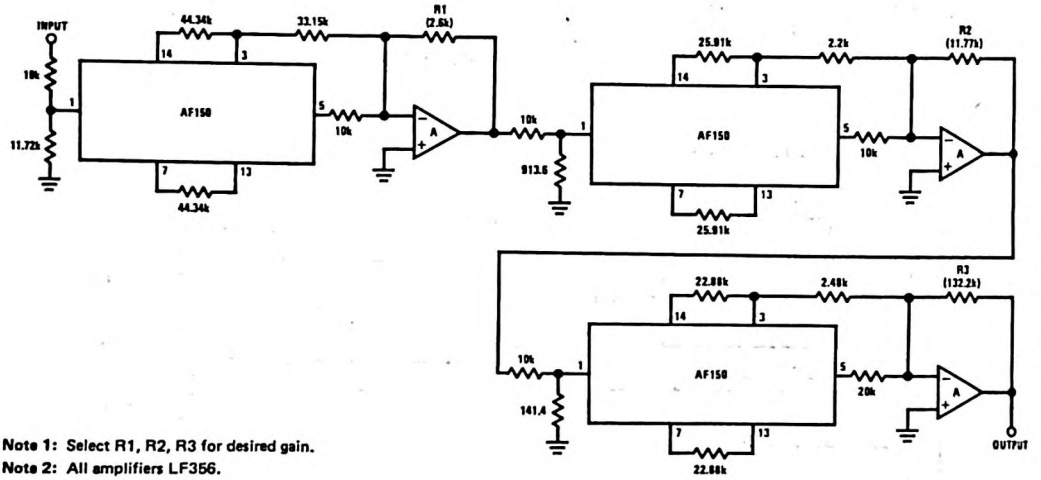
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} = \left(\frac{11.5}{10}\right)^2 \frac{R_L}{10} \qquad R_h = 0.124\ R_L$$

Let $R_L = 20k$, $R_h = 2.48k$

Second Stage



Filter for Example 2



Note 1: Select R1, R2, R3 for desired gain.
Note 2: All amplifiers LF356.

Applications Information (Continued)

From equation 13, the DC gain of the first section is

$$A_{V1} = \frac{11}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}$$

$$A_{V1} = \frac{11}{1 + \frac{10^4}{10^4} + \frac{10^4}{11.72 \times 10^3}} = 3.86\ V/V$$

Similarly, the DC gain of the second and third sections are:

$A_{V2} = 0.850$
$A_{V3} = 0.151$

Therefore, the overall DC gain is 0.495 and can be adjusted by selecting R1 with respect to 10k, R2 with respect to 10k or R3 with respect to 20k.

For convenience, a standard resistor value table is given below.

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ, 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.000	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.002	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.005	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.007	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.110	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.113	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.115	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.118	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

Appendix (See footnote)

The specific transfer functions for some of the most useful circuit configurations using the AF150 are illustrated in *Figures 10 through 16*. Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation. Q_{MIN} is a function of R_{IN} (see graph C).

a) Non-inverting input *(Figure 10)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\frac{1.1}{1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(high pass)} \quad (9)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\omega_1 \left[\frac{1.1}{1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(band pass)} \quad (10)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\frac{1.1}{1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(low pass)} \quad (11)$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\frac{10^4}{R_Q}+\frac{10^4}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2 \quad (12)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}\right)} \text{(DC Gain)} \quad (13)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to \infty} = \frac{1.1}{\left(1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}\right)} \text{(High Freq. Gain)} \quad (14)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\frac{10^4}{R_Q}+\frac{10^4}{R_{IN}}\right)}{\left(1+\frac{R_{IN}}{10^4}+\frac{R_{IN}}{R_Q}\right)} \text{(Center Freq. Gain)} \quad (15)$$

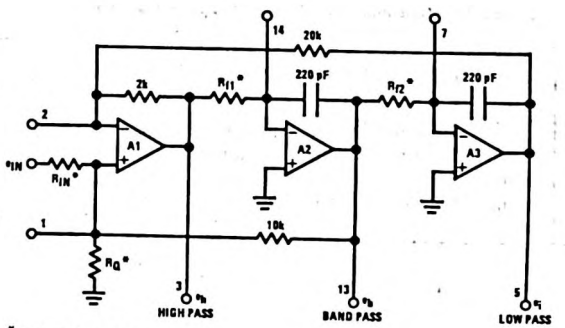
$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220} \qquad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$, (see footnote)

$$Q = \left(\frac{1+\frac{10^4}{R_{IN}}+\frac{10^4}{R_Q}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)} \quad (16)$$

$$R_Q = \frac{10^4}{\left(\frac{1.1Q}{\sqrt{0.1\frac{\omega_2}{\omega_1}}}\right) - 1 - \frac{10^4}{R_{IN}}} \quad (17)$$



*External components

FIGURE 10. Non-Inverting Input ($Q > Q_{MIN}$)

FOOTNOTE:

It should be noted that in the text of this paper, ω_1 and ω_2 have been assumed equal, and hence $R_{f1} = R_{f2}$. No generality is lost in this assumption and it facilitates the design. However, for completeness, the equations given are exact.

Appendix (Continued)

b) Non-inverting input *(Figure 11)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (high pass)} \quad (18)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (band pass)} \quad (19)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (low pass)} \quad (20)$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{10^4}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2 \quad (21)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{0.1\left(1 + \frac{R_{IN}}{10^4}\right)} \quad (22)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}} \quad (23)$$

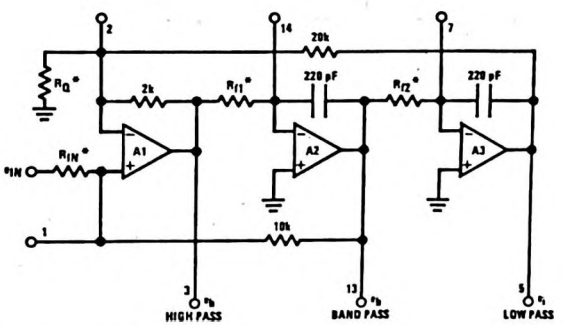
$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_o} = -\frac{1 + \frac{10^4}{R_{IN}}}{1 + \frac{R_{IN}}{10^4}} \quad (24)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \; \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \frac{10^4}{R_{IN}}}{1.1 + \frac{2 \times 10^3}{R_Q}}\right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (25)$$

$$R_Q = \frac{2 \times 10^7}{\left(1 + \frac{10^4}{R_{IN}}\right)\left(\frac{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}{Q}\right) - 1.1} \quad (26)$$



*External components

FIGURE 11. Non-Inverting Input ($Q < Q_{MIN}$)

Appendix (Continued)

c) Inverting input *(Figure 12)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(high pass)} \qquad (27)$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(band pass)} \qquad (28)$$

$$\frac{e_\ell}{e_{IN}} = \frac{-\omega_1\omega_2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(low pass)} \qquad (29)$$

$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220},\quad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1 + \frac{2\times10^3}{R_{IN}}}{1+\frac{10^4}{R_Q}}\right] + 0.1\,\omega_1\,\omega_2 \qquad (30)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{2\times10^4}{R_{IN}} \quad \text{(low pass) (DC gain)} \qquad (31)$$

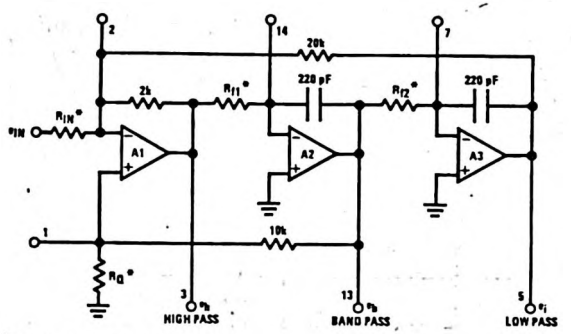
$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = -\frac{2\times10^3}{R_{IN}} \quad \text{(high pass) (high freq. gain)} \qquad (32)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = \frac{\frac{2\times10^3}{R_{IN}}\left(1+\frac{10^4}{R_Q}\right)}{1.1+\frac{2\times10^3}{R_{IN}}} \quad \text{(band pass) (center freq. gain)} \qquad (33)$$

$$\omega_0 = \sqrt{0.1\,\omega_1\,\omega_2}$$

$$Q = \left[\frac{1+\frac{10^4}{R_Q}}{1.1+\frac{10^4}{R_{IN}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \qquad (34)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1+\frac{2\times10^3}{R_{IN}}\right)-1} \qquad (35)$$



*External components

FIGURE 12. Inverting Input, Any Q

Appendix (Continued)

dd) Differential input *(Figure 13)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(high pass)} \quad (36)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(band pass)} \quad (37)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left(\frac{2\times10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(low pass)} \quad (38)$$

$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$$\Delta\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\frac{2\times10^3}{R_{IN2}}}{1+\frac{10^4}{R_Q}+\frac{10^4}{R_{IN1}}}\right] + 0.1\,\omega_1\omega_2 \quad (39)$$

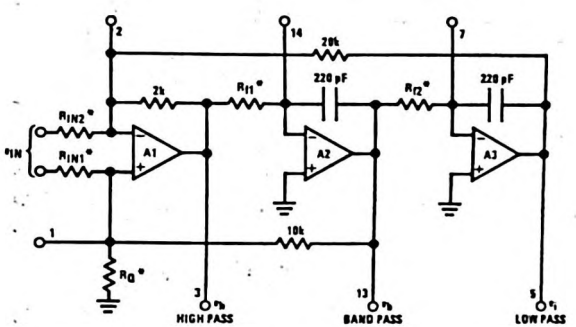
$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{2\times10^4}{R_{IN2}} \text{ (DC gain) (low pass)} \quad (40)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{2\times10^3}{R_{IN2}} \text{ (high freq. gain) (high pass)} \quad (41)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = \frac{\frac{2\times10^3}{R_{IN2}}\left(1+\frac{10^4}{R_{IN1}}+\frac{10^4}{R_Q}\right)}{\left(1.1+\frac{2\times10^3}{R_{IN2}}\right)} \text{ (center freq. gain) (band pass)} \quad (42)$$

$$Q = \left[\frac{1+\frac{10^4}{R_Q}+\frac{10^4}{R_{IN1}}}{1.1+\frac{2\times10^3}{R_{IN2}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (43)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1+\frac{2\times10^3}{R_{IN2}}\right)-1-\frac{10^4}{R_{IN1}}} \quad (44)$$



*External components

FIGURE 13. Differential Input

Appendix (Continued)

e) Notch filter *(Figure 14)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_z^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2} \quad (45)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220},\ \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220},\ \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_z = \omega_0\sqrt{\frac{10\,R_h}{R_L}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_L} \quad \text{(DC gain)} \quad (46)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_h} \quad \text{(high freq. gain)} \quad (47)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_z} = 0 \quad (48)$$

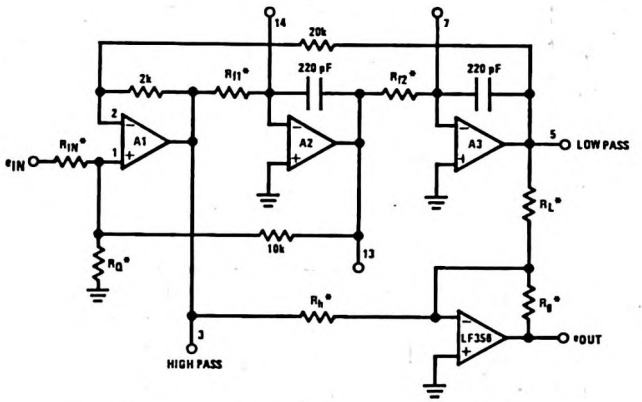


FIGURE 14. Notch Filter Using an External Amplifier

Appendix (Continued)

j) Input notch filter *(Figure 15)* transfer function equations are:

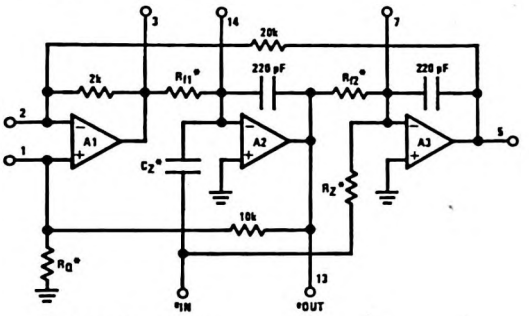
$$\frac{e_{IN}}{e_n} = -\frac{\frac{C_Z}{220 \times 10^{-12}}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,R_Q}{10^4 + R_Q}\right] + \omega_0{}^2} \quad (49)$$

$$\omega_Z = \omega_0\sqrt{\frac{R_{f2} \cdot 220 \times 10^{-12}}{R_Z C_Z}},\ \omega_0 = \sqrt{0.1\,\omega_1\omega_2} \quad (50)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220},\ \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = \frac{-R_{F2}}{R_Z} \quad (51)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{220 \times 10^{-12}} \quad (52)$$



*External components

FIGURE 15. Input Notch Filter Using 3 Amplifiers

g) All pass *(Figure 16)* transfer function equations are:

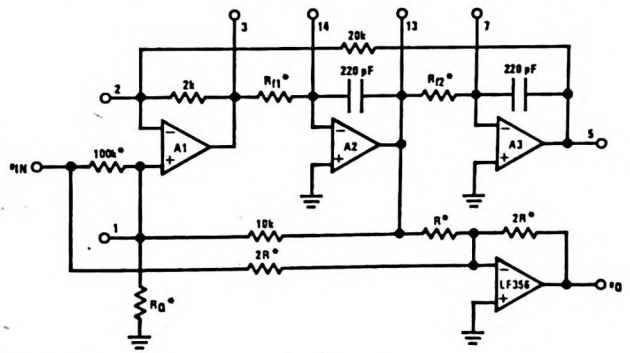
$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{R_Q}}\right] + \omega_o{}^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{R_Q}}\right] + \omega_0{}^2}\right] \quad (53)$$

$$Q = \left[\frac{2 + \frac{10^4}{R_Q}}{1.1}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (54)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220},\ \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at ω_0 is $\frac{2Q}{\omega_0}$ seconds



*External components

FIGURE 16. All Pass

Definition of Terms

A_{MAX}	Maximum pass band peak-to-peak ripple
A_{MIN}	Minimum stop band loss
f_z	Frequency of jw axis pole pair
f_o	Frequency of complex pole pair
Q	Quality of pole
f_c	Pass band edge
f_s	Stop band edge
R_f	Pole frequency determining resistance
R_z	Zero Frequency determining resistance
R_Q	Pole quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a band pass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a band pass filter

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AF151 Dual Universal Active Filter

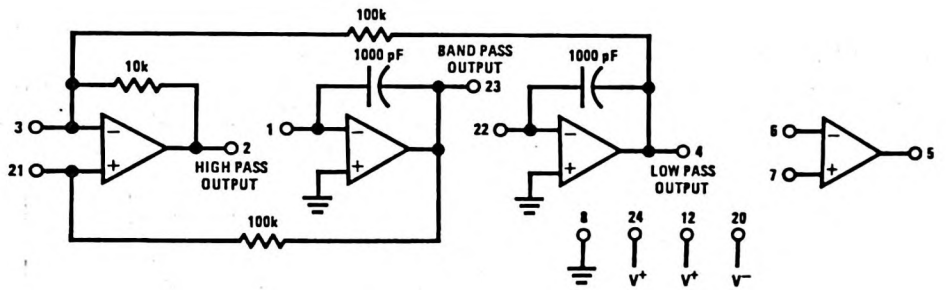
General Description

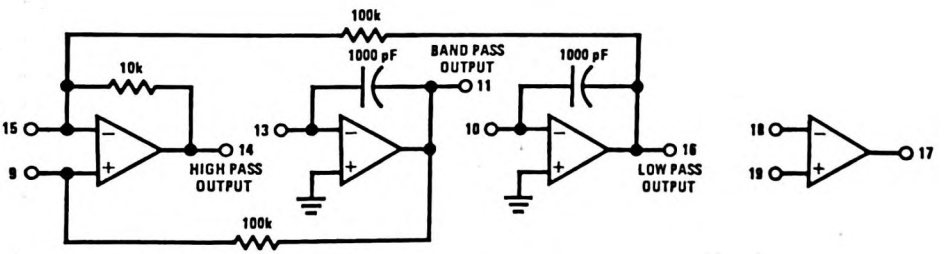
The AF151 consists of 2 general purpose state variable active filters in a single package. By using only 4 external resistors for each section, various second order functions may be formed. Low pass, high pass and band pass functions are available simultaneously at separate outputs. In addition, there are 2 uncommitted operational amplifiers which are available for buffering or for forming all pass and notch functions. Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be easily formed.

Features

- Independent Q, frequency and gain adjustment
- Very low sensitivity to external component variation
- Separate low pass, high pass and band pass outputs
- Operation to 10 kHz
- Q range to 500
- Wide power supply range—±5V to ±18V
- Accuracy—±1%
- Fourth order functions in one package

Circuit Diagrams





Order Number AF151HY
See NS Package HY24A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Complete Active Filter)

Specifications apply for V_S = ±15V and over −25°C to +85°C unless otherwise specified. (Specifications apply for each section).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_c \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_c \times Q \leq 50{,}000$			500	Hz/Hz
f_o Accuracy					
AF151-1C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±2.5	%
AF151-2C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±1.0	%
f_o Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	V_S = ±15V		2.5	4.5	mA

Electrical Characteristics (Internal Op Amp) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$, V_{OUT} = ±10V	25	160		V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±14		V
	R_L = 2 kΩ	±10	±13		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short-Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for V_S = ±15V, T_A = 25°C.

Applications Information

The AF151 consists of 2 identical filter sections and 2 uncommitted op amps. The op amps may be used for buffering inputs and outputs, summing amplifiers (for notch filter generation), adjusting gain through the filter sections, additional passive networks to create higher order filters, or simply used elsewhere in the user's system.

The design equations given apply to both sections; however, for clarity, only the pin designations for section 1 will be shown in the examples and discussion.

See the AF100 data sheet for additional information on this type of filter.

The design equations assume that the user has knowledge of the frequency and Q values for the particular design to be synthesized. If this is not the case, various references and texts are available to help the user in determining these parameters. A bibliography of recommended texts can also be found in the AF100 data sheet.

CIRCUIT DESCRIPTION AND OPERATION

A schematic of one section of the AF151 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system.

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer functions becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(low pass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) \quad \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(notch)}$$

In the all pass transfer function $a_1 = \omega_o^2$, $a_2 = -\omega_o/Q$ and $a_3 = 1$. The transfer function becomes:

$$T(s) \quad \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(all pass)}$$

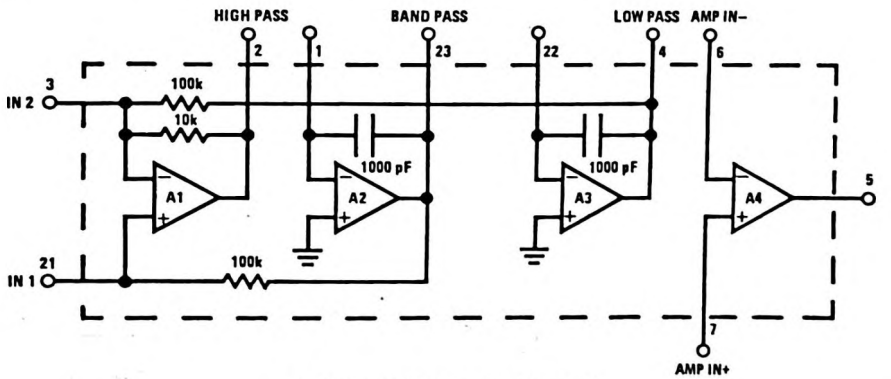


FIGURE 1. AF151 Schematic (Section 1)

Applications Information (Continued)

FREQUENCY CALCULATIONS

For operation above 200 Hz, the frequency of each section of the AF151 is set by 2 equal valued resistors. These resistors couple the output of the first op amp (pin 2) to the input of the second op amp (pin 1) and the output of the second op amp (pin 23) to the input of the third op amp (pin 22).

The value for R_f is given by:

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega \qquad (1)$$

For operation below 200 Hz, "T" tuning should be used as shown in *Figure 3*.

For this configuration,

$$R_S = \frac{R_T{}^2}{R_f - 2R_T} \qquad (2)$$

where R_T or R_S can be chosen arbitrarily, once R_f is found from equation 1.

Q CALCULATIONS

To set the Q of each section of the AF151, one resistor is required. The value of the Q setting resistor depends on the input connection (inverting or non-inverting) and the input resistance. Because the input resistance does affect the Q, it is often desirable to use one of the uncommitted op amps to provide a buffer between the signal source impedance and the input resistor used to set the Q.

To determine which connection is required for a particular Q, arbitrarily select a value of R_{IN} *(Figure 4)* and calculate Q_{MIN} according to equation 3.

$$Q_{MIN} = \frac{1 + \dfrac{10^5}{R_{IN}}}{3.48} \qquad (3)$$

If the Q required for the circuit is greater than Q_{MIN}, use equation 4 to calculate the value of R_Q and the connection shown in *Figure 4*.

$$R_Q = \frac{10^5}{3.48Q - 1 - \dfrac{10^5}{R_{IN}}} \qquad (4)$$

If the Q required for the circuit is less than Q_{MIN}, use equation 5 to calculate the value of R_Q and the connection shown in *Figure 5*.

$$R_Q = \frac{10^4}{\dfrac{0.3162}{Q}\left(1 + \dfrac{10^5}{R_{IN}}\right) - 1.1} \qquad (5)$$

Both connections shown in *Figures 4 and 5* are "non-inverting" relative to the phase relationship between the input signal and the low pass output.

For any Q, equation 6 may be used with the "inverting" connection shown in *Figure 6*.

$$R_Q = \frac{10^5}{3.16\,Q\left(1.1 + \dfrac{10^4}{R_{IN}}\right) - 1} \qquad (6)$$

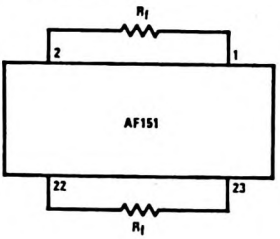


FIGURE 2. Frequency Tuning

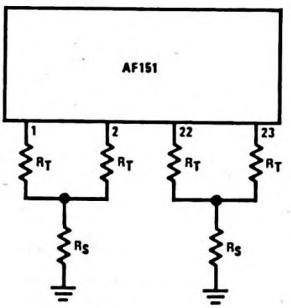


FIGURE 3. "T" Tuning for Low Frequency

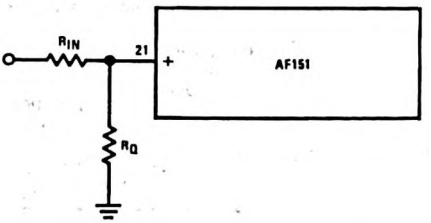


FIGURE 4. Connection for $Q > Q_{MIN}$

FIGURE 5. Connection for $Q < Q_{MIN}$

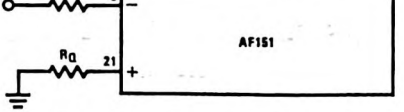


FIGURE 6. Connection for Any Q, Inverting

Applications Information (Continued)

NOTCH TUNING

When the low pass output and the high pass output are summed together, the result is a notch *(Figure 7)*.

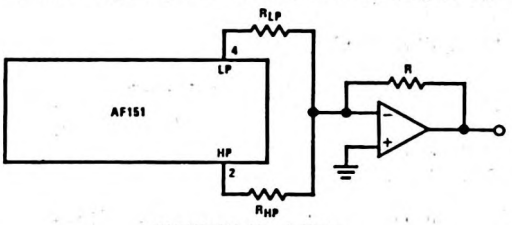


FIGURE 7. Notch Filter

The relationship between R_{LP}, R_{HP}, f_o and f_z, the location of the notch, is given by equation 7.

$$R_{HP} = \left(\frac{f_z}{f_o}\right)^2 \frac{R_{LP}}{10} \qquad (7)$$

Again, it is advantageous to use one of the uncommitted op amps to perform this summing function to prevent loading of this stage or the resistors R_{LP} and R_{HP} from effecting the Q of subsequent stages. Resistor R can be used to set the gain of the filter section.

GAIN CALCULATIONS

The following list of equations will be helpful in calculating the relationship between the external components and various important parameters. The following definitions are use:

- A_L – Gain from input to low pass output at DC
- A_H – Gain from input to high pass output at high frequency
- A_B – Gain from input to band pass output at center frequency

For *Figure 4*:

$$A_L = \frac{11}{\Delta}$$

$$A_H = \frac{1.1}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}$$

For *Figure 5:*

$$A_L = \frac{11 + \frac{10^5}{R_Q}}{\Delta}$$

$$A_H = \frac{1.1 + \frac{10^4}{R_Q}}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5}$$

For *Figure 6:*

$$A_L = -\frac{10^5}{R_{IN}}$$

$$A_H = -\frac{10^4}{R_{IN}}$$

$$A_B = \frac{\frac{10^5}{R_{IN}}\left(1 + \frac{10^5}{R_Q}\right)}{11 + \frac{10^5}{R_{IN}}}$$

For *Figure 7*:

At low frequency, when $f_o < f_z$, the gain to the output of the summing op amp is:

$$A_L = \frac{11\left(\frac{R}{R_{LP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At high frequency, when $f_o > f_z$, the gain to the output of the summing op amp is:

$$A_H = \frac{1.1\left(\frac{R}{R_{HP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At the notch, ideally the gain is zero (0).

TUNING TIPS

In applications where 2% to 3% accuracy is not sufficient to provide the required filter response, the AF151 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass output.

Before any tuning is attempted, the low pass output should be checked to see that the output is not clipping. At the center frequency of the section, the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs, the results obtained when tuning will be incorrect.

Applications Information (Continued)

Frequency Tuning

By adjusting resistor R_f, center frequency of a section can be adjusted. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the R_Q resistor. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will "see" to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

where f_o = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair, the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing).

In either case, the signal is connected to the input and the proper resistor is adjusted for a null at the output.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output.

Adjust the R_f resistor until the phase shift between input and band pass output is 180° or 0°, depending upon the connection.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning (Notch Tuning)

Set the oscillator output to the zero frequency and tune one of the summing resistors for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

DESIGN EXAMPLE

Assume 2 band pass filters are required to separate FSK data.

f1 = 800 Hz, Q = 40
f2 = 1000 Hz, Q = 50

The gain through each filter is to be 10 V/V (20 dB).

Since the design is similar for both sections, only the first section design will be shown for the example.

(a) From equation 1

$$R_f = \frac{50.33 \times 10^6}{f_o} = \frac{50.33 \times 10^6}{800}$$

$$\boxed{R_f = 62.9k}$$

(b) Checking Q_{MIN} from equation 3, arbitrarily let R_{IN} = 300k.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} = \frac{1 + \frac{10^5}{3 \times 10^5}}{3.48} = 0.383$$

Since the Q required for the design (Q = 40), is greater than Q_{MIN}, the circuit of *Figure 4* or *Figure 6* may be used. Arbitrarily we shall select the circuit of *Figure 4*.

(c) From equation 4, R_Q is found to be

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} = \frac{10^5}{(3.48)(40) - 1 - \frac{10^5}{3 \times 10^5}}$$

or $\boxed{R_Q = 725\Omega}$

(d) Calculate the center frequency gain for *Figure 4*.

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)} = \frac{-(1 + 137.9 + 0.333)}{(1 + 3.0 + 414)}$$

$$A_B = 0.333 \text{ V/V}$$

Since the gain at f_o is 0.333 V/V, a gain of 10 V/V can be obtained by using the uncommitted operational amplifier with a gain of 30.03 as shown in *Figure 8*.

Applications Information (Continued)

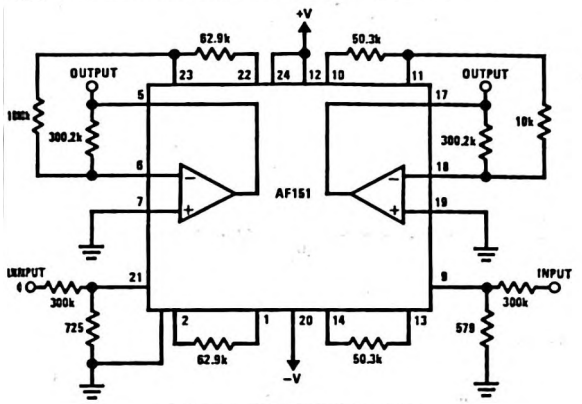


FIGURE 8. Dual Band Pass Filter

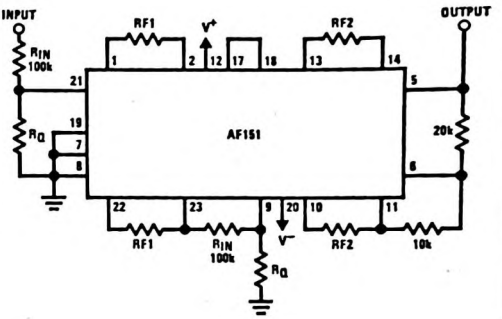


FIGURE 9. Telephone Multifrequency (MF) Band Pass Filter

FREQ	BW	f_c	f1	Q1 & Q2	f2	RF1	RF2	RQ
700	75	698.4	665.6	17	732.8	75.62k	68.68k	1.749k
900	75	898.7	865.8	21.8	932.9	58.13k	53.95k	1.354k
1100	75	1098.8	1065.7	26.7	1132.9	47.23k	44.43k	1.100k
1300	75	1298.9	1265.8	31.6	1332.9	39.76k	37.76k	926.2Ω
1500	75	1499.0	1465.8	36.4	1532.9	34.34k	32.83k	802.1Ω
1700	75	1699.1	1665.9	41.3	1733.0	30.21k	29.04k	705.6Ω

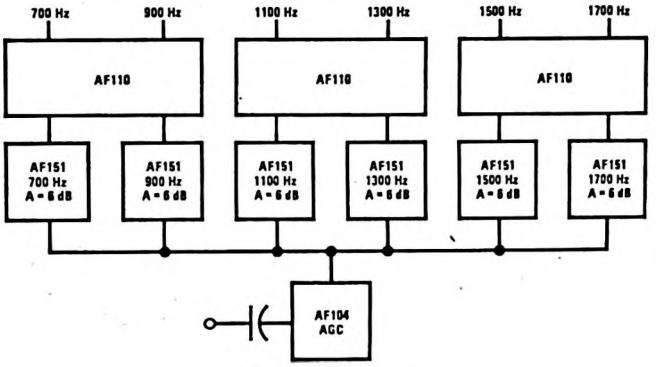
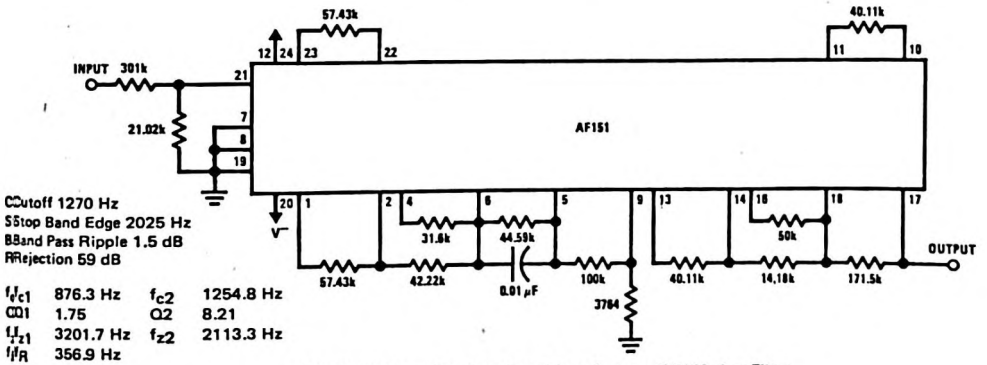


FIGURE 10. MF Tone Receiver

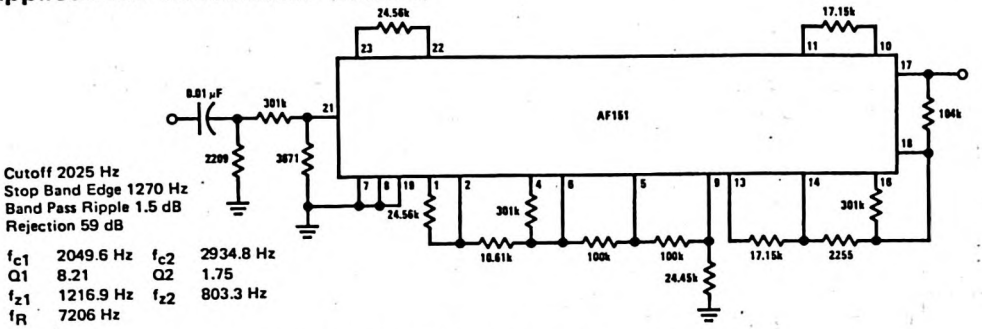


Cutoff 1270 Hz
Stop Band Edge 2025 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	876.3 Hz	f_{c2}	1254.8 Hz
Q1	1.75	Q2	8.21
f_{z1}	3201.7 Hz	f_{z2}	2113.3 Hz
f_R	356.9 Hz		

FIGURE 11. Low Pass Low Speed Asynchronous FSK Modem Filter

Applications Information (Continued)



Cutoff 2025 Hz
Stop Band Edge 1270 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	2049.6 Hz	f_{c2}	2934.8 Hz
Q1	8.21	Q2	1.75
f_{z1}	1216.9 Hz	f_{z2}	803.3 Hz
f_R	7206 Hz		

FIGURE 12. High Pass Low Speed Asynchronous FSK Modem Filter

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example,1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

Section 12

Successive Approximation Registers

12

National Semiconductor

DM2502, DM2503, DM2504 Successive Approximation Registers

Successive Approximation Registers

general description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

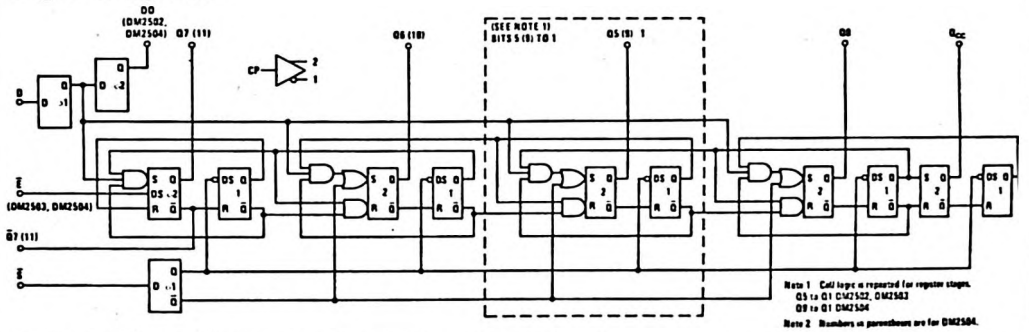
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

features

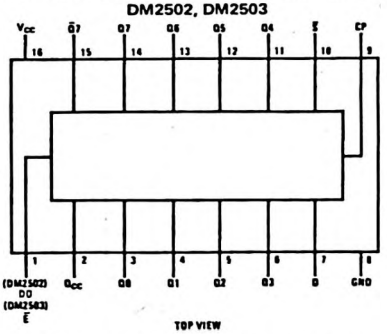
- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

logic diagram


(SEE NOTE 1)
BITS 5 (9) TO 1
Note 1 Cell logic is repeated for register stages.
Q5 to Q1 DM2522, DM2583
Q9 to Q1 DM2504
Note 2 Numbers in parentheses are for DM2504.

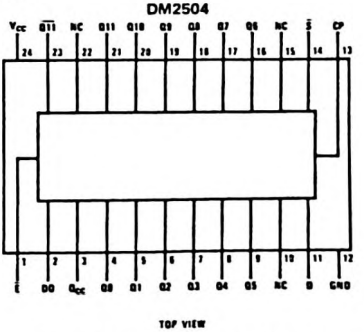
connection diagrams (Dual-In-Line and Flat Packages)

DM2502, DM2503



Order Number DM2502J, DM2502CJ, DM2503J or DM2503CJ
See NS Package J16A
Order Number DM2502CN or DM2503CN
See NS Package N16A
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

DM2504



Order Number DM2504F or DM2504CF
See NS Package F24A

Order Number DM2504J or DM2504CJ
See NS Package J24A

Order Number DM2504CN
See NS Package N24A

12

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503, DM2504	−55	+125	°C

electrical characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max				
CP Input	V_{IH} = 2.4V		6	40	μA
D, $\overline{E}$, $\overline{S}$ Inputs	V_{IH} = 2.4V		6	80	μA
All Inputs	V_{IH} = 5.5V			1.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max				
CP, $\overline{S}$ Inputs	V_{IL} = 0.4V		−1.0	−1.6	mA
D, $\overline{E}$ Inputs	V_{IL} = 0.4V		−1.0	−3.2	mA
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OH} = −0.48 mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max; V_{OUT} = 0.0V; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 9.6 mA		0.2	0.4	V
Supply Current (I_{CC})	V_{CC} = Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

application information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

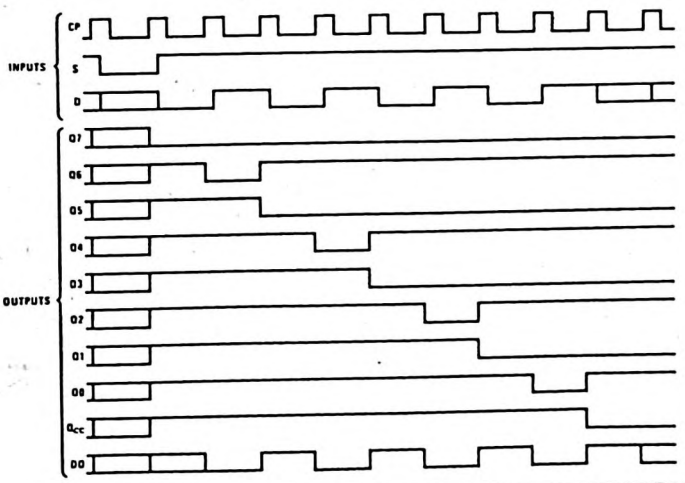
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

timing diagram

DM2502, DM2503



application information (con't)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

definition of terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q}$7 (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

truth table

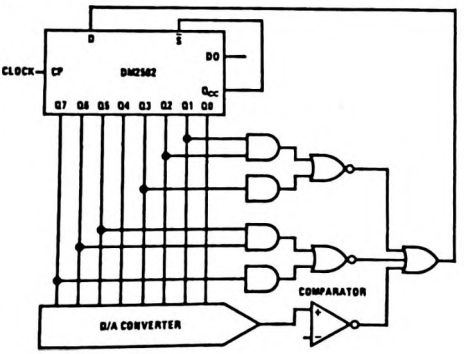
DM2502, DM2503

TIME	INPUTS			OUTPUTS[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	DO[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

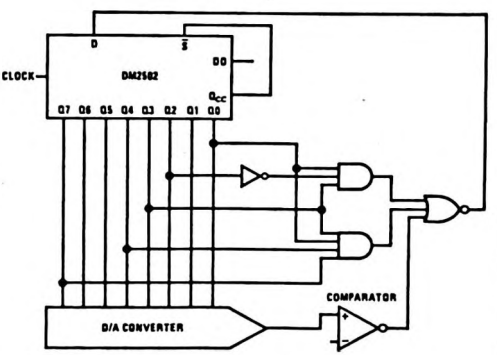
Note 1: Truth table for DM2504 is extended to include 12 outputs.
Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.
Note 3: Truth table for DM2503 does not include DO column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

typical applications



Active High

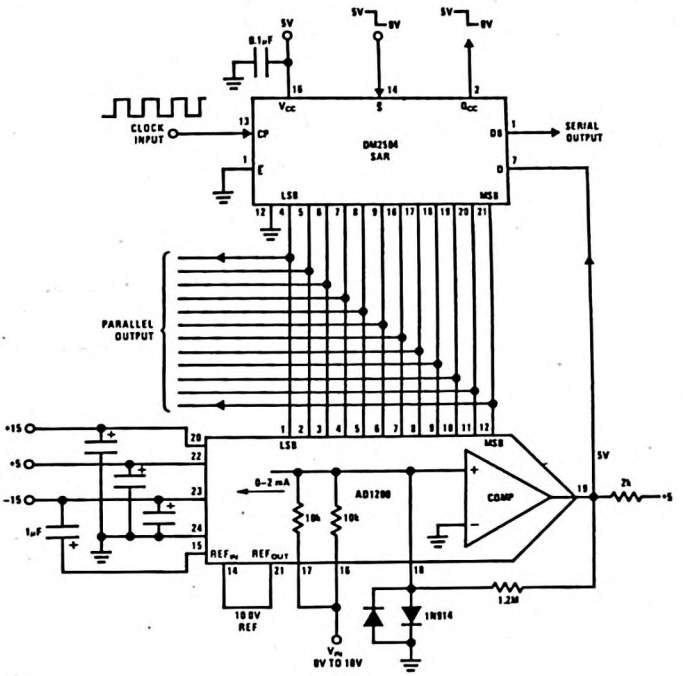


Active Low

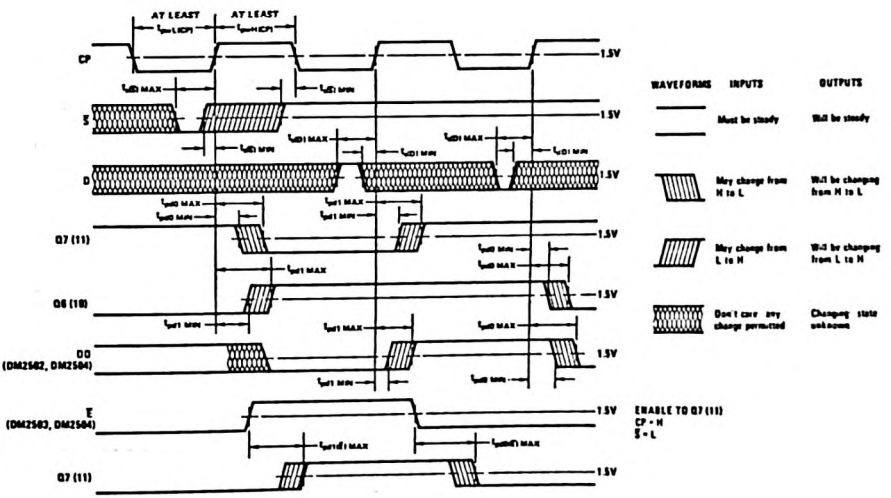
BCD Illegal Code Suppression

typical applications (con't)

High Speed 12-Bit A/D Converter



switching time waveforms



National Semiconductor

Successive Approximation Registers

MM54C905/MM74C905
12-Bit Successive Approximation Register

general description

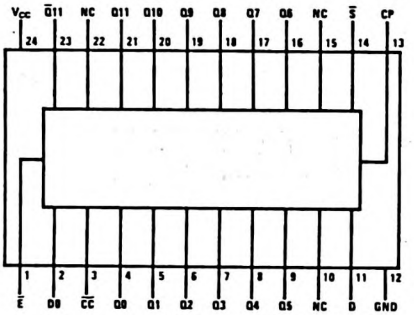
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

connection diagram

Dual-In-Line Package



Order Number MM54C905D or MM74C905D
See NS Package D24A

Order Number MM74C905N
See NS Package N24A

truth table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C905	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	V_{CC} = 4.5V			0.8	V
MM74C905	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C905	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C905	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Q11–Q0 Outputs					
R_{SOURCE}	V_{CC} = 10V ±5%, V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5%, V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

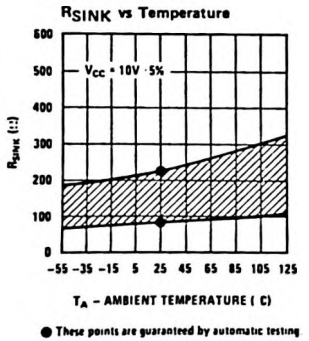
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

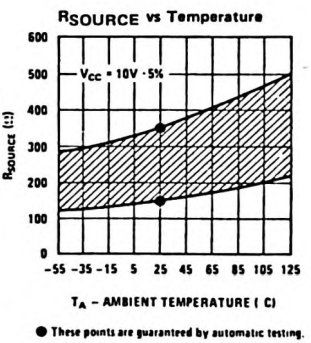
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

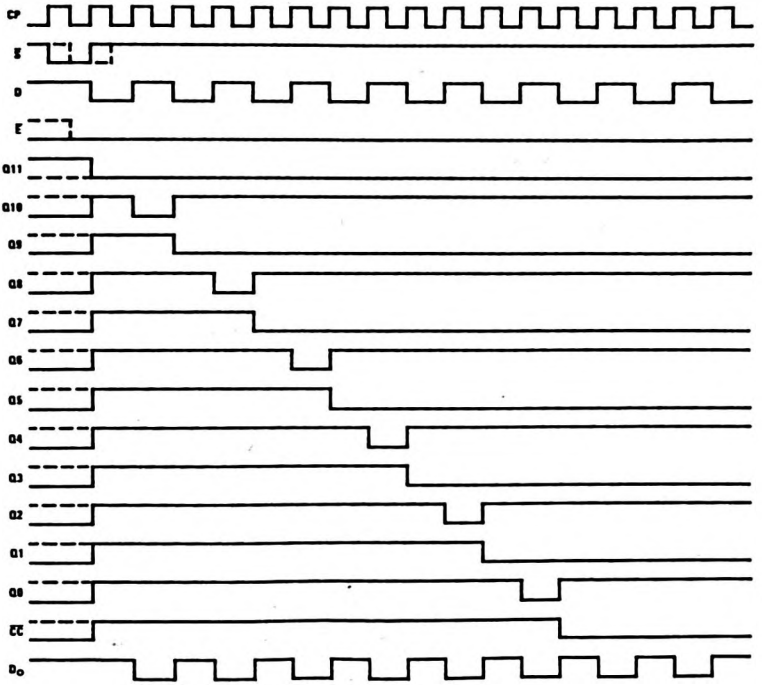
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

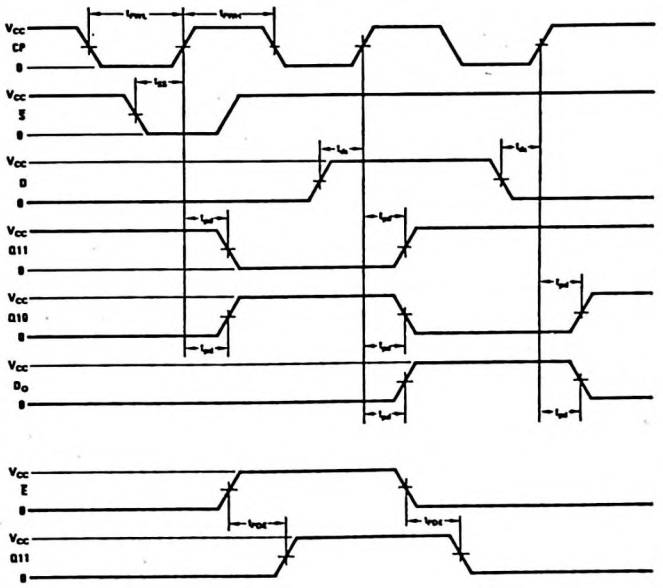




timing diagram



switching time waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

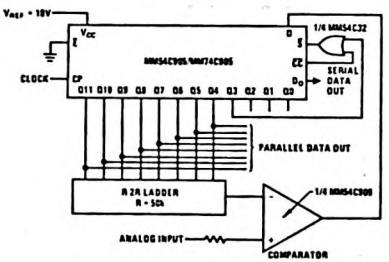
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

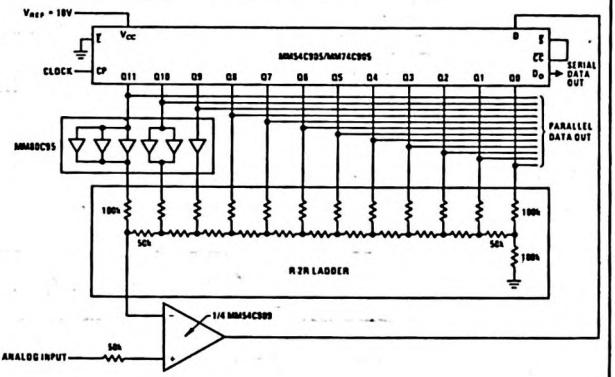
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

typical applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



definition of terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Section 13

Functional Blocks

13

LH0091 True rms to DC Converter

general description

The LH0091, rms to dc converter, generates a dc output equal to the rms value of any input per the transfer function:

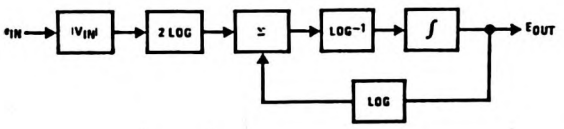
$$E_{OUT(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ±0.05% typ) for decade ranges i.e., 10 mV → 100 mV, 0.7V → 7V, etc.

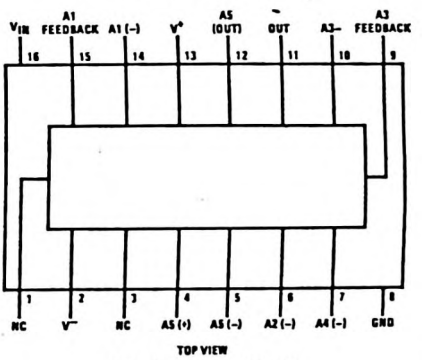
features

- Low cost
- True rms conversion
- 0.5% of reading accuracy untrimmed
- 0.05% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for V_S = ±15V
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range.

block and connection diagrams



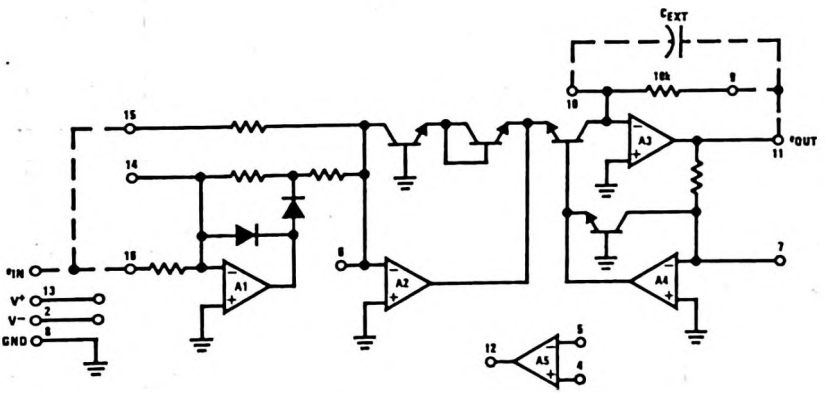
Dual-In-Line Package



TOP VIEW

Order Number LH0091HY
See NS Package HY16B or HY16C

simplified schematic



Note: Dotted lines denote external connections.

absolute maximum ratings

Supply Voltage		±22V
Input Voltage		±15V peak
Output Short Circuit Duration		Continuous
Operating Temperature Range	T_{MIN}	T_{MAX}
LH0091	−55°C	125°C
LH0091C	−25°C	85°C
Storage Temperature Range		
LH0091		−65°C to +150°C
LH0091C		−25°C to +85°C
Lead Temperature (Soldering, 10 seconds)		300°C

electrical characteristics $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

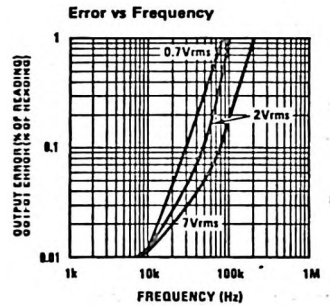
Transfer Function = $E_{O(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$

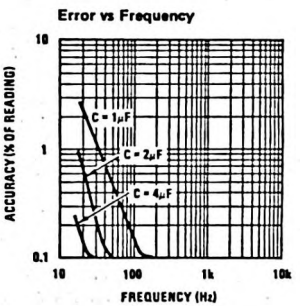
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Definition of Terms)					
Total Unadjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 1)*		20, ±0.5	40, ±1.0	mV, %
Total Adjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 3)*		0.5, ±0.05	1, ±0.2	mV, %
Total Unadjusted Error vs Temperature	−25°C ≤ T_A ≤ +70°C		0.25, ±0.02%		mV, %/°C
Total Unadjusted Error vs Supply Voltage			1		mV/V
AC PERFORMANCE					
Frequency for Specified Adjusted Error	Input = 7Vrms, Sinewave *(Figure 3)*	30	70		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		40		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		20		kHz
Frequency for 1% Additional Error	Input = 7Vrms, Sinewave *(Figure 3)*	100	200		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		75		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		50		kHz
Bandwidth (3 dB)	Input = 7Vrms, Sinewave *(Figure 3)*		2		MHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		1.5		MHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		0.8		MHz
Crest Factor	Rated Adjusted Accuracy Using the High Crest Factor Circuit *(Figure 5)*	5	10		
INPUT CHARACTERISTICS					
Input Voltage Range	For Rated Performance	±0.05		±11	Vpeak
Input Impedance		4.5	5		kΩ
OUTPUT CHARACTERISTICS					
Rated Output Voltage	$R_L \geq 2.5$ kΩ	10			V
Output Short Circuit Current			22		mA
Output Impedance			1		Ω
POWER SUPPLY REQUIREMENTS					
Operating Range		±5		±20	V
Quiescent Current	$V_S = \pm 15V$		14	18	mA

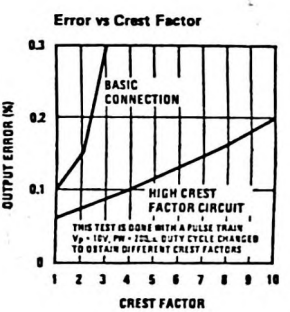
op amp electrical characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	10	mV
I_{OS}	Input Offset Current			4.0	200	nA
I_{BB}	Input Bias Current			30	500	nA
R_{IIN}	Input Resistance			2.5		MΩ
A_{OOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15	160		V/mV
V_{OO}	Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±13		V
V_{III}	Input Voltage Range		±10			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		90		dB
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		96		dB
I_{SOC}	Output Short-Circuit Current			25		mA
S_R	Slew Rate (Unity Gain)			0.5		V/μs
BW	Small Signal Bandwidth			1.0		MHz

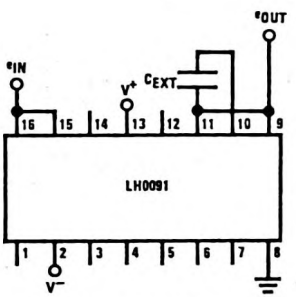
typical performance characteristics







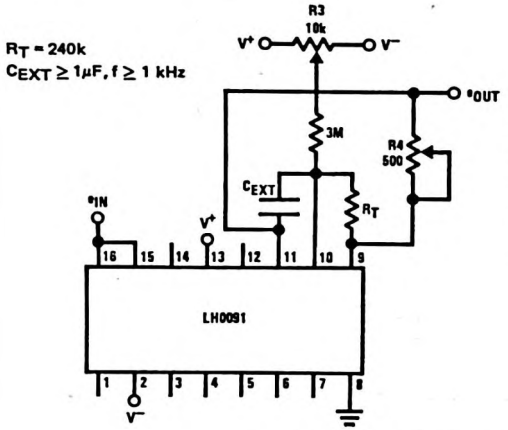
typical applications (All applications require power supply by-pass capacitors.)



$C_{EXT} \geq 1\mu F$; frequency ≥ 1 kHz

FIGURE 1. LH0091 Basic Connection (No Trim)

typical applications (con'd)

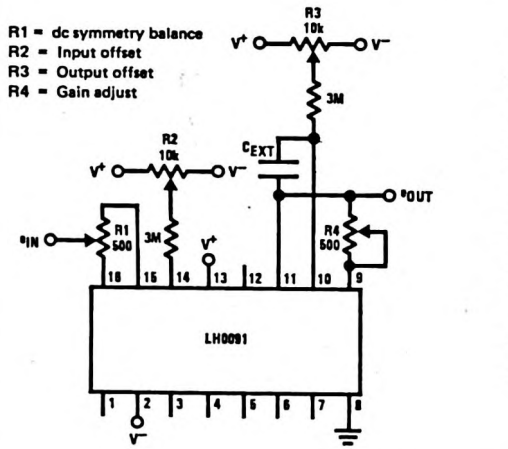


Note. The easy trim procedure is used for ac coupled input signals. It involves two trims and can achieve accuracies of 2 mV offset ±0.1% reading.

Procedure:

1. Apply 100 mV rms (sine wave) to input, adjust R3 until the output reads 100 mV_{DC}.
2. Apply 5 V_{rms} (sine wave) to input, adjust R4 until the output reads 5 V_{DC}.
3. Repeat steps 1 and 2 until the desired initial accuracy is achieved.

FIGURE 2. LH0091 "Easy Trim" (For ac Inputs Only)

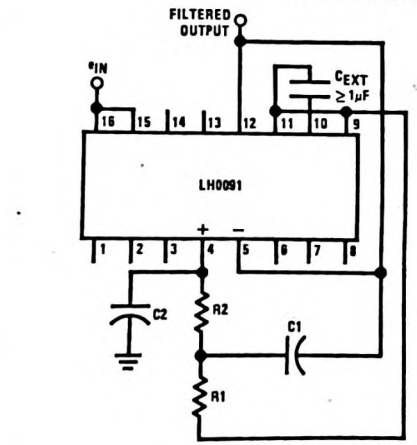


Note. This procedure will give accuracies of 0.5 mV offset ±0.05% reading for inputs from 0.05V peak to 10V peak.

Procedure:

1. Apply 50 mV_{DC} to the input. Read and record the output.
2. Apply −50 mV_{DC} to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50 mV to the input. Use R3 to adjust the output for 50 mV.
4. Apply −50 mV to input. Use R2 to adjust the output for 50 mV.
5. Apply ±10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

FIGURE 3. LH0091 Standard dc Trim Procedure



Note. The additional op amp in the LH0091 may be used as a low pass filter as shown in *Figure 4*.

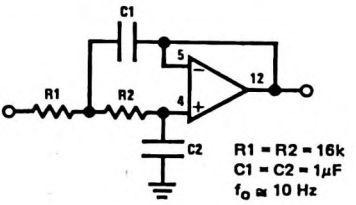
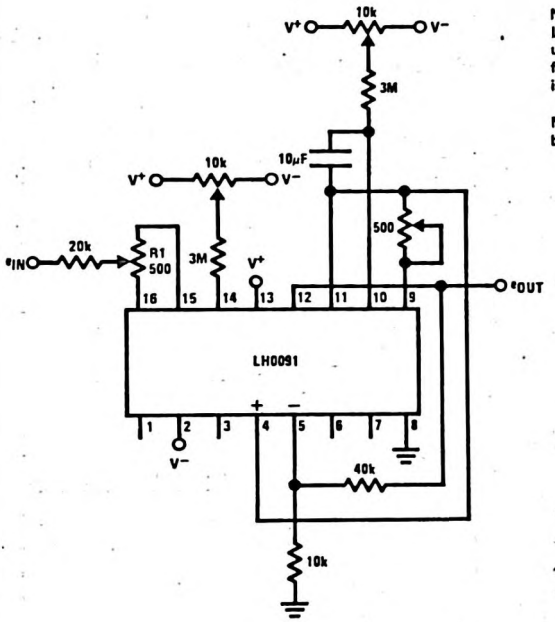


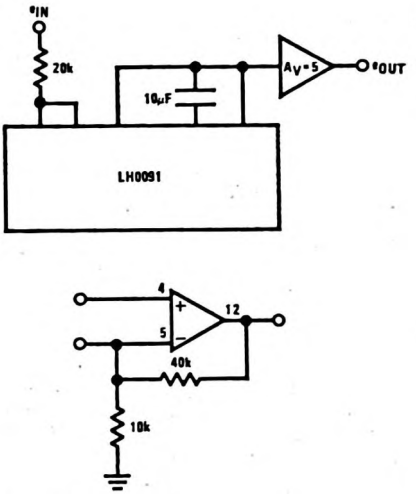
FIGURE 4. Output Filter Connection Using the Internal Op Amp

typical applications (con'd)



Note. When converting signals with a crest factor ≥ 2, the LH0091 should be connected as shown. Note that this circuit utilizes a 20k resistor to drop the input current by a factor of five. The frequency response will correspond to a voltage which is 1/5 e_{IN}.

Note that the extra op amp in the LH0091 may be used to build a gain of 5 amplifier to restore the output voltage.



Note. Response time of the dc output voltage is dominated by the RC time constant consisting of the total resistance between pins 9 and 10 and the external capacitor, C_{EX}.

FIGURE 5. High Crest Factor Circuit

definition of terms

True rms to dc Converter: A device which converts any signal (ac, dc, ac + dc) to the dc equivalent of the rms value.

Error: is the amount by which the actual output differs from the theoretical value. Error is defined as a sum of a fixed term and a percent of reading term. The fixed term remains constant, regardless of input while the percent of reading term varies with the input.

Total Unadjusted Error: The total error of the device without any external adjustments.

Bandwidth: The frequency at which the output dc voltage drops to 0.707 of the dc value at low frequency.

Frequency for Specified Error: The error at low frequency is governed by the size of the external averaging capacitor. At high frequencies, error is dependent on the frequency response of the internal circuitry. The frequency for specified error is the maximum input frequency for which the output will be within the specified error band (i.e., frequency for 1% error means the input frequency must be less than 200 kHz to maintain an output with an error of less than 1% of the initial reading.

Crest Factor: is the peak value of a waveform divided by the rms value of the same waveform. For high crest factor signals, the performance of the LH0091 can be improved by using the high crest factor connection.

National Semiconductor

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_o = V_y \left(\frac{V_z}{V_x}\right)^m, \quad 0.1 \leq m \leq 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

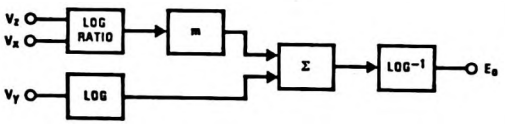
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m = 2 and m = 0.5

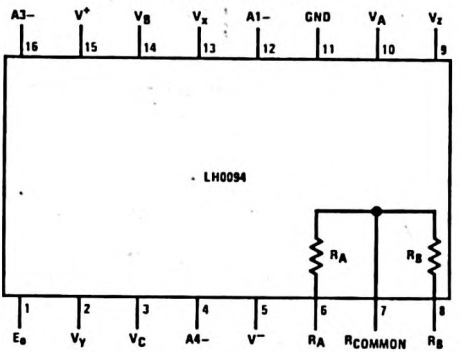
Applications

- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



Dual-In-Line Package

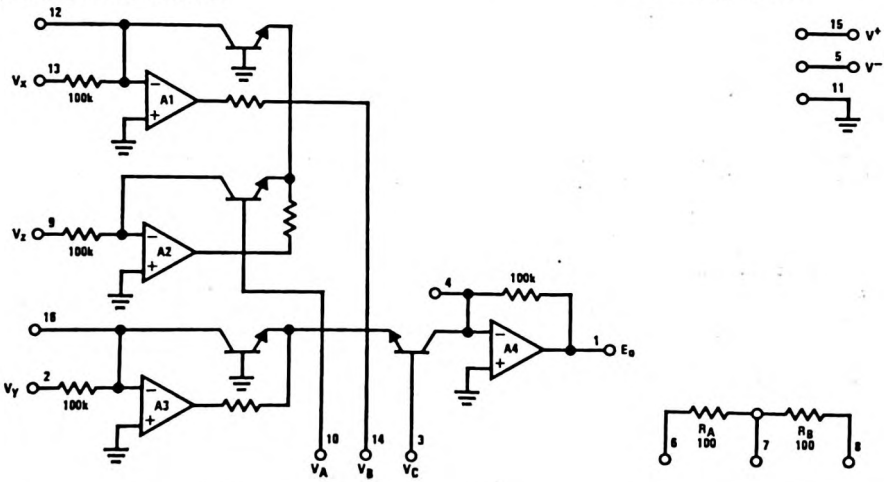


TOP VIEW

Order Number LH0094HY

See NS Package HY16B

Simplified Schematic



Absolute Maximum Ratings

Supply Voltage	±22V	Storage Temperature Range	
Input Voltage	±22V	LH0094D	−65°C to +150°C
Output Short-Circuit Duration	Continuous	LH0094CD	−55°C to +125°C
Operating Temperature Range		Lead Temperature (Soldering, 10 seconds)	300°C
LH0094CD	−25°C to +85°C		
LH0094D	−55°C to +125°C		

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$; $0.1 \le m \le 10$; $0V \le V_X, V_Y, V_Z \le 10V$

PARAMETER	CONDITIONS	LH0094			LH0094C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Multiply	$E_O = \frac{V_Z V_Y}{10}$ $(0.03 \le V_Y \le 10V; 0.01 \le V_Z \le 10V)$							% F.S.
Untrimmed	*(Figure 2)*		0.25	0.45		0.45	0.9	(10V)
External Trim	*(Figure 3)*		0.10			0.1		% F.S.
	vs Temperature		0.2			0.2		mV/°C
Divide	$E_O = 10\ V_Z/V_X$							
Untrimmed	*(Figure 4)*, $(0.5 \le V_X \le 10; 0.01 \le V_Z \le 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 5)*, $(0.1 \le V_X \le 10; 0.01 \le V_Z \le 10)$		0.10			0.1		% F.S.
	vs Temperature		0.2			0.2		mV/°C
Sq. Root	$E_O = 10\sqrt{V_Z/10}$							
Untrimmed	*(Figure 8)*, $(0.03 \le V_Z \le 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 9)*, $(0.01 \le V_Z \le 10)$		0.15			0.15		% F.S.
Square	$E_O = 10\ (V_Z/10)^2$ $(0.1 \le V_Z \le 10)$							
Untrimmed	*(Figure 6)*		0.5	1.0		1.0	2.0	% F.S.
External Trim	*(Figure 7)*		0.15			0.15		% F.S.
Low Level Sq. Root	$E_O = \sqrt{10\ V_Z}$; $5\ mV \le V_Z \le 10V$ *(Figure 10)*		0.05			0.05		% F.S.
Exponential Circuits	$m = 0.2$ $E_O = 10\ (V_Z/10)^2$ *(Figure 11)*, $(0.1 \le V_Z \le 10)$		0.05			0.08		% F.S.
	$m = 5$ $E_O = 10\ (V_Z/10)^5$ *(Figure 11)*, $(1 \le V_Z \le 10)$		0.05			0.08		% F.S.
OUTPUT OFFSET								
	$V_X = 10.0V$, $V_Y = V_Z = 0.0$		2	5		5	10	mV
AC CHARACTERISTICS								
3 dB BANDWIDTH	$m = 1.0$ $V_X = V_Z = 10.0V$ $V_Y = 0.1$ Vrms		10			10		kHz
NOISE	10 Hz to 1 kHz $m = 1$, $V_Y = V_Z = 0.0V$							
	$V_X = 10V$		100			100		μVrms
	$V_X = 0.1V$		300			300		μVrms
EXPONENTS								
m		0.2 to 5	0.1 to 10		0.2 to 5	0.1 to 10		
INPUT CHARACTERISTICS								
Input Voltage	(For Rated Performance)	0		10	0		10	V
Input Impedance	(All Inputs)	98	100		98	100		kΩ
OUTPUT CHARACTERISTICS								
Output Swing	($R_L \ge 10k$)	10	12		10	12		V
Output Impedance			1			1		Ω
Supply Current	($V_S = \pm 15V$), Note 1		3	5		3	5	mA

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode *(Figure 1)* is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

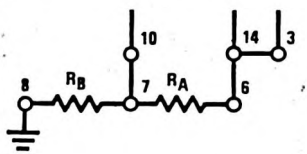
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

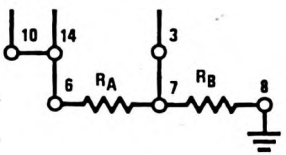
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ±10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*

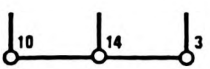


*No external resistors required, strap as indicated

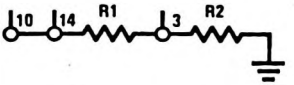
External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

(a) m = 1

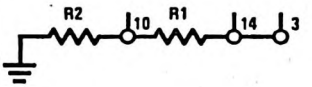


(b) m < 1



$$m = \frac{R2}{R1 + R2} \qquad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

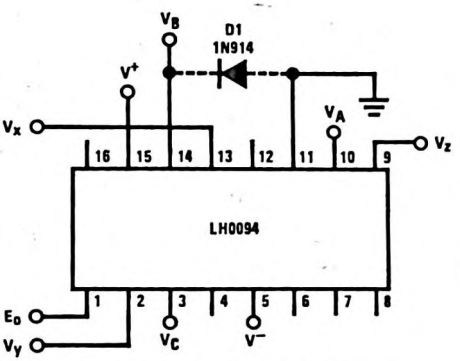
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponents—otherwise, results may be misinterpreted. For example, consider the 1/10th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION



$$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

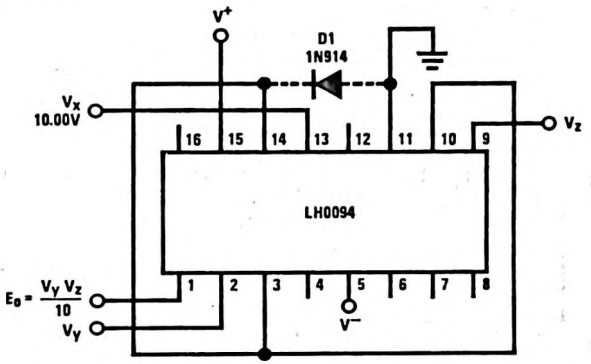


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

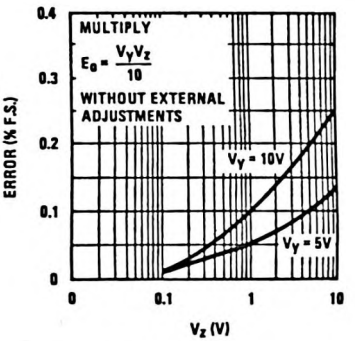


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment

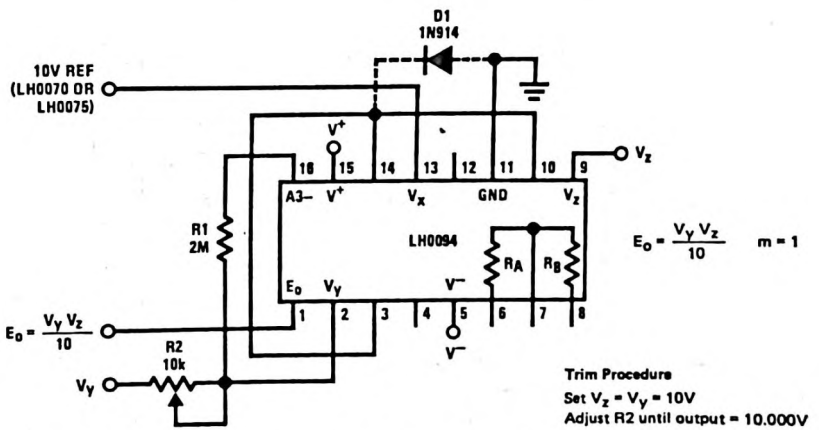


FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

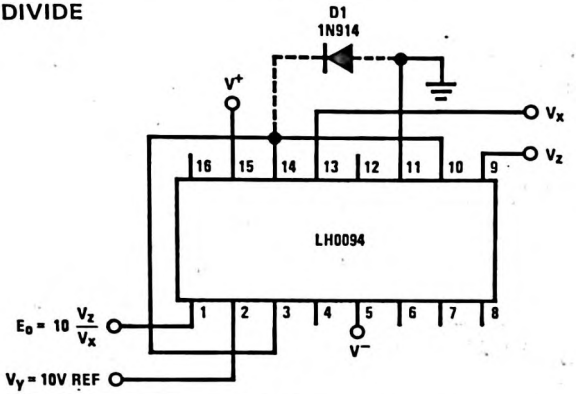


FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

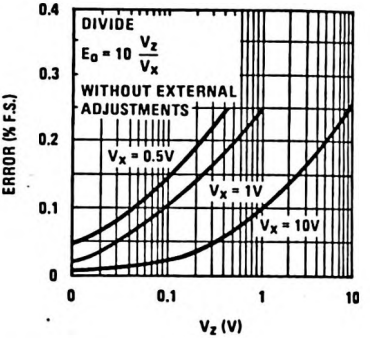


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

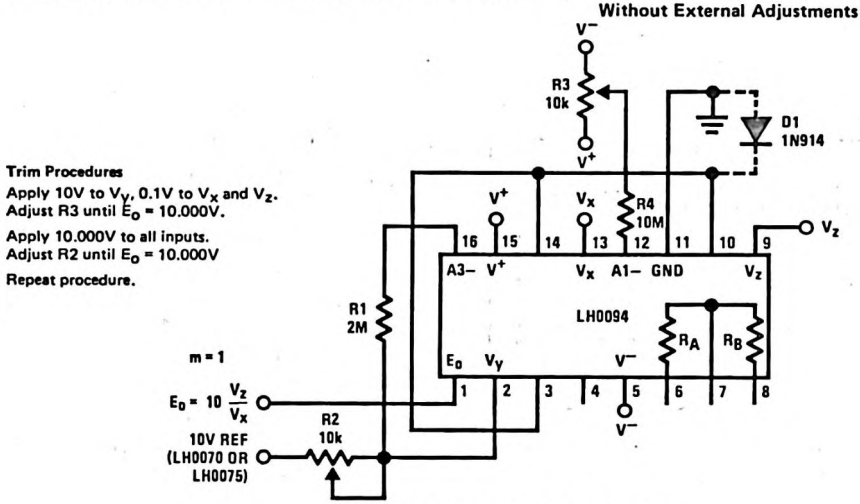


FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

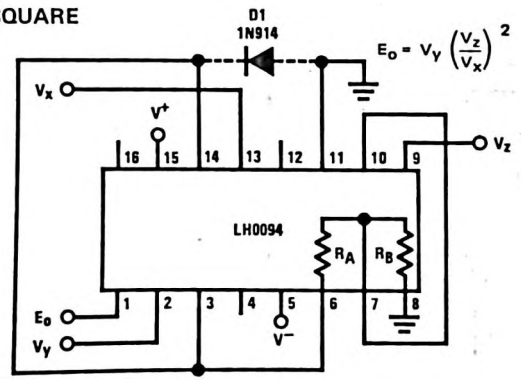


FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

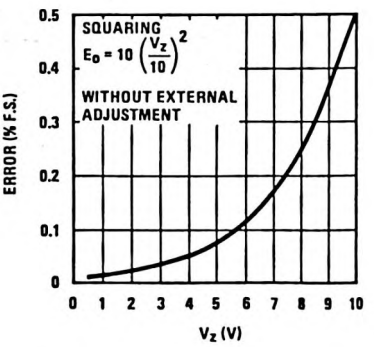


FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)

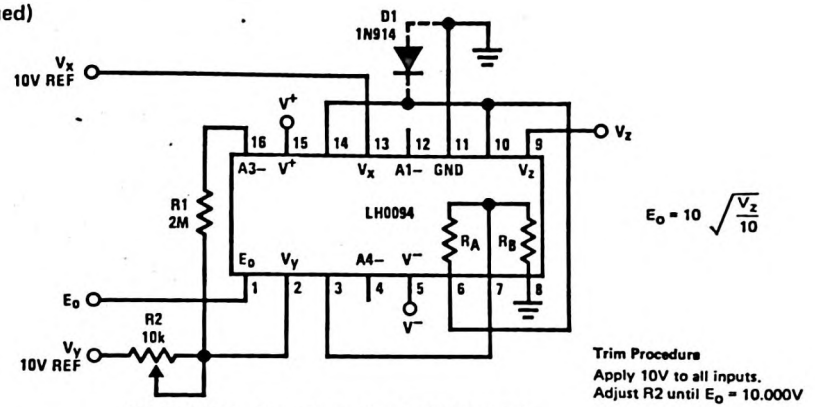


FIGURE 7. Precision Square Rooter (0.15% Typ)

5. SQUARE ROOT

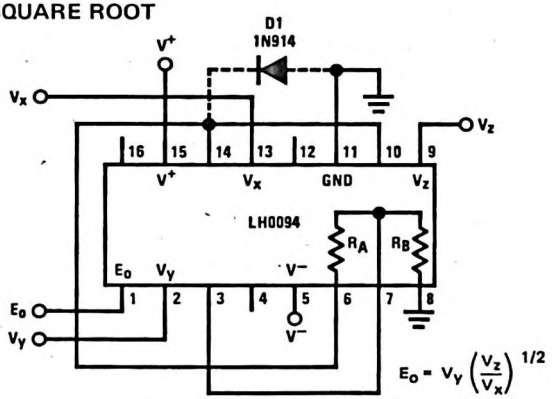


FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

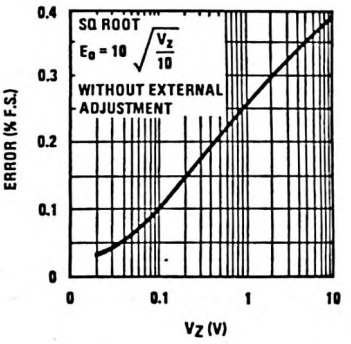


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment

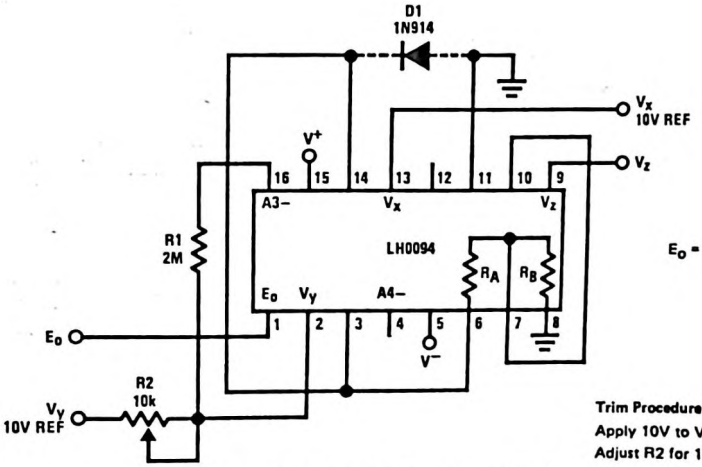


FIGURE 9. Precision Squaring Circuit (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT

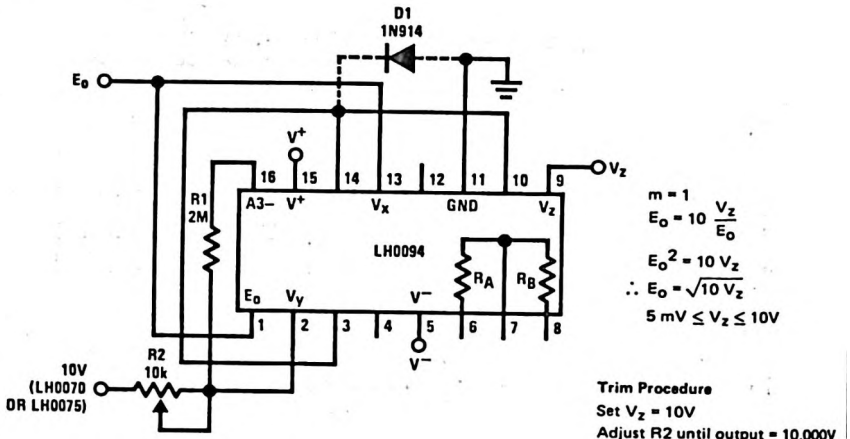


FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications

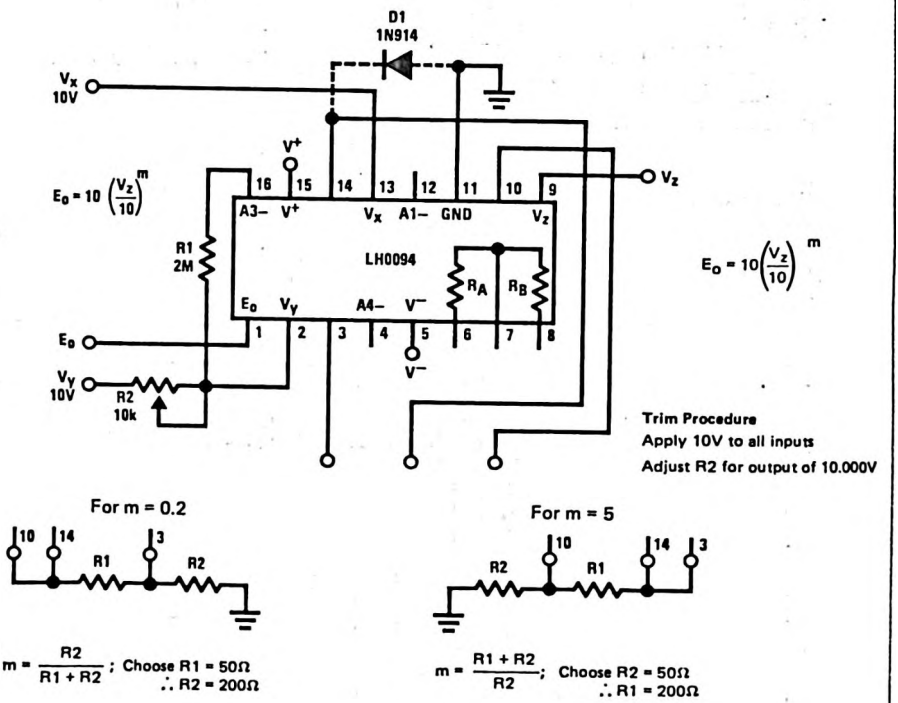
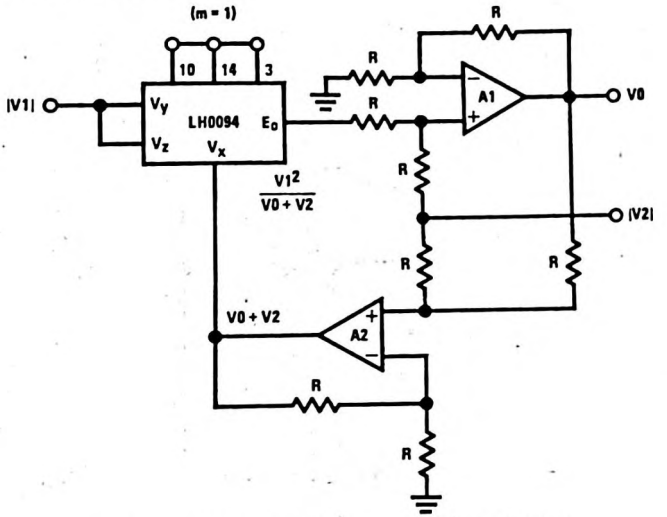


FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$$V0 = \sqrt{V1^2 + V2^2}$$

$$V0 = V2 + \frac{V1^2}{V0 + V2}$$

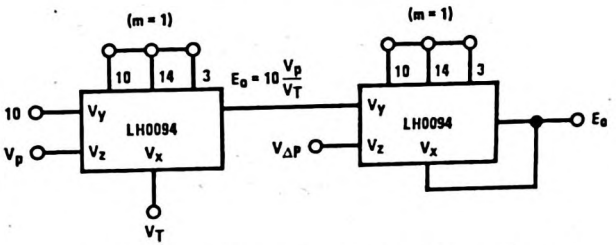
$$V0^2 + V0\,V2 = V2\,V0 + V2^2 + V1^2$$

$$V0^2 = V1^2 + V2^2$$

$$\therefore\ V0 = \sqrt{V1^2 + V2^2} \qquad V1, V2\ 0 \rightarrow 10V$$

R ≈ 10k
National Semiconductor resistor array RA08–10k is recommended

FIGURE 12. Vector Magnitude Function



Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k\sqrt{\frac{P\Delta P}{T}}$$

$$E_o = 10\,\frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_o}$$

$$E_o^2 = 10\,\frac{V_P\,V_{\Delta P}}{V_T}$$

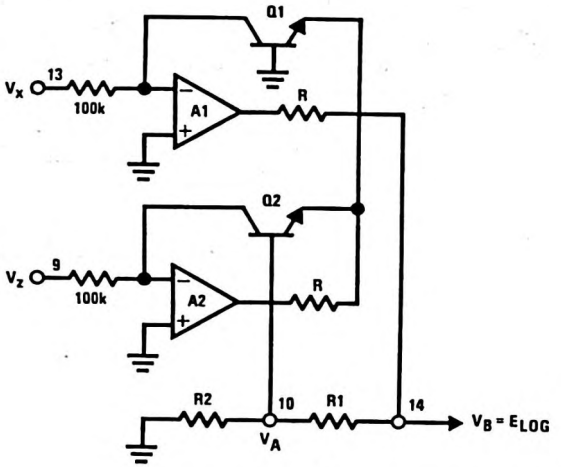
$$E_o = \sqrt{10\,\frac{V_P\,V_{\Delta P}}{V_T}}$$

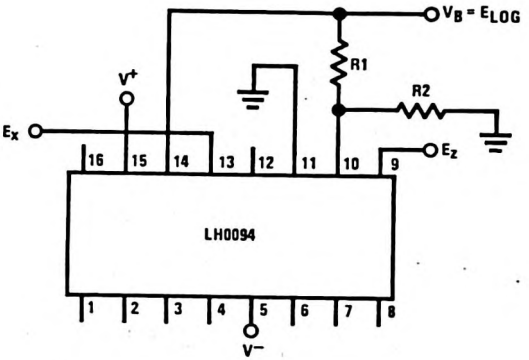
P = Absolute pressure
T = Absolute temperature
ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

13

Typical Applications (Continued)





Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ln \frac{V_z}{V_x}$$

where $K1 = \frac{R1 + R2}{R2}$

If $K1 = \frac{1}{KT/q \ln 10}$

then $E_{LOG} = \text{Log}_{10} \frac{V_z}{V_x}$

$R1 = 15.9\ R2$
$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of ≈ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

general description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

features

- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- High segment sourcing current — 40 mA @ $V_{CC} - 1.6V$, $V_{CC} = 5V$
- Internal multiplexing circuitry

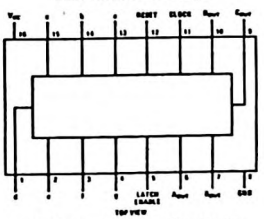
design considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DM75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

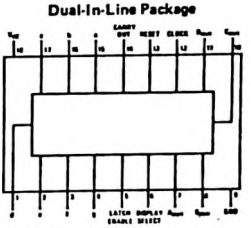
connection diagrams

Dual-In-Line Package



Order Number MM74C925N
See NS Package N16A

Dual-In-Line Package



Order Number MM74C926N, MM74C927N
or MM74C928N
See NS Package N18A

functional description

Reset	— Asynchronous, active high
Display Select	— High, displays output of counter Low, displays output of latch
Latch Enable	— High, flow through condition Low, latch condition
Clock	— Negative edge sensitive
Segment Output	— Current sourcing with 80 mA @ $V_{OUT} = V_{CC} - 1.6V$ typical. Also, sink capability = 2 LTTL loads
Digit Output	— Current sourcing with 1 mA @ $V_{OUT} = 1.75V$. Also, sink capability = 2 LTTL loads
Carry-out	— 2 LTTL loads. See carry-out waveforms.

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absolute maximum ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V
Voltage at Any Input Pin	Gnd − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply at −40°C ≤ T_j ≤ +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20		Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{JA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

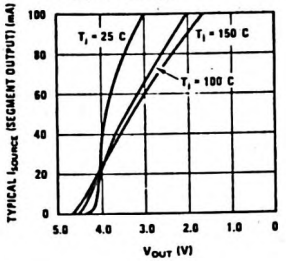
Note 4: θ_{JA} measured in free-air with device soldered into printed circuit board.

acc electrical characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified

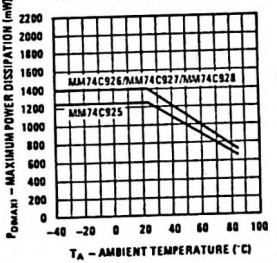
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$, Square Wave Clock	$T_j = 25°C$	2	4		MHz
			$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5.0V$	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5.0V$			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

typical performance characteristics

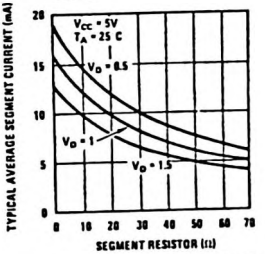
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature



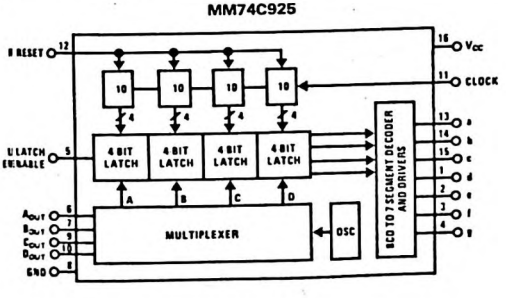
Typical Average Segment Current vs Segment Resistor Value



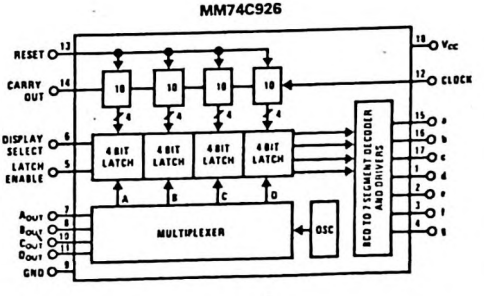
Note. V_D = Voltage across digit driver.

logic and block diagrams

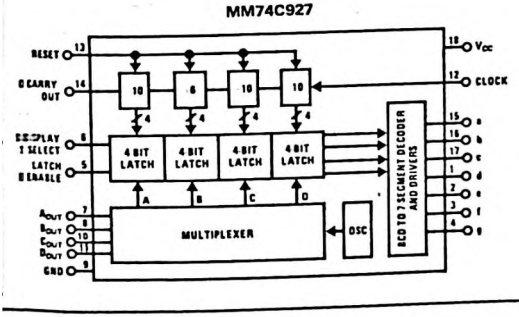
MM74C925



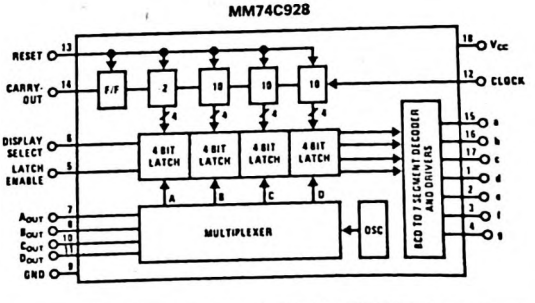
MM74C926



MM74C927



MM74C928



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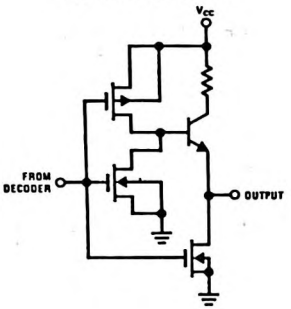
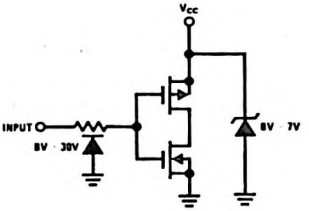
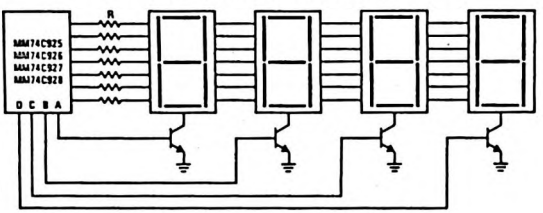
Segment Output Driver



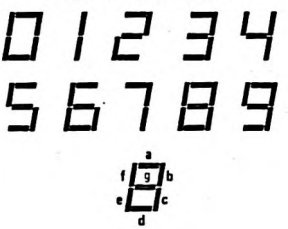
Input Protection



Common Cathode LED Display

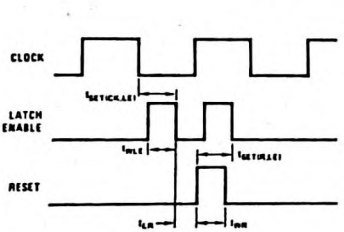


Segment Identification

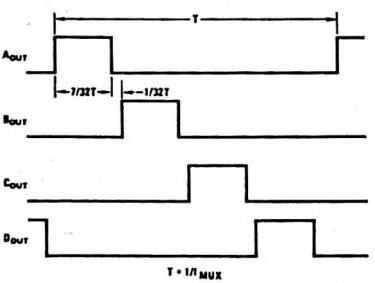


switching time waveforms

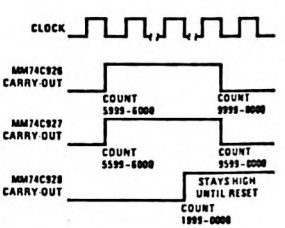
Input Waveforms



Multiplexing Output Waveforms



Carry-Out Waveforms



NSB5388 3 1/2-Digit 0.5 Inch LED Display

General Description

The NSB5388 is a 3 1/2-digit, 0.5 inch high GaAsP LED display. Basically a common cathode multiplexed display, the NSB5388 features separate access to the ± sign and decimal points and is directly compatible with the ADD3500, ADD3501 DVM circuit. Electrical connection is by PCB type terminals on the edge of the display.

The optical design of this unit creates a distinct, easy to read display with a wide viewing angle, excellent ON/OFF contrast and segment uniformity. The NSB5388 provides the designer with an effective, easy to implement answer to the need for an inexpensive large numeric display.

Recommended Display Processing

The multidigit series display is constructed on a standard printed circuit board substrate and covered with a plastic lens. The edge connector tab will stand 230°C for 5 seconds. Permanent damage to the display will result if lens temperature exceeds 70°C. Since the display is not hermetic, immersion of the entire package during flux and clean operation may cause condensation of flux or cleaner on the underside of the lens. Only the edge connectors should be immersed.

Rosin core solder, solid core solder, and low activity organic fluxes are recommended. Freon TF, Isopropanol, Methanol or Ethanol solvents are recommended only at room temperature and for short periods. The use of other solvents or elevated temperature use of the recommended solvents may cause permanent damage to the lens or display.

Applications

- Digital instrumentation
  - Power supply readouts
  - Multimeters
  - Panel meters

Absolute Ratings

Average Current per Segment	20 mA max
Peak Current per Segment	75 mA max
Reverse Voltage per Segment	3.0V max
Operating and Storage Temperature	−20°C to +70°C
Relative Humidity at 35°C	98%
Lead Temperature (Soldering, 5 seconds)	230°C

Electrical and Optical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity (Peak)	10 mA/Seg. Peak	0.10	0.20		mcd
Digit and D.P. Light Intensity (Peak)	10 mA/Seg. Peak	0.80	1.6		mcd
Segment Forward Voltage	10 mA/Seg. Peak		1.7	2.0	V
Segment Reverse Voltage	100 μA/Seg.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Width, Half-Intensity			40		nm
Viewing Angle, Off Axis			60		degrees
Intensity Matching	10 mA/Seg. Avg.		±33		%

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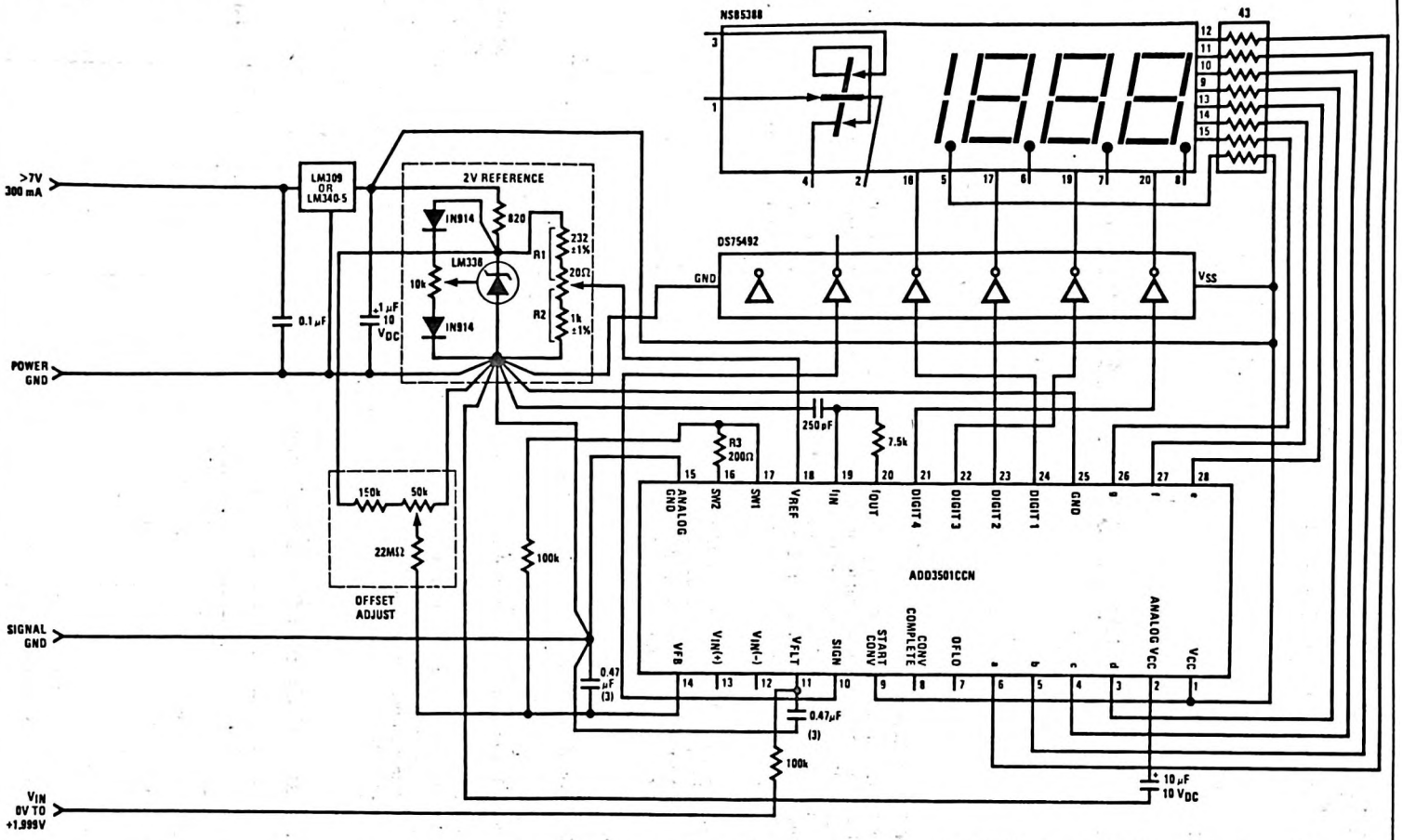
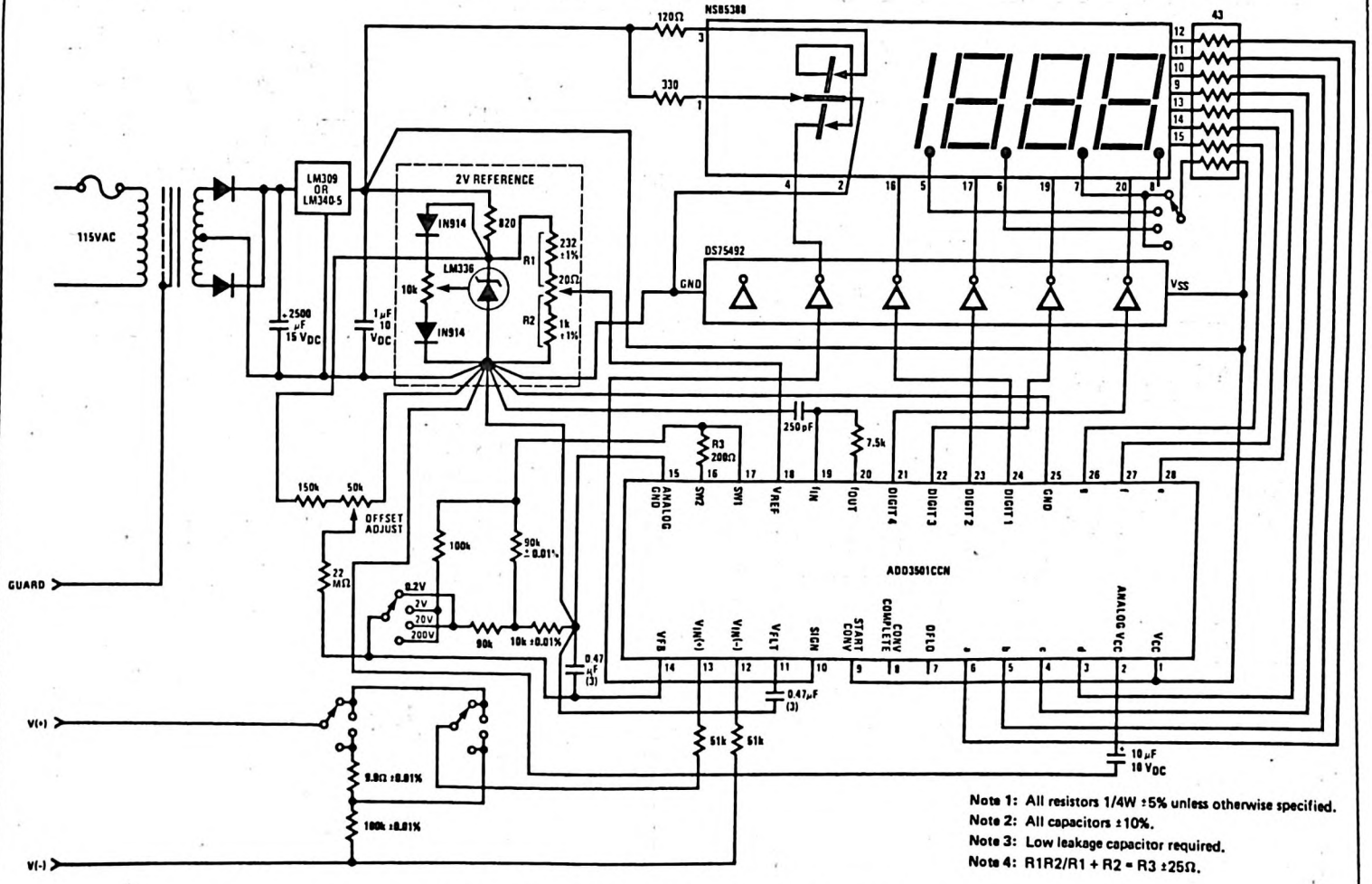
Typical Applications



Note 1: All resistors 1/4W ±5% unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor required.
Note 4: R1R2/R1 + R2 = R3 ±25Ω.

FIGURE 1. 3 1/2-Digit DPM, +1.999V Full-Scale



Note 1: All resistors 1/4W ±5% unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor required.
Note 4: R1R2/R1 + R2 = R3 ±25Ω.

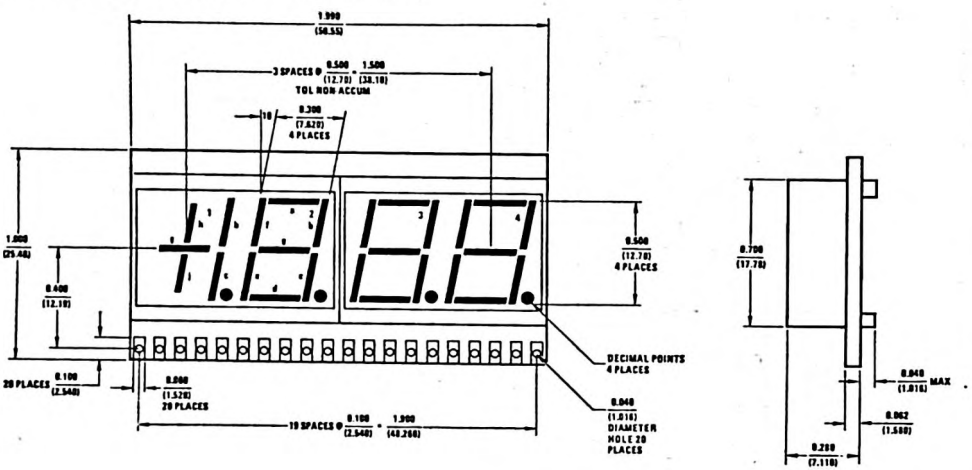
FIGURE 2. 3 1/2-Digit DVM, 4-Decade, ±0.2V, ±2V, ±20V and ±200V Full-Scale

Pin Connections

PIN NO.	ELECTRICAL CONNECTION
1	Digit No. 1 Segment G Anode
2	Digit No. 1 Segment G Cathode
3	Digit No. 1 Segment H Anode *
4	Digit No. 1 Segment J Cathode *
5	Digit No. 1 Segment DP Anode
6	Digit No. 2 Segment DP Anode
7	Digit No. 3 Segment DP Anode
8	Digit No. 4 Segment DP Anode
9	Segment D Anode
10	Segment C Anode
11	Segment B Anode
12	Segment A Anode
13	Segment E Anode
14	Segment F Anode
15	Segment G Anode
16	Digit No. 1 Cathode
17	Digit No. 2 Cathode
18	NC
19	Digit No. 3 Cathode
20	Digit No. 4 Cathode

*Segments H and J internally connected in series

Physical Dimensions inches (millimeters)



Note 1: Material: super-punch circuit board or approved equivalent 0.062 thick.
Note 2: All tolerances are 0.015 (0.38).

NSB5918 3 3/4-Digit 0.5 Inch LED Display

General Description

The NSB5918 is a 3 3/4-digit, 0.5 inch high GaAsP LED display. Basically a common cathode multiplexed display, the NSB5918 features separate access to the ± sign and decimal points and is directly compatible with the ADD3701 DVM circuit. Electrical connection is by PCB type terminals on the edge of the display. The 3 3/4-digit is distinguished from 3 1/2 and 4 1/2-digit designs by the fact that the overflow sign is followed by 4 full 7-segment digits.

The optical design of this unit creates a distinct, easy to read display with a wide viewing angle, excellent ON/OFF contrast and segment uniformity. The NSB5918 provides the designer with an effective, easy to implement answer to the need for an inexpensive large numeric display.

Recommended Display Processing

The multidigit series display is constructed on a standard printed circuit board substrate and covered with a plastic lens. The edge connector tab will stand 230°C for 5 seconds. Permanent damage to the display will result if lens temperature exceeds 70°C. Since the display is not hermetic, immersion of the entire package during flux and clean operation may cause condensation of flux or cleaner on the underside of the lens. Only the edge connectors should be immersed.

Rosin core solder, solid core solder, and low activity organic fluxes are recommended. Freon TF, Isopropanol, Methanol or Ethanol solvents are recommended only at room temperature and for short periods. The use of other solvents or elevated temperature use of the recommended solvents may cause permanent damage to the lens or display.

Applications

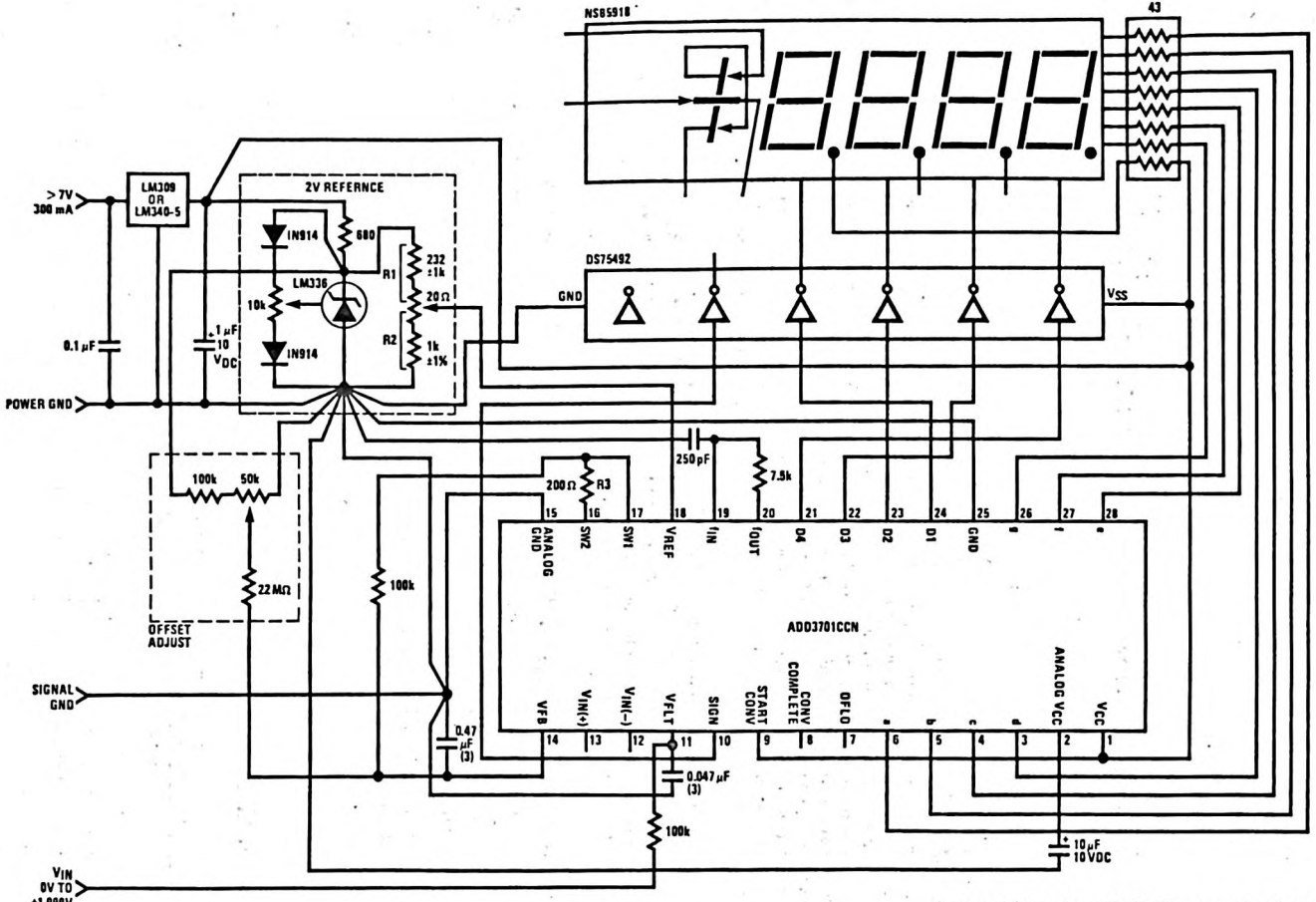
- Digital instrumentation
  - Power supply readouts
  - Multimeters
  - Panel meters

Absolute Ratings

Average Current per Segment	20 mA max
Peak Current per Segment	75 mA max
Reverse Voltage per Segment	3.0V max
Operating and Storage Temperature	−20°C to +70°C
Relative Humidity at 35°C	98%
Lead Temperature (Soldering, 5 seconds)	230°C

Electrical and Optical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity	10 mA/Seg. Avg.	0.10	0.20		mcd
Digit and D.P. Light Intensity	10 mA/Seg. Avg.	0.80	1.6		mcd
Segment Forward Voltage	10 mA/Seg.		1.7	2.0	V
Segment Reverse Voltage	100 μA/Seg.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Width, Half-Intensity			40		nm
Viewing Angle, Off Axis			60		degrees
Intensity Matching	10 mA/Seg. Avg.		±33		%



Note 1: All resistors 1/4W ±5% unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor required.
Note 4: R1R2/R1 + R2 = R3 ±25Ω.

FIGURE 1. 3 3/4-Digit DVM, +3.999 Count Full-Scale

Typical Applications (Continued)

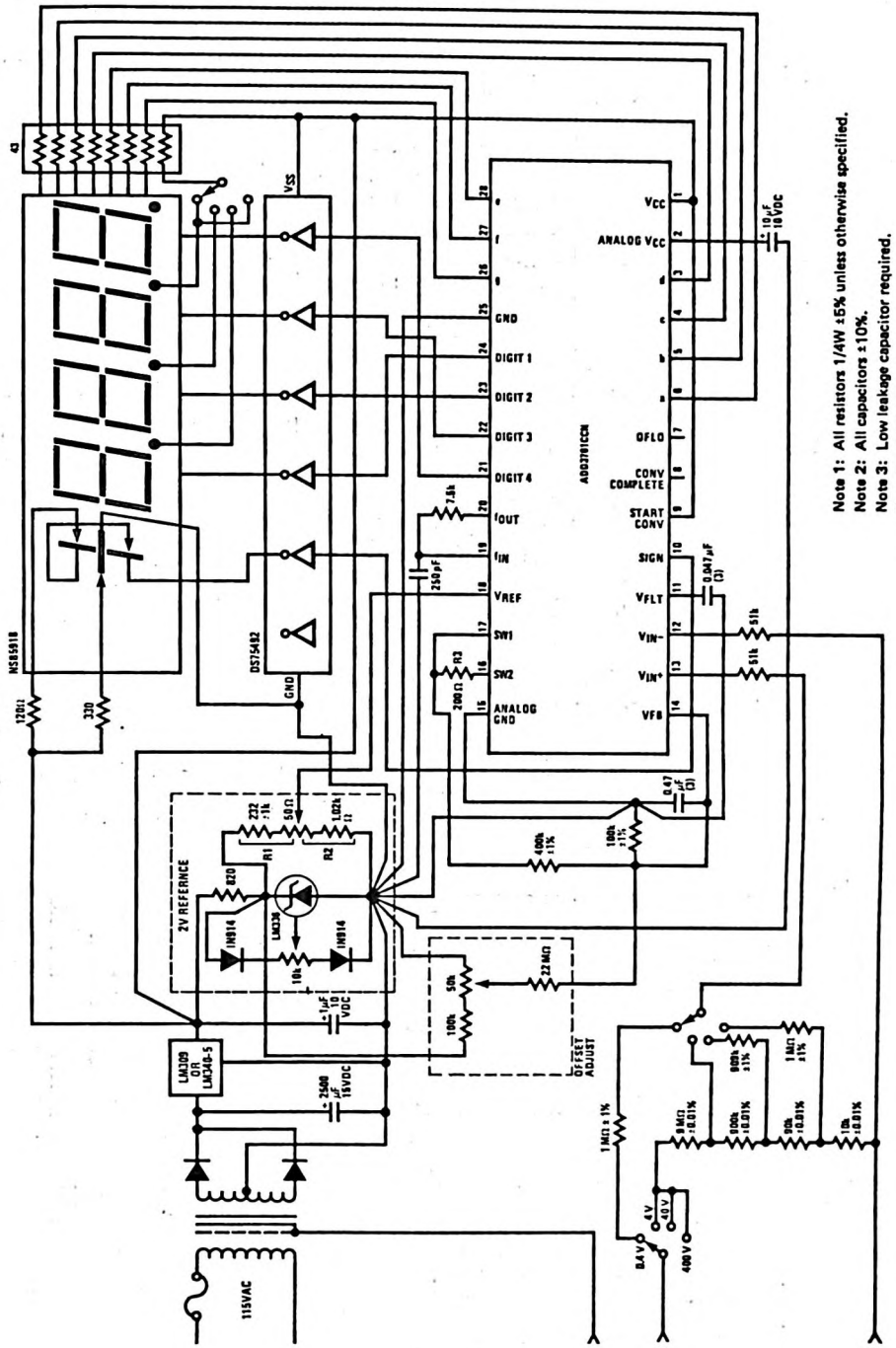


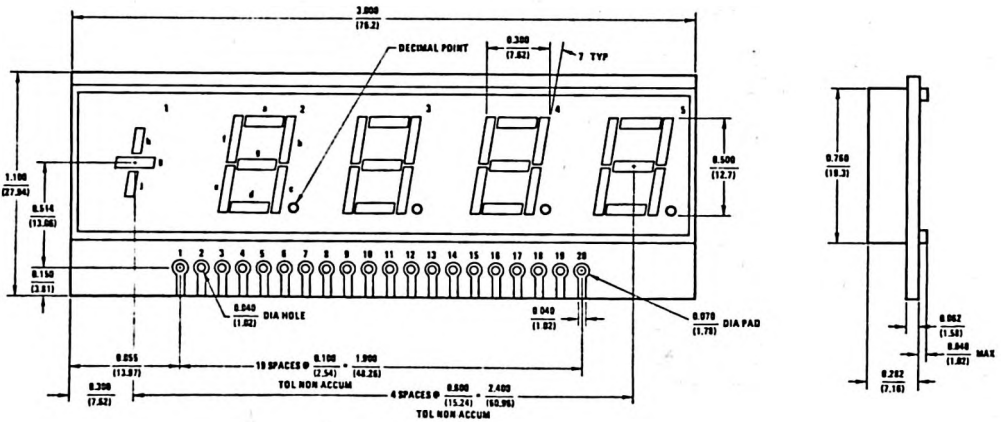
FIGURE 2. 3 3/4-Digit DVM, 4-Decade, ±0.4V, ±4V, ±40V and ±400V Full-Scale

Pin Connections

PIN NO.	ELECTRICAL CONNECTION
1	Digit No. 1 Segment G Anode
2	Digit No. 1 Segment G Cathode
3	Digit No. 1 Segment H Anode *
4	Digit No. 1 Segment J Cathode *
5	Digit No. 2 Segment DP Anode
6	Digit No. 3 Segment DP Anode
7	Digit No. 4 Segment DP Anode
8	Digit No. 5 Segment DP Anode
9	Segment D Anode
10	Segment C Anode
11	Segment B Anode
12	Segment A Anode
13	Segment E Anode
14	Segment F Anode
15	Segment G Anode
16	Digit No. 2 Cathode
17	Digit No. 3 Cathode
18	NC
19	Digit No. 4 Cathode
20	Digit No. 5 Cathode

*Segments H and J internally connected in series

Physical Dimensions inches (millimeters)



Note 1: Material: super-punch circuit board or approved equivalent 0.062 thick.
Note 2: All tolerances are 0.015 (0.38).

Section 14

Application Notes

14

Specifying A/D and D/A Converters

National Semiconductor
Application Note 156
Jim Sherwin
February 1976

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

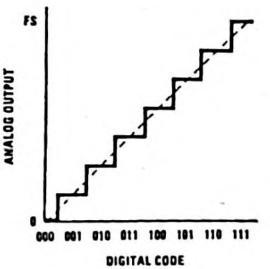


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be ± 0 LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

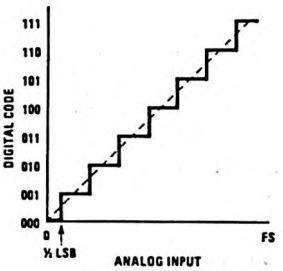


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

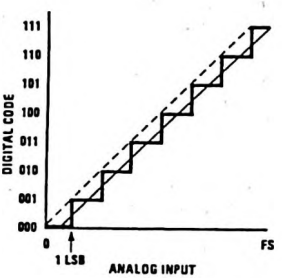


FIGURE 3. ADC Transfer Curve, No Offset

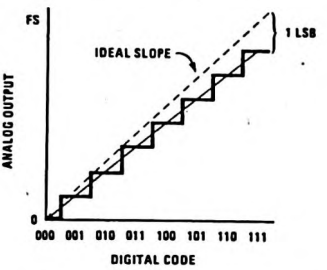


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

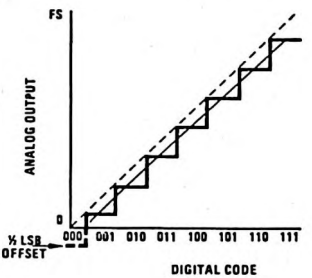


FIGURE 5. Linear, ½ LSB Offset Error

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specifi-

cation of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ≤ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

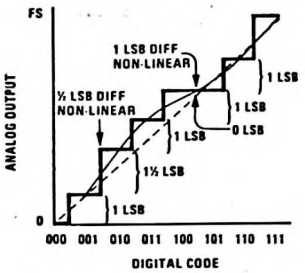


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

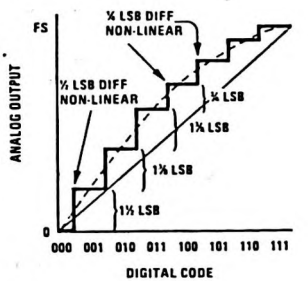


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

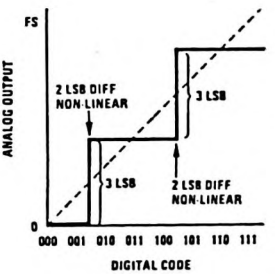


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

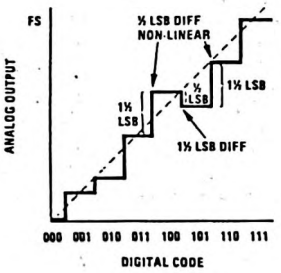
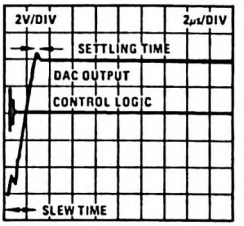
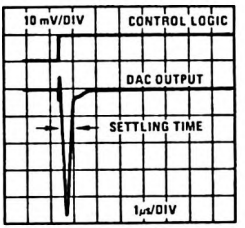


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

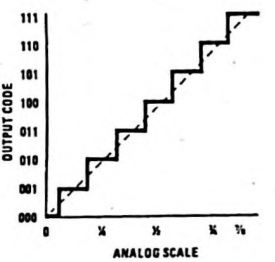
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

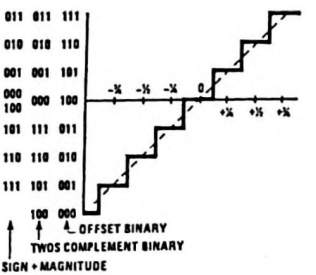
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

Twos Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number –8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

Data Acquisition System Interface to Computers

National Semiconductor
Application Note 159
Jim Sherwin
April 1976

INTRODUCTION

The need of interfacing several analog data channels to computers has not escaped the attention of the data system firms. There are presently available a number of data acquisition units (DAUs) which will directly interface 8-64 analog data channels to one or more types of computers or microcomputers, and more appear on the market almost monthly. Some of these DAUs are even constructed to plug into the mainframe of the computer for which they are designed. Nearly all of these commercially available DAUs are of more or less conventional design, operating in either a random channel address or sequential address mode. Figure 1 shows a typical functional diagram of such a random channel address DAU. Its advantages are simplicity, straightforward design, and comparatively low cost (depending upon performance and special features). In operation, the computer addresses a specific channel, the analog multiplexer (MUX) is set to the desired channel, a sample and hold (S&H) circuit acquires and holds the analog signal, an analog-to-digital converter (ADC) digitizes the signal, a ready signal is returned to the computer, and the data is presented to the data bus via TRI-STATE® bus drivers. If the data is 12-bit and the data bus is 8-bit, the data word must be broken into two bytes and addressed separately. The prime disadvantage of these DAU designs is that the computer must either enter a wait mode while data is readied or it can proceed with its assigned task, watch for a data-ready flag signal, and return for the data.

From the standpoint of microprocessor system design, it is clearly desirable to access input data as if it were main memory. It is further desirable that input data access time be equivalent to that of main memory so that the processor need not enter a wait mode while data is readied for input. One attractive method of accomplishing this is to use one A/D converter (of a type containing TRI-STATE output data latches) on each input data channel. Henceforth I shall refer to this as parallel conversion. Figure 2 shows such a system containing only an address decoder and multiple A/D converters with all outputs wired in parallel onto the data bus. Note the absence of S&H modules.

The advantages of this DAU system are the immediate data access and its simplicity. However, one's first thought on considering a parallel-conversion system might be that the cost of ADCs would exclude their consideration on a one-per-channel basis. But, although this may have been true in the past, currently available monolithic and hybrid ADCs are priced such that this system concept is entirely feasible. Furthermore, the converter price trend is definitely downward as more monolithic units are released, so the economic feasibility can only improve in the next few years, thus extending the application to an ever larger segment of the market. The ideal converter for use in the system of Figure 1 includes converter, comparator, and buffered TRI-STATE output data latches in one package. The unit would

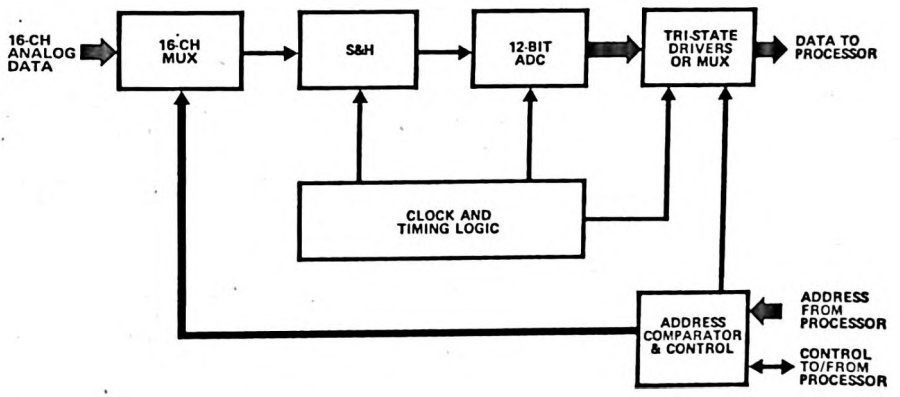


FIGURE 1. Random-Addressed Multiplexed DAU

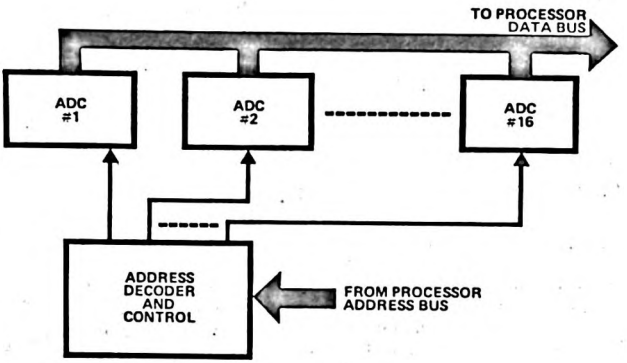


FIGURE 2. Parallel Data Conversion Concept

operate in the continuous convert mode with the last data remaining in the output latches until the next completed conversion shifts new data into the latches. Valid latest data is thus always available for readout on the data bus except for a brief period when the data is being updated. In contrast, a converter without buffered output latches does not hold data after a start-conversion signal and so must be operated in the command mode with a wait for data after the converter is started.

In spite of the advantages of the parallel-conversion DAU, there is (at present ADC prices) a more cost-effective way of providing the same immediate memory-access mode of operation, particularly for 12-bit data. Figure 3 shows a multiplexed DAU with self-contained memory which will interface to computer systems in the memory-access mode without a wait period.

The total package count of this system is lower than that of the parallel-conversion DAU, the cost/channel is lower, and the required space and power is lower. A disadvantage is that the accessed data may be as much as 800μs old, compared to a possible 1-4μs with parallel conversion. The key to the success of the system is the dedicated on-card 16x12 RAM. Neither does the system require a special ADC design with buffered output data latches. Main memory could, of course, be used instead, but then some machine time would be utilized as memory write time. This way, the latest data is always ready and waiting in the DAU (peripheral) memory, and software is considerably simplified.

Before exploring any of the three systems in more detail, it is worth considering the system limitations, the economics, and the probable market segment which could be served by the three types of DAU described.

The required data bandwidth has obvious strong effects on system cost and realization. The bandwidth of a sampled data system is limited by Shannon's sampling criterion and other practical considerations to, say,

$$f_{max} = \frac{1}{5\, t_{conversion}}$$

which is 4kHz for a 50μs conversion cycle time. However, when no S&H module is used ahead of the ADC, as in a parallel-conversion DAU, conversion must take place within the time it takes the input signal to change by ±½ LSB or 1 part in 2^{n+1}. For sine waves, the maximum rate of change is determined as follows:

$$\frac{\Delta v}{\Delta t} = \omega v_{pk},$$

but

$$v_{max} = \frac{2\, v_{pk}}{2^{n+1}}$$

therefore

$$\frac{2\, v_{pk}}{2^{n+1}\, \Delta t} = 2\pi f_{max}\, v_{pk}$$

and

$$f_{max} = \frac{2^{-(n+1)}}{\pi\, t_{conv}}.$$

For the same 50μs conversion time and an 8-bit accuracy requirement of ±½ LSB, f_{max} is 12Hz. Figure 4 compares data bandwidth of 8- to 14-bit systems with and without S&H. The economic effect of adding an S&H module ahead of each ADC in a parallel-conversion DAU is obvious (possibly doubling the cost per channel of an 8-bit system) as is the cost of significantly increasing conversion speed except by use of tracking converters (advantageous only in parallel-conversion systems).

The conventional random-addressed DAU can serve any part of the data acquisition market where the task of the computer is light enough that the system can afford to enter a wait mode at data request. This wait period can be as low as 10-20μs if sufficient money is available for fast S&H circuits and fast ADCs, as high-speed components are traditionally quite expensive. Lower cost systems may require a wait period of 100-200μs before data is available. At the expense of more complex software, the computer could remain busy during the period of data preparation, and would return for the data when it was made ready. The data bandwidth may be deter-

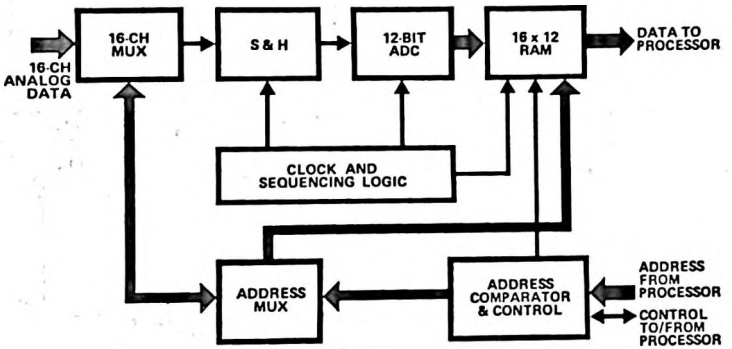


FIGURE 3. Multiplexed Immediate-Data-Access DAU

mined from Figure 4. Sixteen channels of 10Hz data could be available if each channel were sampled once every 20ms. This is a data throughput rate of 16ch x 1/20ms = 800Hz. The higher cost DAUs of this type have capability of 50-100kHz throughput rates. However, if the computer waits while data is made ready, it will be completely occupied with gathering data when the maximum throughput rate is utilized.

The parallel conversion DAU without S&H circuits is destined to operate on low-bandwidth data as indicated in Figure 4. To be economically feasible the ADCs must be of low cost. This means an 8- or 10-bit successive approximation register (SAR) or a 12-bit integrating monolithic ADC must be used. New ADC designs using tracking counters could increase data bandwidth capability over that possible with SAR counters. For purely economic reasons, then, use of parallel-conversion DAU systems will be limited to low bandwidth data — 10-30Hz on 8-bit, 2-5Hz on 10-bit, and less than 1Hz on 12-bit systems. These bandwidth figures for 8- to 10-bit systems could be considerably improved, say by 8-10 times, if tracking converters were used in place of SAR converters. This definitely suggests that there is a need for low-cost tracking converters. Note that S&H circuits are not needed in the parallel-conversion systems.

The multiplexed DAU with memory can serve any segment of the data market. It is limited in bandwidth

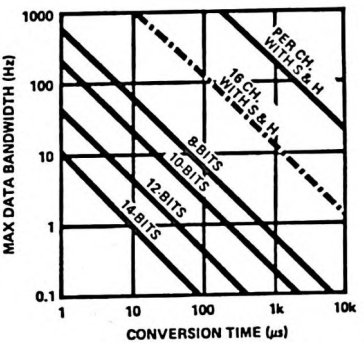


FIGURE 4. Data Bandwidth vs. Conversion Time

or data throughput rate principally by the S&H and ADC operating times, its cost per channel is only slightly higher than that of the conventional DAU, and it allows the computer to operate in the most efficient manner.

A comparison of system costs must include the following for a 16-channel system.

Parallel Conversion	Random Addressed Multiplexed	Multiplexed with Memory
116 A/D Converters	1 A/D Converter	1 A/D Converter
116 Anti-Aliasing Filters	1 S&H Module	1 S&H Module
0Control Circuits	1 16-Channel Multiplexer	1 16-Channel Multiplexer
AAdditional power for extra converters	16 Anti-Aliasing Filters	16 Anti-Aliasing Filters
ILower data bandwidth	More complex control circuits	1 16x12 RAM
SSimple software	Longer data access time	More complex control circuits
	Possibly more complex software	High-speed data access
		Simple Software

14

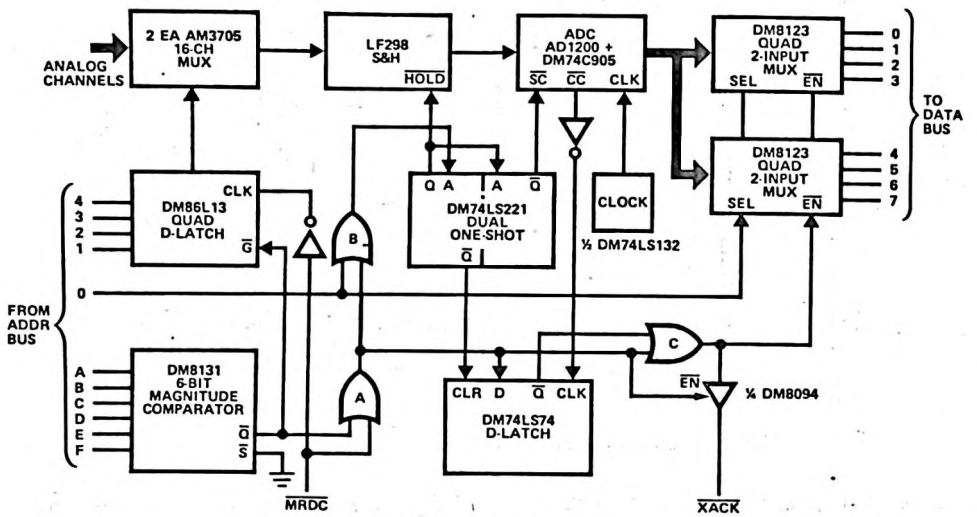


FIGURE 5. Conventional DAU for 8080

The future trends in DAU designs will include an increasing number of parallel-conversion DAUs, especially as cost reductions appear on monolithic ADCs with TRI-STATE output circuits (or latches). We should also start to see some tracking converters in the low-cost monolithics with TRI-STATE output data latches. Expect to see multiplexed DAUs with memory appearing in the near future. Its simplicity from a circuit and software standpoint cannot long go unnoticed.

RANDOM ADDRESSED DATA ACQUISITION UNIT

A conventional, random-addressed, 16-channel, 12-bit DAU is diagrammed in Figure 5. The analog section contains a 16-channel analog multiplexer, a sample-and-hold block, and a 12-bit ADC. A more complete system might contain a differential multiplexer and/or a differential (or instrumentation) amplifier preceding the S&H block. The data output circuits are arranged to interface an 8-bit data bus as found on an 8080 or 6800 microcomputer (μC). Since the data word is 12 bits, the μC must accept it in two 8-bit bytes. Normally the μC would address the DAU with two consecutive address locations corresponding to a 0 and a 1 at the address LSB to load the two bytes of data. The DM8123 multiplexers are ideally suited to this use. They have TRI-STATE output circuits, and the channel-select input may be directly driven from the address LSB. If a 16-bit address bus were being interfaced, such as in the PACE μC, the output multiplexers would be replaced with DM8097 or equivalent TRI-STATE output buffers (see Figure 11). In both instances, low-power versions of these parts, the DM81L23 and DM80L97, could be used to drive a lightly loaded data bus.

The address decoding is accomplished with a DM8161 6-bit magnitude comparator looking at the six most significant address bits. These 6 bits are compared with an address code hard wired into a DIP header which can be different for each DAU card in a system. Comparing only 6 address bits allows a possible 64 cards in a single system and uses up to 64 pages of memory position. If this is not satisfactory, two address comparators ORed together (DM8163) could select from 12 bits of address. The magnitude comparator(s) plus the four address lines to the 16-ch MUX make up the complete address decoding. The output of the magnitude comparator(s) indicates when this DAU has been addressed, and the four address lines to the MUX select the 1-of-16 channels of this DAU.

This circuit is designed to interface the 8080 μC. Thus, a memory read command $\overline{\text{MRDC}}$ must be received, and an acknowledgement $\overline{\text{XACK}}$ must be issued to indicate when data is ready. Operation is as follows: A valid address on address lines A-F causes comparator output $\overline{Q}$ to go low. This gates the inputs of the quad D latch to accept the 1-of-16 address word from address lines 1-4. At the occurrence of $\overline{\text{MRDC}}$ the address is clocked into the quad D latch and presented to the 16-ch MUX which selects the addressed channel. When $\overline{Q}$ and $\overline{\text{MRDC}}$ are both low, the output of OR gate A goes low, which enables the XACK signal buffer. If the address LSB is 0 (byte 1 of a 2-byte data request), OR gate B output goes low to trigger a one-shot.

The one-shot circuits are a simple means of timing the sample period and the converter start commands. There are other methods (see Figure 15) of accomplishing this timing without the hazards associated with one-shot circuits; however, the simplicity of this scheme lends itself to easy understanding of the timing required. The first one-shot generates a sample pulse of 5-30μs as required for the S&H to acquire and settle to 0.01% of value. Its $\overline{Q}$ output presets the single D latch ($\overline{Q}$ = 1). The trailing edge of this pulse returns the S&H to HOLD condition and triggers the next one-shot to generate a start conversion command of about 3μs. When the ADC completes conversion, its $\overline{CC}$ output goes low, thus clocking a 0 into the single D latch to reset its Q output low. Both inputs to OR gate C now being low will enable the output MUX and return a low on the $\overline{\text{XACK}}$

line indicating to the μC that data is ready. Address LSB = 0 selects the 8 LSB of the data word for presentation to the data bus. A subsequent address with LSB = 1 selects the 8 MSB of the data word, but will not trigger the one-shot or preset the D latch because the output of OR gate B will remain high. Since the output of OR gates A and C will be low, $\overline{XACK}$ is returned and the output MUXs are enabled to present byte 2 of the data word on the data bus. When $\overline{MRDC}$ returns high, the output circuits are disabled. If the 6-bit comparator does not see a valid address, no action is taken by the DAU.

This represents the simplest possible DAU for interfacing to computers. The interface to the 8080 is one of the simplest. Only minor modifications are required to interface, for example, the 6800 or PACE μCs (see Figures 9 and 11). The only timing anomaly in the logic system shown is that when the $\overline{XACK}$ buffer is enabled there will be a 10-40ns pulse of 0 output. The computer, however, does not act on an XACK signal at this time and so will enter a wait mode until $\overline{XACK}$ is returned later on.

The analog signal section has purposely been omitted from this discussion of interfacing to processors because its details will depend upon analog signal levels, the possible requirement for differential channels, the possible need of an instrumentation amplifier following the multiplexer, and S&H timing requirements. The analog section of the DAU may be made up of various components, depending upon the required performance and operating conditions. A pair of 8-channel multiplexers will give the flexibility of connecting as differential 8-channel or as single ended 16-channel whereas a single 16-channel MUX with space and wiring on the board for another 16-channel MUX would allow for either 32 channels or 16 differential channels. A pair of AM3705s could be used for lowest cost where analog signals are no greater than ±5V. The S&H circuit could be monolithic LF198, hybrid LH0023, LH0043 or LH0053, made up of individual discrete and integrated circuits, or it could be any of several available modules.

The ADC used in this system may be of a conventional design with speed and accuracy being the only important technical considerations. No special TRI-STATE output or output data latches are needed as the data is latched in the register until a new start conversion (SC) command is given. The ADC could be made up of an AD1200 ADC building block plus DM2504 or MM74C905 successive-approximation register, it could be an AD1210 plus LH0071 reference and appropriate MOS-TTL and TTL-MOS buffers, or it could be any one of a number of other ADCs on the market.

Total power is about 2.8 watts and cost is about $9.50 per channel for components as indicated in Table 1. Note that output drivers are standard TTL circuits whereas low power TTL may be used for lower power dissipation where a lightly loaded data bus is to be driven.

PARALLEL-CONVERSION DATA ACQUISITION UNIT

Parallel data conversion is likely the simplest possible μC data system concept which will effect immediate access to latest input data as if it were main memory. It may be treated as main memory by the processor and is only slightly more complex than the simplified system of Figure 2. The individual ADCs in Figure 2 include TRI-STATE output for direct wire ORing on the data bus. However, to make each capable of driving a heavily loaded system bus would require significant and unnecessary power dissipation in each ADC. Accordingly, except in minimally loaded systems, a separate set of TRI-STATE TTL output data buffers would be added to Figure 2. Small differences in the address decoder and control circuits will exist, depending upon which μC system will be used.

The control circuits are exceptionally simple, being required primarily to accept the memory read command and to return a memory ready signal. The most complex part of the control circuits is that required of μC systems which accept data in two 8-bit bytes rather than in one 16-bit byte, yet even this added complexity is minimal.

Table 1. Conventional DAU Power & Cost

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
2 – DM8123	Quad 2-Input MUX	800	2.56
1 – DM8161	Hex Comparator	250	2.56
1 – DM86L13	Quad D-Latch	30	1.28
1 – DM74LS221	Dual One-Shot	30	3.00
1 – DM74LS132	Quad Schmidt NAND	60	2.00
1 – DM7432	Quad OR Gate	100	.49
1 – DM74LS74	Dual D F-F	20	3.00
1 – DM8094	TRI-STATE 4 x Buffer	144	.71
		2834	150.05
			$9.38/Channel

Table 2. Microprocessor System Characteristics

	8080	PACE	6800	SC/MP
Address Word Length	16-bit	16-bit data/address bus	16-bit	12- or 16-bit
Data Word Length	8-bit		8-bit	8-bit
Address & Data Polarity	All chips are 1 = true; however, if Intel system bus drivers and receivers are used, 8080 system data and address bits are 0 = true.			
Address Strobe	None	NADS = 0 to set memory address latches	VMA = 1 (concurrent with)	NADS = 0
Memory Read Strobe	MRDC = 0 to read data	IDS = 1 to input data	R/W = 1 to read data	NRDS = 0 to read data
Maximum Clock Rate	2MHz	2MHz	1MHz	1MHz

Since μC systems differ somewhat from one another, it is worth our effort to look at the hardware and software details and the system timing requirements of several of them when considering a DAU interface. From this consideration we can establish the desired function and characteristics of the ADCs, DACs, address decoders, control components, and μC interface signals. The following exercises include interfacing parallel conversion DAUs of 8- and 12 bits to the Intel 8080, the National PACE, and the Motorola 6800 microcomputer systems. Interface to other systems such as National's SC/MP will be similar. All request, control, and answer signals are considered along with the required signal polarities and timing relationships. Table 2 summarizes the important characteristics of these three systems.

8080 Interface

The 16-channel, 8-bit parallel-conversion DAU shown in Figure 6 will interface with an 8080 μC system without a wait period in the memory-read cycle. This system can be built with existing components for about $10 per channel. It is a minimal system, capable of driving only a lightly loaded data bus, as the MM5357 ADCs can drive but a single TTL load. When heavier loads must be driven, two quad TRI-STATE output buffers will be needed. The address decoding uses a 4-line to 16-line decoder which selects the addressed channel from the four least significant (LSB) of address bits. A 6-bit address comparator compares the six most significant (MSB) address bits with a code hard-wired into the code-select-header. The comparator output gates the 4:16 decoder only if the proper memory page (1 of 64) is addressed. The comparator output, gated by the memory read command $\overline{\text{MRDC}}$, inhibits the clock to prevent data change in the output latches during the data access period. Concurrence of the correct address and $\overline{\text{MRDC}}$ also returns a data-ready acknowledgement to the μC via the TRI-STATE output of a buffer. No other logic is required; however, inverters are necessary in the ADC enable lines due to a sense mismatch in the 4:16 decoder output and the ADC enable inputs. The system is truly as uncomplicated as indicated in Figure 2.

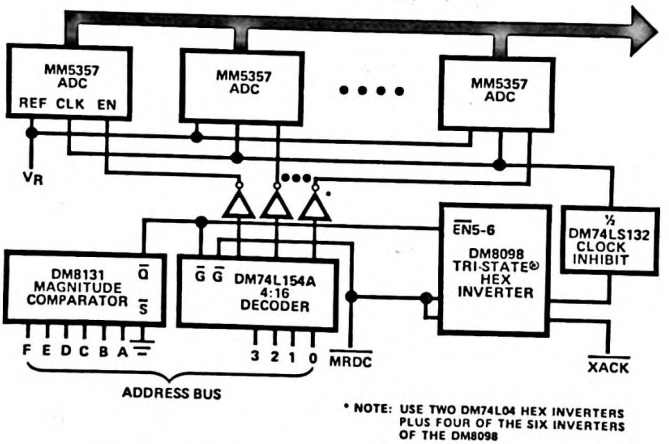


FIGURE 6. 16-Ch, 8-Bit Parallel-Conversion DAU for 8080

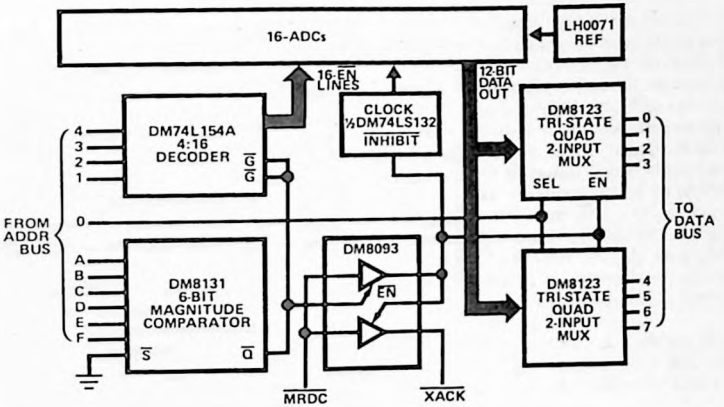


FIGURE 7. 16-Ch, 12-Bit Parallel-Conversion DAU for 8080

As 12-bit data is likely of greater interest in the market, the remainder of the discussion will consider the logic necessary to handle 12-bit data. Accordingly, Figure 7 shows a 16-channel, 12-bit parallel-conversion DAU for the 8080. No part number designation appears on the ADCs because they are hypothetical units possessing the characteristics considered desirable in this application. The converters contain the DAC switches, ladder network, comparator, up/down counter (for tracking conversion), control logic, and TRI-STATE buffered outputs. They operate continuously with the output data buffer updated at the end of each conversion. Such a converter containing CMOS logic could settle in less than 1-4 μs (after an initial but longer acquisition period) without being costly to construct, and would thus provide 12-bit accuracy to ±½ LSB at a data bandwidth of 10-20 Hz. A single external buffered reference could suffice for all converter channels. An external gated clock could drive all converters. Address decoding is the same as outlined for the 8-bit system. The LSB address bit is used to select byte 1 or byte 2 of the 12-bit output data word by means of the two DM8123 quad, TRI-STATE, 2-input multiplexers. Address bits 1-4 are decoded into 1-of-16 select bits to enable the TRI-STATE output of the selected ADC. Since the 1-of-16 output select of the DM75L154A decoder is 0 true, it is desirable that the ADC enable input be 0 true. Otherwise, 16 inverters would be required. The control timing may be considered in reference to the 8080 timing requirements shown in Figure 8.

The DM8131 address comparator provides an output to gate the 4:16 decoder and to enable the DM8093 quad TRI-STATE line driver. This occurs (+30 ns) only if the address is valid for this data card. If the address is valid, the 4:16 decoder accepts the address and the DM8093 is set to accept the MRDC command at inputs 5 and 6 (+250 ns). The decoder output to the ADC enable lines is available (+180 ns), and valid data is available from the selected ADC (+330 ns). As the data card must return a data ready signal (+440 ns) to prevent extending the memory access cycle, the DM8093 transmits the $\overline{\text{MRDC}}$

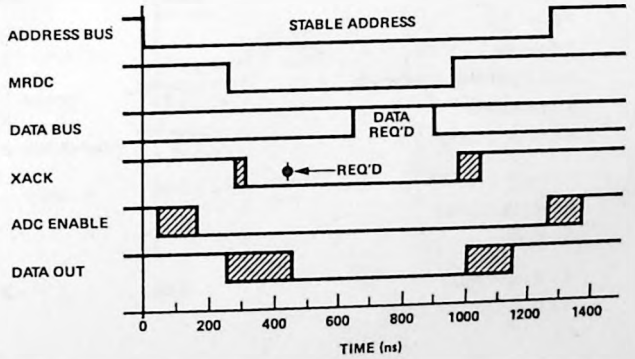


FIGURE 8. Timing and Control for 8080

back out to the μC on the XACK line (+300ns) in advance of the time required. A 0 is placed on the XACK line for the duration of the MRDC command. The MRDC signal also enables the output multiplexer enable lines (+300ns) via the DM8093. This signal also interrupts the clock drive to the ADCs to prevent a change in data output during the remainder of the memory read cycle. A desirable built-in design feature of the ADC for this application might be a clock inhibit or data transfer inhibit operating from the $\overline{EN}$ input. Valid data is present on the data bus (+460ns) at least 200ns before it is required. Valid data remains stable until the end of the MRDC command when XACK and data output lines return to their normal high-impedance states.

Data is placed on the data bus in two 8-bit bytes as controlled by the LSB address code. A 0 selects the 8 LSB data, and a 1 selects the MSB data. Two consecutive memory addresses will then read the entire data word in two bytes. As there are only 12 data bits, zeros are placed on the remaining data lines. For 2s complement binary data coding of ± input analog signals, the 12th bit would be inverted and extended to the remaining data lines so that signals would appear as valid data to the microprocessor.

Total address decode, control, clock, and output drive logic circuitry is contained in six DIP circuits (only one of 24 pins). To this must be added a code-select header, a reference, and 16 converters. Total power required is 4.2 watts for 16 channels of 12-bit data from ±5V analog signals of 10Hz bandwidth (see Table 3). Low Power TTL output drive capability would reduce power drain by 370mW. Total cost of parts (assuming a future price of $25/ADC) would run to about $26 per channel (see Table 4).

Table 3. Power Required, 16-Channel, 12-Bit

			P_D (mW)	
		8080	6800	PACE
16 –	ADC		3200	
1 – LH0071	Reference		45	
1 – DM74LS132	4 x 2-Input NAND Schmidt		60	
1 – DM74L154A	4:16 Decoder		24	
1 – DM8131	6-Bit Comparator		250	
1 – DM8093	4 x Buffer	170		
or 1 – DM8099	6 x NAND Buffer		175	
or 3 – DM8097	6 x Buffer			975
2 – DM8123	4 x 2-Input MUX	400	400	
or 1 – DM86L13	4 x D-Latch			30
		4199	4154	4584

Table 4. Cost of Components, 16-Channel, 12-Bit

			$ (100s)	
		8080	6800	PACE
16 –	ADC		400.00	
1 – LH0071	Reference		5.00	
1 – DM74LS132	4 x 2-Input NAND Schmidt		2.00	
1 – DM74L154A	4:16 Decoder		2.46	
1 – DM8131	6-Bit Comparator		2.56	
1 – DM8098	6 x Inverter	1.65		
or 1 – DM8099	6 x NAND Buffer		1.70	
or 3 – DM8097	6 x Buffer			5.55
2 – DM8123	4 x 2-Input MUX	2.56	2.56	
or 1 – DM86L13	4 x D-Latch			1.28
		416.23	416.28	418.85
			≈ $26/Channel	

6800 Interface

For other μC systems, the logic will change slightly. Figure 9 shows the logic section of the DAU of Figure 7 modified as necessary to interface with the 6800 μC. The 6800 timing and control signals are shown in Figure 10. With the 6800, the address information, the valid memory address VMA signal, and the read/write W/R signal all come up approximately simultaneously and remain for about one clock period of 1μs (min.). The data need not appear on the data bus until 100ns thereafter. The valid address decoding is accomplished by ANDing the VMA and R/W signals together in a TRI-STATE 2-input AND gate. When enabled by the comparator output, this gate returns a READY signal to the μC and enables the output multiplexers. The appropriate data byte is selected by the LSB address bit as with the 8080 system. The necessary 10ns data hold time is provided by the ADC and output multiplexer disable delays. The remainder of the DAU is identical to that of Figure 7. Cost and power required are also similar to those of the 8080 system interface.

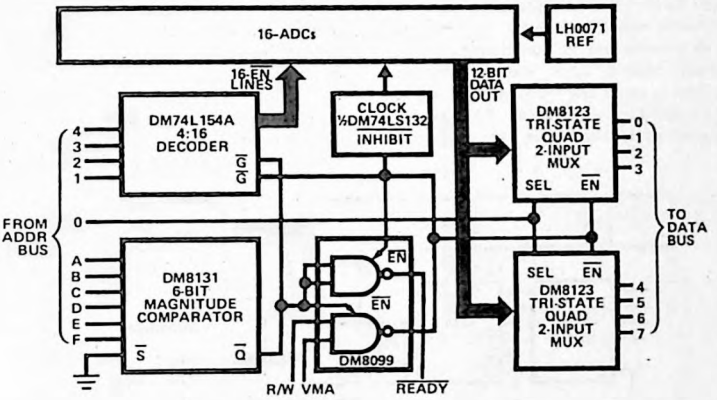


FIGURE 9. 16-Ch, 12-Bit Parallel-Conversion DAU for 6800

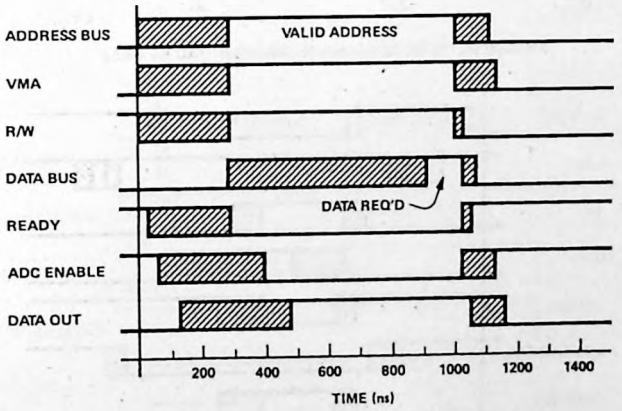


FIGURE 10. Timing and Control for 6800

PACE Interface

Figure 11 shows the logic section of the DAU of Figure 7 modified to interface with a PACE μC. The PACE timing is shown in Figure 12. Since the PACE μC has but a single address/data bus, address latches are required for address decoding. The DM8131 address comparator contains output latches, but the DM74L154A 4:16 decoder does not, so a quad latch is inserted ahead of the 4:16 decoder. The latches all set on the rising edge of the NADS signal provided by PACE during the time that address information is on the bus, and drop out on the next NADS signal. Comparator output applied to gate the 4:16 decoder provides an enable ADC signal lasting until the falling edge of the next NADS pulse. The IDS signal ANDed with the comparator output enables the TRI-STATE output buffers and inhibits the clock. An additional MSB inverter would be needed for ± analog signals in order to provide the 2s complement code. Total address decode, control, clock, and output drive circuitry is contained in seven DIP packages, one more than required for the 8080 system interface. Total power and cost are comparable to those given for the 8080 system interface.

ADC CHARACTERISTICS

The ADC for use on a parallel-conversion DAU must contain TRI-STATE output data latches. Otherwise it may be conventional. The MM5357 was designed for direct connection to a data bus, therefore it contains the necessary output latches. At this writing there are other ADCs with the TRI-STATE output latches appearing on the market, and more can be expected. The MM5357 is nearly ideal for use in an 8-bit parallel-conversion DAU. It would be even more suitable to this use if it were a tracking converter, and the polarity of its enable input and of its data output were of opposite polarity. The data polarity is of lesser importance as the bus drivers probably needed may as well be inverting as non-inverting except for common usage. The enable polarity should match the decoder output to obviate the need for 16 inverters (3 logic packages, though of little cost). See the later discussion of ADC hardware for additional thoughts on this subject.

This parallel-conversion data system has data bandwidth limited to about 10 Hz for 8-bit SAR converters, but may be increased to 150-300 Hz with 8-bit tracking

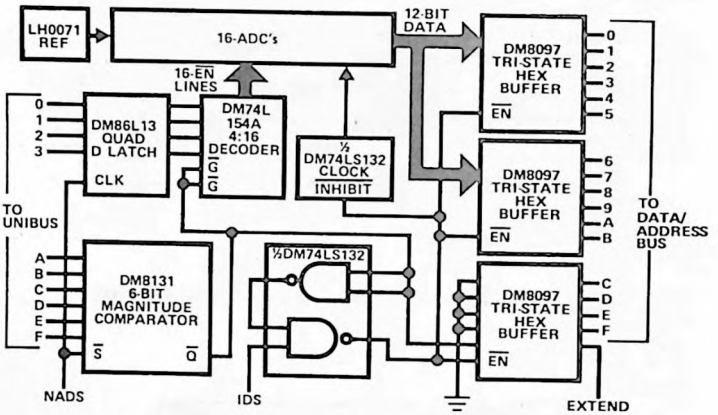


FIGURE 11. 16-Ch, 12-Bit Parallel-Conversion DAU for PACE

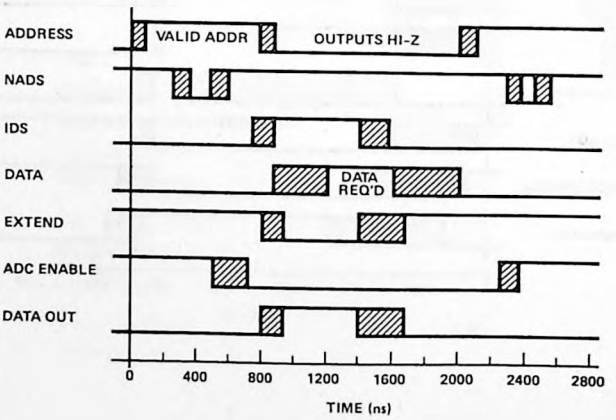


FIGURE 12. Timing and Control for PACE

converters. 12-bit data bandwidth will be 1/16 that of the 8-bit systems. On the other hand, no S&H module is required. Data rates could be considerably increased if S&H modules were added to each channel; however, costs per channel would more than double. For use with S&H modules, SAR logic converters would be faster than tracking types, allowing data bandwidths of over 600Hz/channel for 12-bit data.

MULTIPLEXED DATA ACQUISITION UNIT WITH MEMORY

A multiplexed data acquisition system containing memory is probably the most cost-effective way of providing an immediate data-access interface to processors. The processor may address the peripheral data-acquisition unit to obtain immediate data without entering a wait mode, just as if it were accessing main memory. Latest valid data is always present within the DAU memory which is updated at a rate determined by the channel multiplexer rate and ADC conversion speed. There is no need to write subroutines into processor software or firmware to address and request data from the peripheral, resume its assigned processing task while watching for a flag set by the peripheral indicating that data is ready, and returning to accept data from the peripheral.

The multiplexed DAU with memory shown in Figure 3 takes care of routinely updating its memory by sequentially sampling each data channel, digitizing the channel signals, and writing data into its self-contained memory. When the DAU is interrogated, the sequential process is momentarily interrupted, the RAMs are addressed by the processor, and data is read out to the data bus. The memory can be three each DM8599 16x4-bit RAMs. These have TRI-STATE outputs, so can connect directly to the data bus. Note that the RAM inverts the data bits from the ADC. The RAMs are available in low-power TTL to drive a lightly loaded data bus, or they are available in Schottky versions for driving higher speed systems. In fact, almost the entire logic system could be realized in Schottky circuits, which should allow interfacing even the new fast bipolar μCs without a wait cycle.

The MUX sequencing circuits are shown in Figure 13. When the μC is not accessing memory on the DAU, the 16 data channels are scanned in continuous sequence.

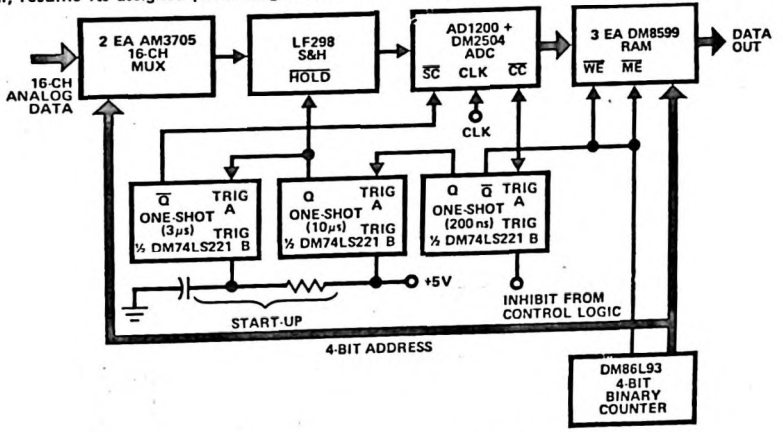


FIGURE 13. Sequencing Logic with OS

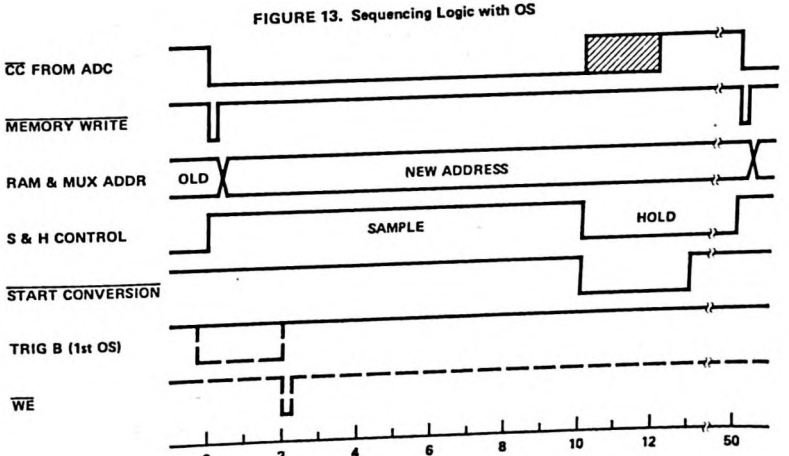


FIGURE 14. Timing for One-Shot Sequencing

Data on each channel is sampled and held in the S&H module while the ADC converts the analog data to digital. At the completion of conversion, the digital output of the ADC is written into the RAMs before the multiplexer selects the next channel. The timing and sequencing of channels is accomplished with a 4-bit binary (÷ 16) counter and three one-shot pulse generators. Where one-shots are undesirable, an alternate approach using shift register timing could provide the same function. A valid address output from the address comparator switches the RAM address input from the ÷16 counter to the address bus input, thereby addressing the RAM to the desired channel for data readout. If the data conversion sequence is in the memory write condition, the gate applied to WE prevents switching the MUX to the address bus or returning an XACK signal until the memory has been loaded. Thereupon, the sequence is interrupted as outlined above. The interruption of the sequence lasts for about 1300ns (8080 system) while the address is valid.

The sequential data conversion cycle is shown in the timing signals of Figure 14. The conversion-complete $\overline{CC}$ output of the ADC triggers a one-shot to generate a 200ns memory write pulse. The trailing edge of this pulse advances the address ÷16 counter to the next channel and triggers a second one-shot to produce a 10μs sample period. At the completion of the sample period, the S&H goes into hold mode and a third one-shot generates a 3μs start conversion $\overline{SC}$ pulse. When the DAU is in the command read mode, a 0 appears at B trigger input to the first one-shot. If a $\overline{CC}$ signal occurs during the time the 0 is present on the B input, the one-shot will not be triggered until the B input returns to a 1.

An alternate sequencing circuit without one-shot circuits is shown in Figure 15 with timing relationships in Figure 16. It makes use of a shift register and exclusive-OR gates to generate the gates needed to write into memory, sample and hold, and start conversion. The ADC clock is generated at twice the desired clock frequency and divided by 2 in a D flip-flop. In this manner, the minimum gate width is 1/4 of the ADC clock period (620ns in this example). The $\overline{CC}$ signal is clocked into a D flip-flop with a delay of 620ns. The delayed output clears the shift register (SR) and is clocked into the SR after an additional 620ns delay. An exclusive-OR of the SR input and Q1 output generates a 620ns gate to write data into the RAMs. The trailing edge of this $\overline{WE}$ gate clocks the ÷16 counter to advance the MUX and RAM address to the next channel. Exclusive-ORing of SR Q1 and Q7 produces an 8.75μs sample gate. (If the acquisition and settling time of the S&H is greater than 8.75μs, additional circuit complexity is required.) Exclusive-ORing of Q7 and Q8 produces a synchronized 1.25μs gate to start the ADC. This circuit may not be the most versatile or elegant for the purpose. For those applications with longer S&H acquisition times or other requirements, some alternate circuit may be designed if that of Figure 15 is unacceptable.

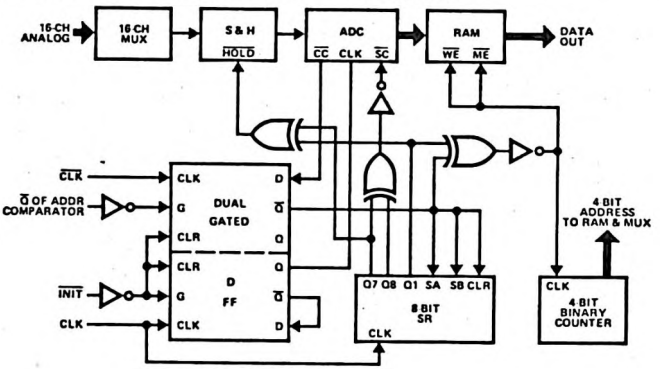


FIGURE 15. Sequencing Logic with SR

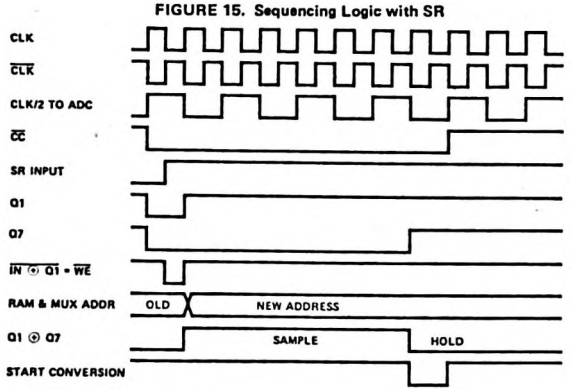


FIGURE 16. Timing for S-R Sequencing

The μ-computer interfaces shown in Figures 17 and 18 are similar to that of Figure 5. The PACE interface is seen to be slightly less complex than that of Figure 17 for 8-bit data-bus machines. A single DAU card with plug-in or strap options could be built to interface any of the three μCs considered. Such a universal circuit is shown in Figure 19. This circuit also includes an option to provide binary output for unipolar analog signals or complementary binary output for ± signals. In the case of binary output, the 13-16th data bits are set to 0. In the case of complementary binary, the sign bit is extended to the 13-16th data bits for valid recognition by the μC.

The total dissipation is 3.5 watts and cost is $11 per channel as shown in Table 5. Both are only slightly greater than those for the conventional DAU.

The ADC desired for this application is similar to the conventional ADC except that the ADC data output should be complementary to compensate for the data inversion within the RAMs. The AD1210 or AD1200 are thus ideal choices for an ADC in the multiplexed DAU with memory.

CONVERTER CHARACTERISTICS

Each approach to the DAU requires different characteristics of the ADC. Table 6 summarizes the requirements for each of the three DAU types. The sequential or addressed DAU types require similar ADCs. If the conventional addressed DAU must utilize bus drivers, the desired ADC characteristics are identical to those for the sequential DAU with memory. Only the parallel-conversion DAU is seen to require buffered TRI-STATE output latches.

By far the most important characteristic of an ADC for use in a parallel-conversion DAU is that it have buffered TRI-STATE output latches. It is desirable that it also have the other characteristics checked in Table 6. Items 1 and 2 are by far the most important of the desired characteristics. The need for item 1 has been discussed. TTL compatible control and data signals are desirable so that TTL-MOS and MOS-TTL interface buffers are not required between the ADC and the rest of the system. Dual output strobing makes it possible to wire-OR interface directly to an 8-bit data bus or to use only an 8-line buffer without the need for the output multi-

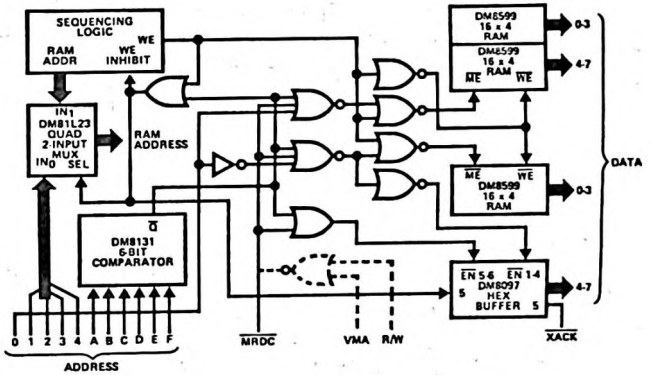


FIGURE 17. Address Comparator and Control for 8080 (6800)

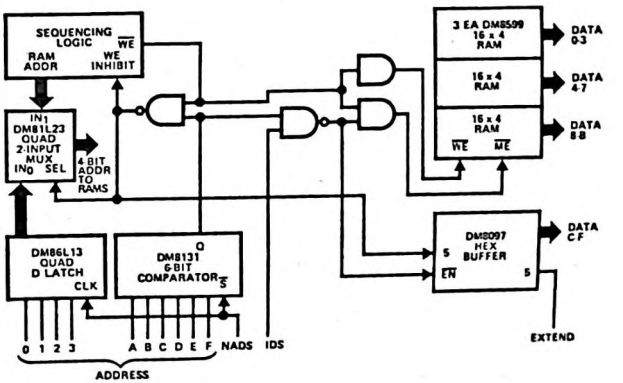


FIGURE 18. Address Comparator & Control for PACE

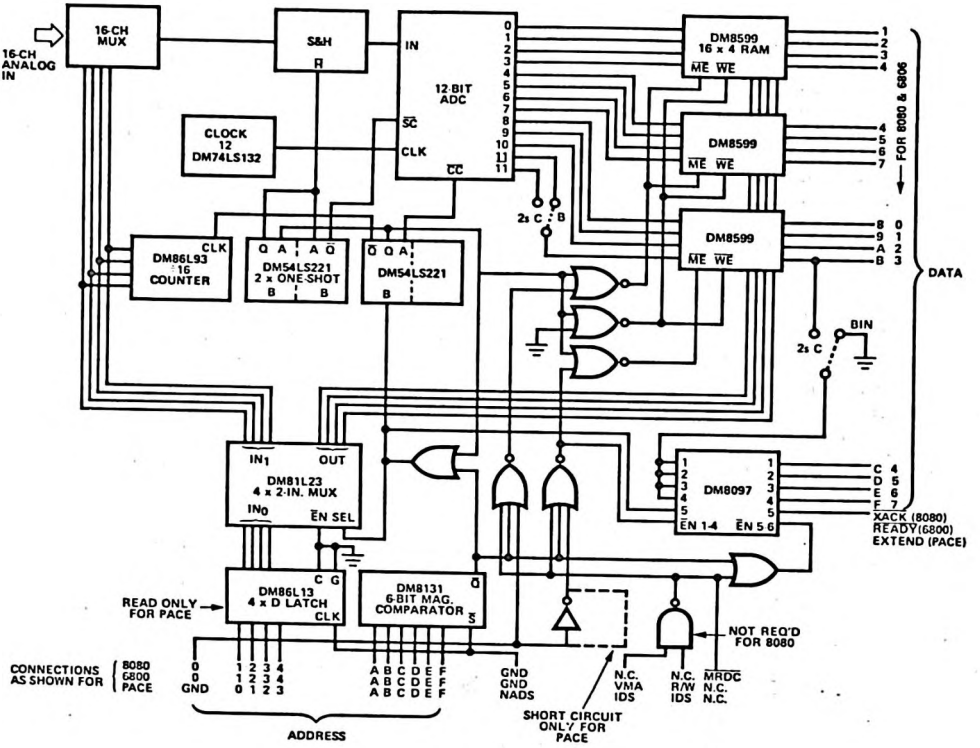


FIGURE 19. Multiplexed Immediate-Data-Access DAU

Table 5. Power & Cost, 16-Channel, 12-Bit Sequential with Memory

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
1 – LH0070	Reference	45	5.00
3 – DM8599	256-Bit RAM	1200	15.36
1 – DM8097	6 x Buffer	325	1.65
1 – DM8131	6-Bit Comparator	250	2.56
1 – DM81L23	4 x 2-Input MUX	20	2.00
1 – DM74LS27	3 x 3-Input NOR	17	3.00
1 – DM7402	4 x 2-Input NOR	55	.35
1 – DM74L32	4 x 2-Input OR	12	.64
1 – DM86L93	÷16 Counter	25	2.11
2 – DM74LS221	2 x One-Shot	60	6.00
1 – DM74LS132	4 x NAND Schmidt	60	2.00
1 – DM86L13	4 x D-Latch	30	1.28
		3500	176.00
			$11/Channel

plexers shown in Figure 5 et. al., although a separate buffer is required in most systems. Tracking operation provides the higher speed useful in a conversion circuit without an S&H. Inhibiting data transfer to output data latches when the output is enabled prevents changing the output code while data is being read from the data bus. This function can be accomplished with an external gate, but could be convenient if handled within the ADC logic. Straight binary (not complemented) output is desired for all μC interfaces (except the 8080 when operating with Intel system bus drivers and receivers). As it may be necessary to add TRI-STATE line drivers to drive the data bus, data inversion can be handled by inverting buffers when required. The availability of both Q and $\overline{Q}$ outputs on the MSB simplifies data readout as binary or 2s complement without adding an external inverter. Table 6 has been arranged in the approximate order of preference for parallel-conversion DAU use; the preference will be different for multiplexed data.

The National MM5357 is the choice for an 8-bit ADC having buffered TRI-STATE output latches and TTL compatibility when converting ±5 or 0-5V analog inputs. If converting 0-10V inputs, it becomes 10V CMOS compatible. Several monolithic ADCs of 8 to 12 bits have been announced. These monolithic converters and future versions of them promise to bring converter prices down to a level which will make parallel-conversion economically feasible. Several hybrid converters have also been announced with attractive prices; however, it is the monolithics which promise the lowest ultimate cost. Features of several of these new products are compared in Table 7. Although only the MM5357 and the AD7550 are suitable in present form, their prices and characteristics show that the desired attributes are and will be possible at the needed prices.

The future ADC most suited for use in a parallel-conversion DAU might appear as in Figure 20. This

Table 6. Desired A/D Converter Characteristics

	Parallel Conversion	Sequential w/ Memory	Addressed w/o Memory
Buffered TRI-STATE Output Data Latches	x		?
TTL-Compatible Control & Data Signals	x	x	x
Dual Output-Enable (Bits 0-7 & Bits 8-11)	x		x
Counter Logic	UP/DN	SAR	SAR
Internal Comparator	x	x	x
Both Q & $\overline{Q}$ Outputs on MSB	x	x	x
Binary Output Polarity	Data*	$\overline{\text{Data}}$	Data*
Busy Output (TRI-STATE w/ Enable)	?		x
Internal Clock		x	x
Continuous Recycle when CC = SC	x		
Inhibit Data XFR to Latches when Enabled	x		

* Unimportant if Buss drivers used.

Table 7. Low-Cost Monolithic and Hybrid ADCs

	National MM5357	Analog Devices AD7570L	Teledyne 8702	National AD1210 (Hybrid)	Analog Devices AD7550
Number of Bits	8	10	12	12	13
Cost (in 100s)	$7.95	$69.00 (1-49)	$29.50	$24.95	$25.00
Conversion Method	Potentiometric	R-2R	Differential Charge Balancing	R-2R	Integrating
Logic Type	PMOS SAR	CMOS SAR	CMOS Integrating	CMOS SAR	CMOS Quad Slope
Conversion Time	25μs	20μs + Comp. Settling	20ms	130μs	40ms
Logic Interface at 5V Analog Sig. 0-10V	TTL CMOS	TTL TTL/CMOS	TTL TTL	TTL CMOS	TTL TTL/CMOS
External Circuits Required	Ref + Clock	Ref + Comparator	Ref	Ref + Clock	Ref
Output Buffered Latch?	Yes	No	Yes	No	Yes
TRI-STATE Output?	Yes	Yes	No	No	Yes
Separate Output Enables?	NA	Yes	Not Strobed	No	Yes
Output Code	Inverted	Normal	Normal	Inverted	2s Complement
Power Dissipation	170mW Dynamic	10mW Standby + Dynamic + Comparator	20mW Dynamic	140mW Dynamic	10mW Dynamic

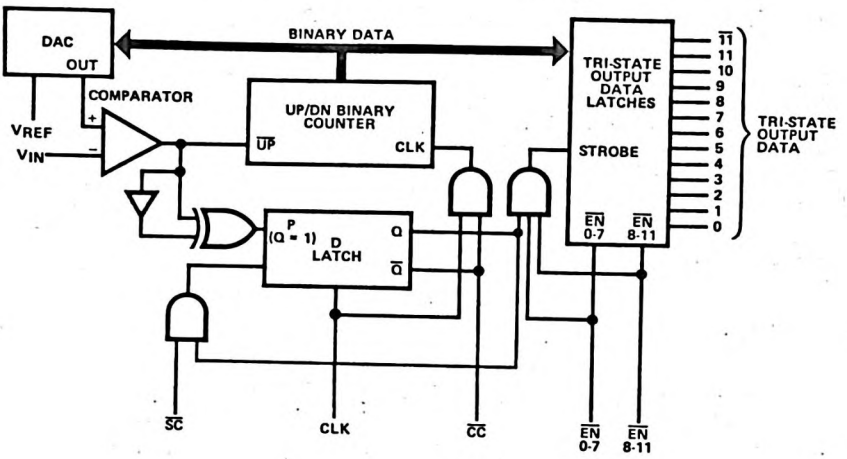


FIGURE 20. Tracking ADC for Parallel-Conversion DAU

design meets all the goals of Table 6. It could run at a clock rate of 0.25-1 MHz (1-4 μs conversion time) because it is a tracking converter, it contains TRI-STATE buffered output data latches, the separate high and low bit-enable lines allow two-byte operation of an 8-bit data bus, the output latches will not change state when the output is enabled, and the $\overline{CC}$ and $\overline{SC}$ terminals may be strapped for continuous conversion without missing a clock period. An 8- or 10-bit converter and possibly a 12-bit converter of this type could be built on a single chip without much difficulty. If not, a hybrid or two-chip design is practical. Where speed is not of importance, monolithic 10- or 12-bit converters can be built with integrating or voltage-to-frequency conversion techniques. The integrating technique possibly allows the greatest accuracy with the least circuitry, and is a prime contender for the application. As the integrating ADC utilizes both linear and digital circuits, it is normally of multi-chip design. However, as technology advances, it will become increasingly practical to produce the low-drift, low-offset amplifiers, integrators, and current sources required of a 12-bit ADC on a single reasonably small chip along with the necessary logic.

A two-chip approach would likely be the choice today. We will certainly see some of these desired design features appearing on ADCs in the near future.

As far as ADCs and DACs are concerned, the entire makeup of their internal logic sections is different from that of conventional converters of today (except for the MM5357 and AD7550). Tables 6 and 8 outline the desired characteristics of ADCs and DACs for parallel-conversion and multiplexed systems. Figures 20 and 21 indicate the logic required. The ADC of Figure 20 is suitable for relatively high speed data acquisition without S&H circuits, while that of Figure 21 is suitable for slowly varying data only.

DATA DISTRIBUTION SYSTEMS

Until now, the discussion has centered entirely around the data acquisition end of the system. At first thought, the data distribution may seem almost trivial. However, there is still the address recognition and decoding plus the control functions. The conventional data distribution unit (DDU) has used a single DAC, a multi-channel analog demultiplexer, low-pass filters and possibly S&H

Table 8. Desired D/A Converter Characteristics

	Parallel Conversion	Multiplexed System
Hi-Z Digital Input Circuits	x	x
Strobed Data Input Latches	x	x
Dual Input Data Strobes (Bits 0-7 & Bits 8-11)	x	x
Optional Internal Inversion of MSB	x	x
Internal Output Amp & FB Resistors	x	?
Internal Reference	?	x

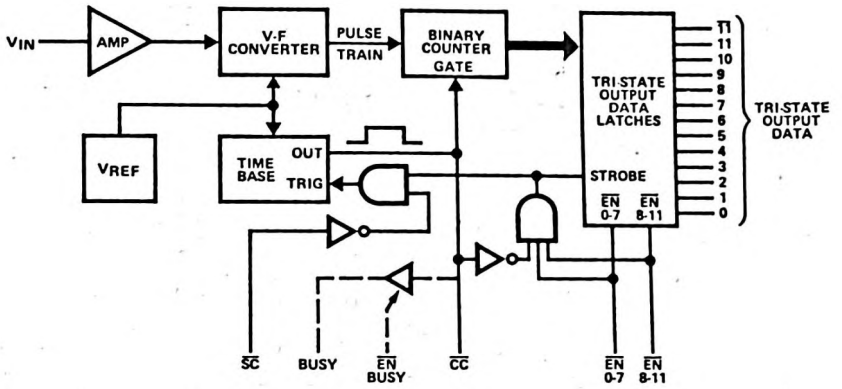


FIGURE 21. V-F ADC for Parallel-Conversion DAU

circuits on each channel reconverted to analog form. Such a system could benefit from a DAC with input data latches and separate (double-byte) input gating or strobing controls while a parallel-conversion DDU has even more need of these input characteristics.

The parallel-conversion DDU shown in Figure 22 would, if constructed with available DACs, require 12-bit input data latches ahead of each DAC. The characteristics desired of a DAC for this use are listed in Table 8. High impedance digital inputs prevent loading the data bus while a strobed input data latch allows entering data only in the addressed DAC and holding it until updated (thus performing the function of DAC and S&H). Separate input data strobes for low and high bits are used for the same reason as with the ADC, for alternate enabling on successive input data bytes. Figure 23 outlines the desired DAC for use in a parallel-conversion DDU.

The DDU address decoding and complexity is similar to that of the DAU. Input data strobing separated as 8 LSB and the remaining MSB is an advantage when used on 8-bit data bus systems. The cost per channel is essentially that of the DAC used. Likewise, for power dissipation. Practicality will be entirely dependent on ultimate cost of the converters. Advantages over a demultiplexed system are that only minimal output filters are required and that an output amplifier per channel is not required (already exists in each DAC).

CONCLUSION

Each type of DAU described exhibits unique advantages as indicated in the comparisons of Table 9.

Further reduction in the costs of monolithic converters will make the parallel-conversion type of DAU attractive where low-speed data is handled. For 8-bit data, this type of DAU is extremely attractive at this time because the DAU cost per channel is essentially that of an ADC which is as low as $8 in lots of 100.

It would seem that the multiplexed DAU with memory exhibits all of the advantages of the conventional random-addressed DAU plus all those of the parallel data conversion DAU except that the data in any specific channel may be older. Offsetting this single comparative disadvantage are significantly lower cost per channel, lower power requirements, and no requirement for special ADCs with buffered output latches. The multiplexed approach with memory is only slightly more complex or costly than a standard DAU, yet it brings the great advantage of high-speed immediate data access with significant cost savings over the parallel conversion technique.

Although the character of an ADC or DAC used in a parallel-conversion data system differs markedly from those used in the usual multiplexed data system, the processor interface requirements are similar or identical. The sense of μC bus control signals is of relatively minor importance so long as they are standardized among the several μC units available. Positive-true data and address signals are possibly a slight advantage over zero-true signals when TRI-STATE circuits are used. For the multiplexed system described, data inversion through the RAM would suggest the advantage of complementary binary output data from an ADC.

Conventional ADCs and DACs available today (except the MM5357 and AD7550) do not have the characteristics needed for parallel-conversion systems. However, this picture is changing as more units are designed for direct data bus interface. Fortunately, however, the multiplexed DAU with memory does not require the bus oriented type of ADC. There is at least one available DAC which includes the dual-strobed input data latches suggested for direct data bus interface; I would expect to see others appearing in future designs, both monolithic and hybrid.

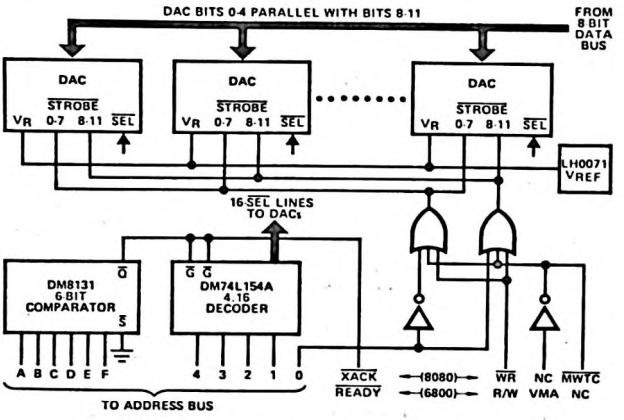


FIGURE 22. Parallel-Conversion DDU for 6800 or 8080

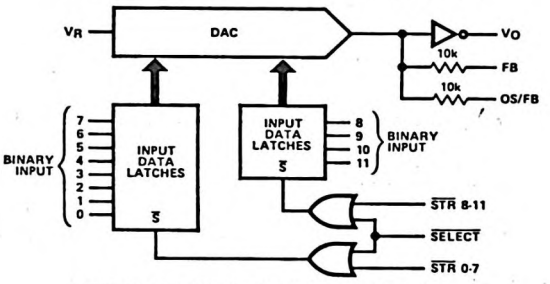


FIGURE 23. DAC for Parallel-Conversion DAU

Table 9. Comparison of Three Types of DAU

Features of DAU 16-Channel, 12-Bit	Conventional Random-Addressed	Parallel-Conversion Without S&H	Multiplexed With Memory
Approx. Component Cost (100s) (based on a $25 ADC)	$9.38	$26	$11
Approx. Power Dissipation	2.8W	4.3W	3.5W
Data Bandwidth/Channel t_{conv} = 50μs t_{acq} (S&H) = 10μs	200Hz	10Hz (tracking: t_{conv} = 4μs)	200Hz
Data Access Time	60μs	< 0.5μs	< 0.5μs
Software	60μs delay or subroutine and return on flag	as memory access	as memory access
Logic Interface Complexity	9 DIP	6 DIP	13 DIP
No. of IC Packages			
ADC Requirement		TRI-STATE buffered output data latches	

IC Voltage Reference has 1 ppm per Degree Drift

National Semiconductor
Application Note 161
Robert C. Dobkin
June 1976

A new linear IC now provides the ultimate in highly stable voltage references. Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50μV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

SUB SURFACE ZENER IMPROVES STABILITY

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N+ emitter diffusion is then made completely covering the P+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P+ and N+. Since the P+ is completely covered by N+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N+ and the other is to the P base diffusion. The current flows laterally through the base to the P+ or cathode of the zener. Surface breakdown does not occur since the base P to N+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

CIRCUIT DESCRIPTION

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two

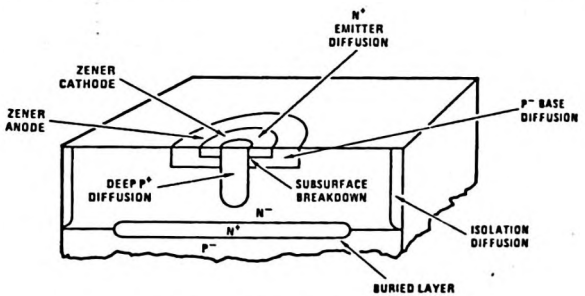


FIGURE 1. Subsurface Zener Construction

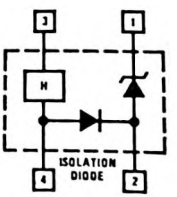


FIGURE 2. Functional Block Diagram

circuits is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the temperature stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3*. The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400μA to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500μA. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200μA. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120μA to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed Q1 and Q2. The Darlington is connected across th supply and initially draws 140 mA (set by current lim transistor Q3). As the chip heats, the turn on voltage fo Q4 decreases and Q4 starts to conduct. At about 90° the current through Q4 appreciably increases and le drive is applied to Q1 and Q2. Power dissipation decrease to whatever is necessary to hold the chip at the stabiliz tion temperature. In this manner, the chip temperatur is regulated to better than 2°C for a 100°C temperatur range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13 Transistor Q13 drives two buffers Q12 and Q11. Externa current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250μA by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

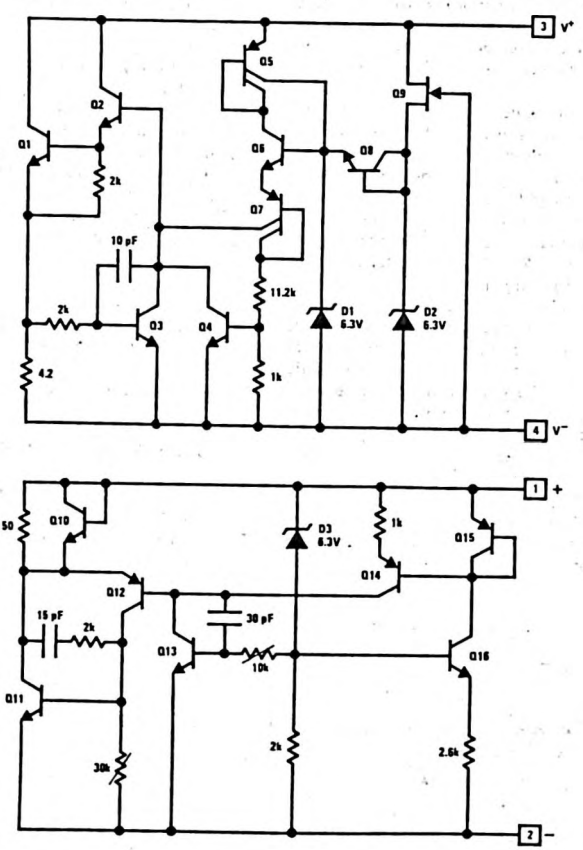


FIGURE 3. Schematic Diagram of LM199 Precision Reference

PERFORMANCE

A polysulfone thermal shield, shown in *Figure 4,* is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

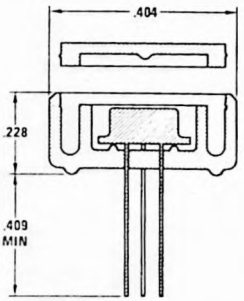


FIGURE 4. Polysulfone Thermal Shield

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6.* Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 00.7μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 mA ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 200 ppm) rather than the LM199.

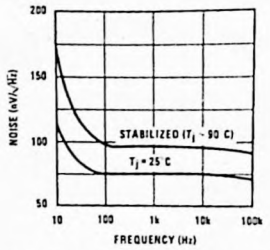


FIGURE 5. Wideband Noise of the LM199 Reference

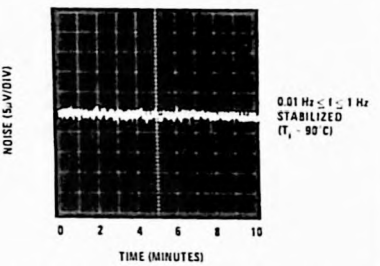


FIGURE 6. Low Frequency Noise Voltage

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7.* This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in Table I.

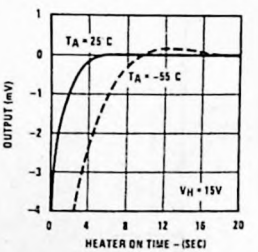


FIGURE 7. Fast Warmup Time of the LM199

Table I. Typical Specifications for the LM199

Reverse Breakdown Voltage	6.95V
Operating Current	0.5 mA to 10 mA
Temperature Coefficient	0.3 ppm/°C
Dynamic Impedance	0.5Ω
RMS Noise (10 Hz to 10 kHz)	7μV
Long-Term Stability	≤ 20 ppm
Temperature Stabilizer Operating Voltage	9V to 40V
Temperature Stabilizer Power Dissipation (25°C)	300 mW
Warm-up Time	3 Seconds

APPLICATIONS

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the $\overline{V}$.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 8* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10μA) results in a reference change of only 5μV. *Figure 9* shows reverse voltage change with current.

Biasing current for the reference can be anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation

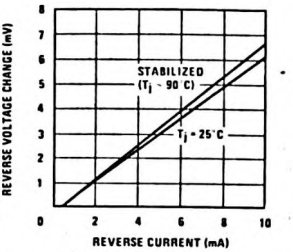


FIGURE 9. The LM199 Shows Excellent Regulation Against Current Changes

is better than discrete zeners. For optimum regulation, lower operating currents are preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8μV/°C, this is an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a −55°C to +125°C temperature

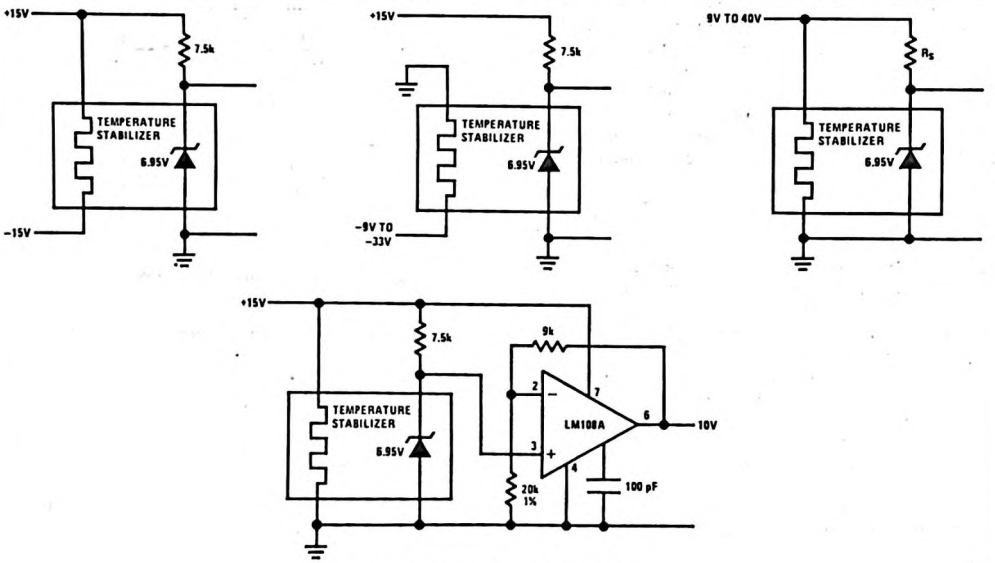


FIGURE 8. Basic Biasing of the LM199

range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also cause errors. The kovar leads from the LM199 package form a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30μV. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15μV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10μV to 20μV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10μV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

Figure 11 shows a standard cell replacement with a 1.01V output. A LM321 and LM308 are used to minimize op amp drift to less than 1μV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6μV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

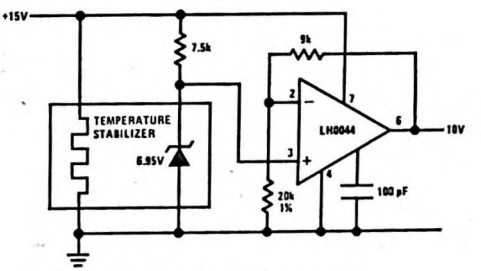


FIGURE 10. Buffered 10V Reference

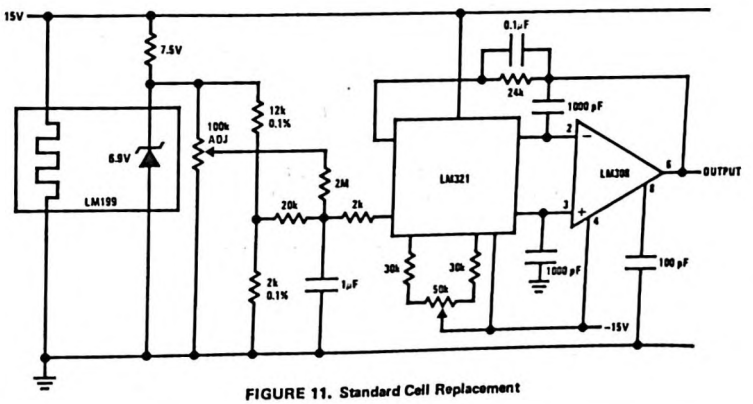


FIGURE 11. Standard Cell Replacement

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12*. The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13*. The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5μA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14*. The reference is biased from the ±15V input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

CONCLUSIONS

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

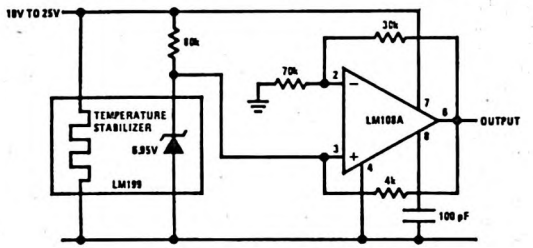


FIGURE 12. Wide Range Input Voltage Reference

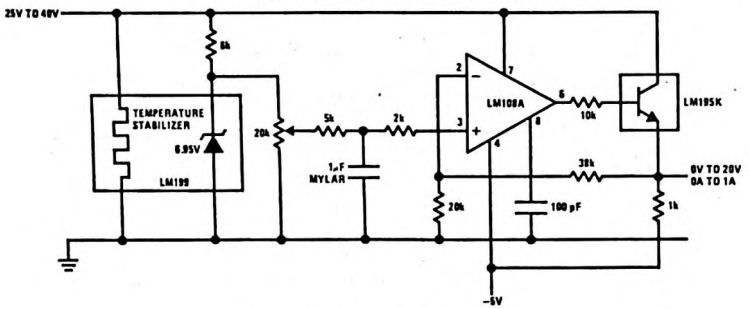


FIGURE 13. Precision Power Supply

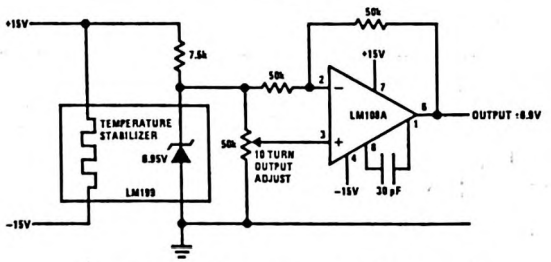


FIGURE 14. Bipolar Output Reference

IC Zener Eases Reference Design

National Semiconductor
Application Note 173
Robert C. Dobkin
November 1976

description

A new IC Zener with low dynamic impedance and wide operating current range significantly simplifies reference or regulator circuit design. The low dynamic impedance provides better regulation against operating current changes, easing the requirements on the biasing supply. Further, the temperature coefficient is independent of operating current, so that the LM129 can be used at any convenient current level. Other characteristics such as temperature coefficient, noise and long term stability are equal to or better than good quality discrete Zeners.

The LM129 uses a new subsurface breakdown IC Zener combined with a buffer circuit to lower dynamic impedance. The new subsurface Zener has low noise and excellent long term stability since the breakdown is in the bulk of the silicon. Circuitry around the Zener supplies internal biasing currents and buffers external current changes from the Zener. The overall breakdown is about 6.9 V with devices selected for temperature coefficients.

The Zener is relatively straightforward. A buried Zener D1 breaks down biasing the base of transistor Q1. Transistor Q1 drives two buffers Q2 and Q3. External current changes through the circuit are fully absorbed by the buffer transistors rather than by D1. Current through D1 is held constant at 250 μA by a 2k resistor across the emitter base of Q1 while the emitter-base voltage of Q1 nominally temperature compensates the reference voltage.

The other components, Q4, Q5 and Q6, set the operating current of Q1. Frequency compensation is accomplished with two junction capacitors.

All that is needed for biasing in most applications is a resistor as shown in figure 2. Biasing current can be anywhere from 0.6 mA to 15 mA with little change in performance. Optimally, however, the biasing current should be as low as possible for the best regulation. The dynamic impedance of the LM129 is about 1 Ω and is independent of current. Therefore, the regulation of the LM129 against voltage changes is 1/Rs.

Lower currents or higher Rs give better regulation. For example, with a 15 V supply and 1 mA operating current, the reference change for a 10% change in the 15 V supply is 180 μV. If the LM129 is run at 5 mA, the change is 900 μV or 5 times worse. By comparison, a standard IN821 Zener will change about 17 mV. All discrete Zeners have about the same regulation since their dynamic impedance is inversely proportional to operating current.

If the Zener does not have to be grounded, a bridge compensating circuit can be used to get virtually perfect regulation, as shown in figure 3. A small compensating voltage is generated across R1, which matches the dynamic impedance of the LM129. Since the dynamic impedance of the LM129 is linear with current, this circuit will work even with large changes in the unregulated input voltage.

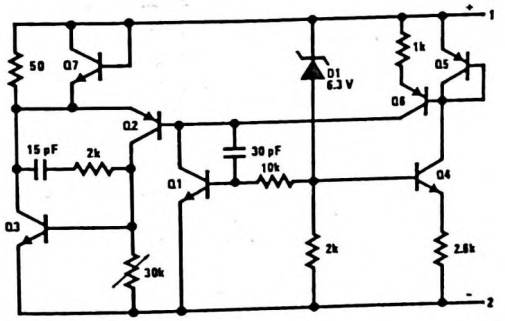


FIGURE 1. IC Reference Zener

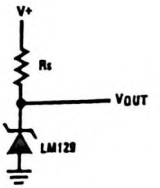


FIGURE 2. Basic Biasing

Other output voltages are easily obtained with the simple op-amp circuit shown in figure 4. A simple non-inverting amplifier is used to boost and buffer the Zener to 10 V. The reference is run directly from the input power rather than the output of the op-amp. When the Zener is powered from the op-amp, special starting circuitry is sometimes necessary to insure the output comes up in the right polarity. For outputs lower than the breakdown of the LM129 a divider can be connected across the Zener to drive the op-amp.

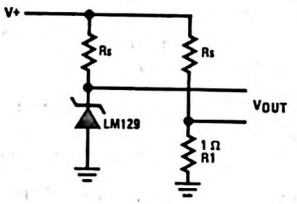


FIGURE 3. Bridge Compensation for Line Changes

An AC square wave or bipolarity output reference can easily be made with an op-amp and FET switch as shown in figure 5. When Q1 is "ON," the LM108 functions as a normal inverting op-amp with a gain of −1 and an output of −6.9 V. With Q1 "OFF" the op-amp acts as a giving 6.9 V at the output. Some non-symmetry will occur from loading change on the LM129 in the different states and mismatch of R1 and R2. Trimming either R1 or R2 can make the output exactly symmetrical around ground.

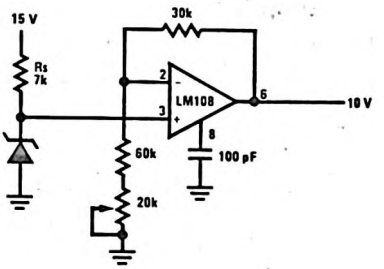


FIGURE 4. 10 Volt Buffered Output Reference

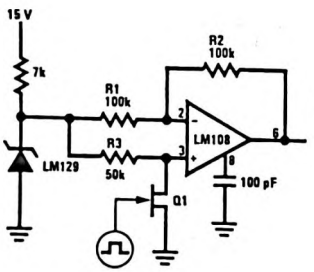


FIGURE 5. Bipolar Output Reference

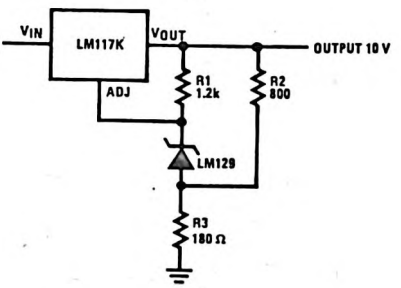


FIGURE 6. High Stability 10 V Regulator

By combining the LM129 with an LM117 three-terminal regulator a high stability power regulator can be made. This is shown in figure 6. Resistor R1 biases the LM129 at about 1 mA from the 1.25 V reference in the LM117. The voltage of the LM129 is added to the 1.25 V of the LM117 to make a total reference voltage of 8.1 V. The output voltage is then set at 10 V by R2 and R3. Since the internal reference of the LM117 contributes only about 20% of the total reference voltage, regulation and drift are essentially those of the external Zener. The regulator has 0.2% load and line regulation and if a low drift Zener such as the LM129A is used overall temperature coefficient is less than 0.002%/°C.

The new Zener can be used as the reference for conventional IC voltage regulators for enhanced performance. Noise is lower, time stability is better, and temperature coefficient can be better depending on the device selected. Further, the output voltage is independent of power changes in the regulator.

Figure 7 shows an LM723 using an external LM129 reference. The internal 7 V reference is not used and a single resistor biases the LM129 as the reference. The 5k resistor chosen provides sufficient operating current for the Zener over the 10 V to 40 V input voltage range of the LM723. Since the dynamic impedance of the LM129 is so low, the reference regulation against line changes is only 0.02%/V. This is small compared to the regulation of 0.1%/V for the LM723; however, the resistor can be replaced by a 1 mA to 5 mA FET used as a constant current source for improved regulation. When the FET is used reference regulation is easily 0.001%/V. Output voltage is set in the standard manner except that for low output voltages sufficient current must be run through the Zener to power the voltage divider supplying the reference to the LM723.

An overload protected power shunt regulator is shown in figure 8. The output voltage is about 7.8 V — the 7 V breakdown of the LM129 plus the 0.8 V emitter-base voltage of the LM395. The LM395 is an IC, 1.5 A power transistor with complete overload protection on the chip. Included on the chip are current limiting and thermal limiting, making the device virtually blowout-proof. Further, the base current is only 5 μA, making it easy to drive as a shunt regulator. As the input voltage rises, more drive is applied to the base of the LM395, turning it on harder and dropping more voltage across the series resistance. Should the input voltage rise too high, the LM395 will current limit or thermal limit, protecting itself.

The new IC Zener can replace existing Zeners in just about any application with improved performance and simpler external circuitry. As with any Zener reference, devices are selected for temperature coefficient and operating temperature range. Since the devices are made by a standard integrated circuit process, cost is low and good reproducibility is obtained in volume production.

Finally, since the device is actually an IC, it is packaged in a rugged TO-46 metal can package or a 3-lead plastic transistor package.

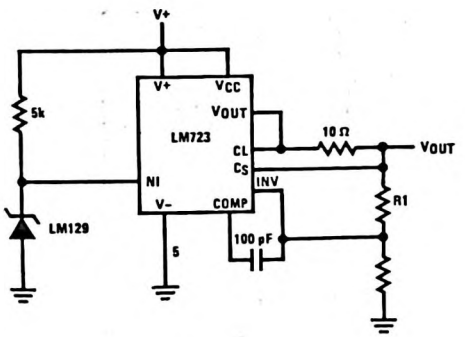


FIGURE 7. External Reference For IC

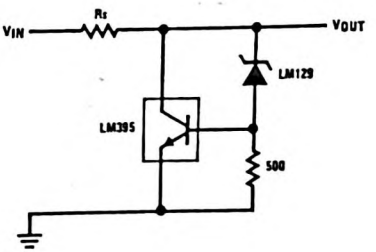


FIGURE 8. Power Shunt Regulator

A/D Converter Testing

National Semiconductor
Application Note 179
Dennis Dauenhauer
Doug Falco
April 1977

Attempting to test an analog-to-digital converter can be a challenging and rewarding experience. The recent increased interest in converter products has spawned renewed interest in test equipment dedicated to testing converters. Unfortunately, the broad range of converter products available makes testing by a single piece of equipment difficult at best.

A crude method of testing would be to monitor an analog signal at the converter input using a precision DVM and compare that with the converter output. This is simple enough to do, but in most cases this would prove impractical. For a 10-bit converter, this would require plotting 1,024 such readings. Automatic equipment can be used, but in all cases will require some sophisticated interface hardware and software routines. A person favoring auto test equipment can expect to pay around $10,000 for the hardware and at least that much for the software. What will be described is a method which costs a couple hundred dollars in components and which gives a device characteristic in a relatively short time period.

Because very little standardization has occurred for converter products, the user must adhere to the old adage "caveat emptor" or "buyer beware". The only universal statement that can be made for definitions of terms characterizing converter products is that they are universally inconsistent. For this reason, this application note will provide a simple method of providing a very graphic means of testing several of National's A/D converter products. It is also recommended that the reader refer to Application Note AN-156 for additional information concerning converter products definitions. Specific parameters which will be focused on in this paper are zero error, scale error, non-linearity error, differential non-linearity, monotonicity, total unadjusted error and quantizing error.

The block diagram of *Figure 1* shows the basic blocks of the complete test circuit of *Figure 2*. A storage scope is required to provide a continuous display. A Tektronix 7633 or equivalent is recommended. A typical characteristic for the ADC0800 shown in *Figure 3*.

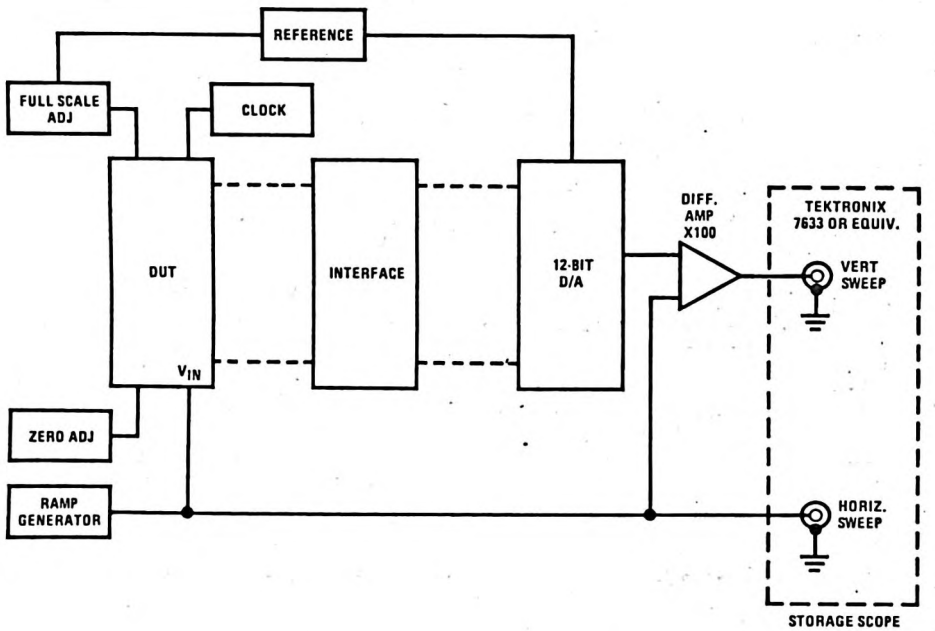
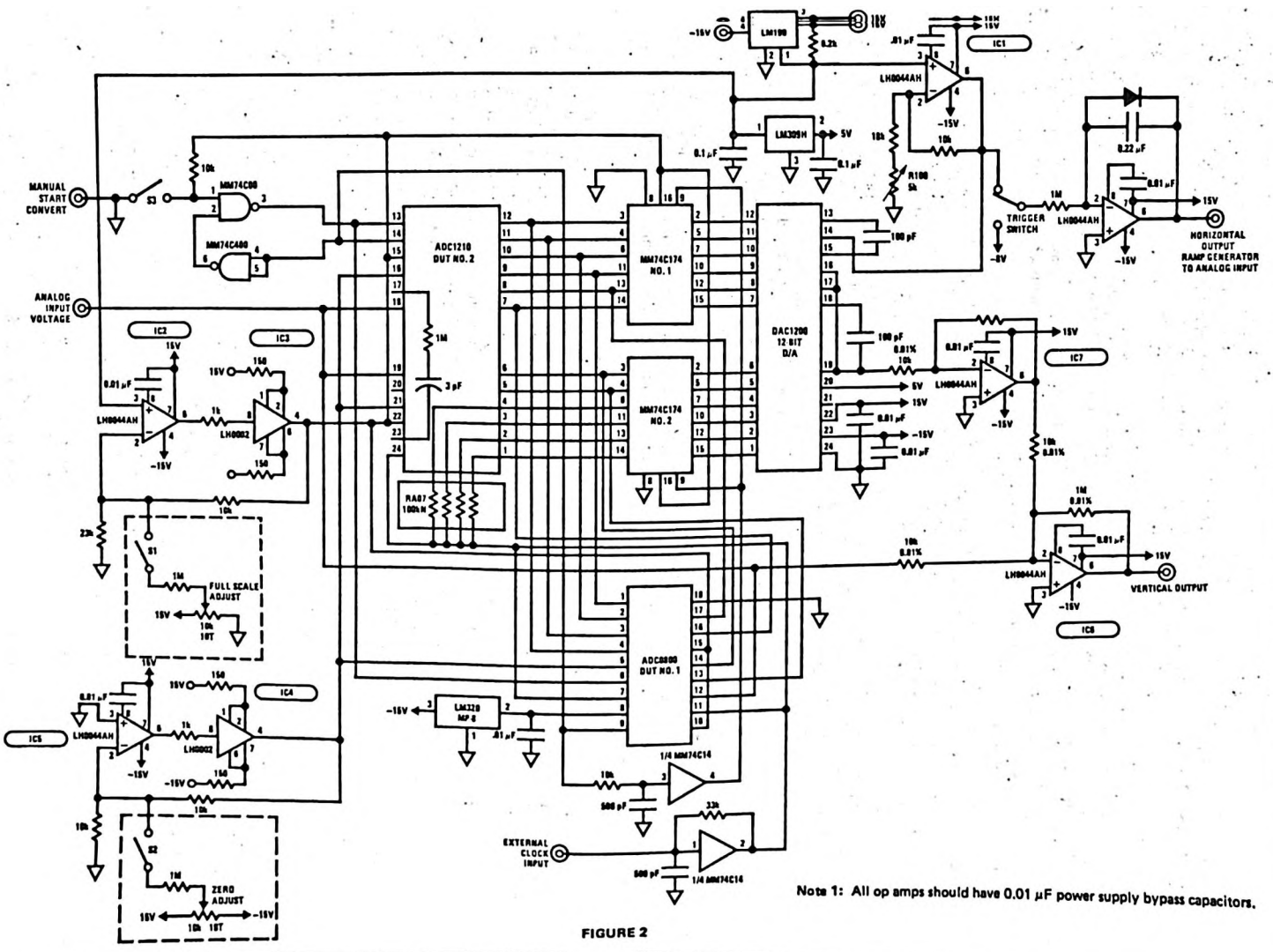


FIGURE 1. Block Diagram for A/D Tester



Note 1: All op amps should have 0.01 µF power supply bypass capacitors.

FIGURE 2

The ramp generator provides a linear output voltage from 0V to 10V. This voltage is used as a) the horizontal amplifier input to the scope b) as a reference voltage to the difference amplifier and c) as the analog input voltage to the device under test.

The storage scope is used as an X-Y display with the horizontal input functioning as an input amplifier. The vertical input (Y-direction) displays the difference between the converter's analog input voltage and the equivalent output voltage of the same converter. The equivalent output voltage is generated by the 12-bit digital-to-analog converter (DAC1200). The horizontal input (X-direction) displays the difference voltage over the entire analog input voltage range. For a reference voltage set to 10.24V, the range is 0V to 10.24V. In the case of an 8-bit A/D, there would be 256 different voltages displayed across the entire range of the reference.

The test circuit shown in *Figure 2* can be used to test the ADC0800, ADC1211 or the ADC1210. These are 8-bit, 10-bit and 12-bit analog-to-digital converters.

Zero and full scale adjustment circuits are provided to allow a more accurate computation of non-linearity error.

The DAC1200D is a 12-bit D/A converter. It is quite adequate for the 8-bit and 10-bit parts but may be replaced by a higher resolution part if testing 12-bit A/D converters. The LH0044AH is a precision low noise amplifier and the LH0002CH is a buffer amplifier. The output of the reference must be adjusted to the full scale input voltage to assure proper output from the DAC1200. This is done by adjusting R-100.

TESTING

Figure 3 shows a typical output characteristic for the ADC0800, an 8-bit A/D converter. The reference line is set by switching the vertical channel (Y-axis amplifier) to dc and triggering the ramp generator. The adjustment is made using the horizontal positioning. The vertical range should be set to 5V/division. The 50 mV/division shown is the effective range of the channel taking into the account that the difference amplifier has a gain of 100.

When the initial set-up is completed, it is relatively easy to get readings for zero error, scale error, non-linearity error, differential non-linearity error, quantizing error, and to detect missing codes.

Zero error is simply the deviation from the reference line to the middle of the quantizing error when the input voltage is zero. All errors can be expressed as percent of full scale of in LSB's (least significant bits). For a 0V to 10.24V analog input 8-bit converter;

$$1\ \text{LSB} = \frac{10\text{V}}{2^8} = 40\ \text{mV} = 0.40\%\ \text{FS}$$

Scale error is the same as the zero error except that it occurs when the analog input voltage is at full scale.

In most applications, it is not the non-linearity in itself which is important, but rather the slope of the non-linearity. For instance, in an application using an A/D to sense gas in a tank and then to compute the remaining miles or time based on the current rate of usage, you do not want a large non-linearity slope. This gives the typical analog gas gauge effect of getting what appears to be good mileage over a certain range and poorer mileage over another range. Specifying non-linearity error and differential non-linearity error provides an error band around which to limit this change in slope or rate of change.

Non-linearity error can be defined in either of 2 ways. Shown in *Figure 3* is the "best straight line" definition for non-linearity. This is the more traditional definition for non-linearity and is the one use for the ADC0800 because of the inherent unidirectional nature of the error. A more conservative definition of "ideal straight line linearity" or more appropriately "total error" is twice that of the best straight line error. This linearity error is the maximum deviation from a straight line drawn between zero and full scale. The ADC1210 and ADC1211, 12-bit and 10-bit A/D converters, use this definition of non-linearity because the deviation can be in either direction.

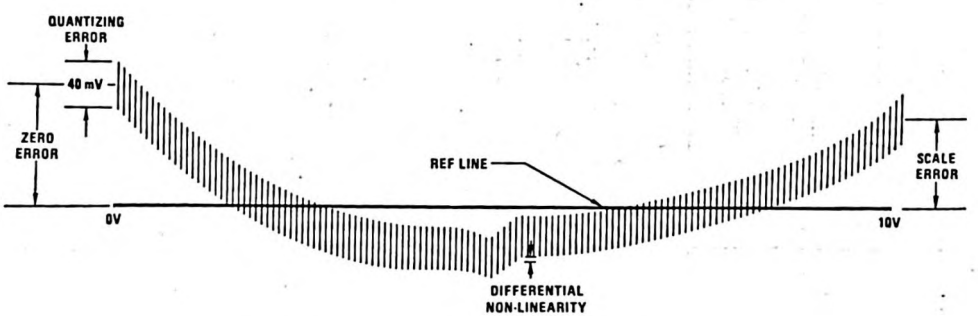


FIGURE 3. Typical Output Characteristic for the ADC0800

Differential non-linearity is most noticeable in converters using the successive approximation technique for conversion. It occurs when switching in a new resistance value for approximating the analog input voltage. It is the amount of change in the input voltage required to get a change in the digital output. On the scope it shows up as a change in non-linearity at one point. Differential non-linearity with this test method can be used to check for "no missing codes". "No missing codes" means that over the reference range, the converter will provide 2^n digital output codes, where N is the resolution of the converter.

Total unadjusted error is the maximum deviation from an ideal transfer function for an A/D converter. This error does not include quantizing error. The non-linearity error of an unadjusted ADC0800 is in a direction so as to decrease the total error. Therefore, the total unadjusted error for the ADC0800 will be either the zero error or the scale error, whichever is greater. This characteristic is only peculiar to this form of successive approximation type of converter.

Quantizing is inherent in the nature of the device. An 8-bit converter can make only 256 changes in the output regardless of the input voltage range. Therefore, for any converter there is always 1 LSB of quantizing error. This would appear as ±1/2 LSB of error around a straight line approximation of the output characteristic.

Monotonicity is the ability of the converter to give a digital output which is always in the same direction as the analog input voltage. The ADC0800 is inherently monotonic.

This paper has focused on the parameters peculiar to A/D converter products. It should give the user of any manufacturer's A/D converter a method for easily testing and comparing the characteristics of a particular A/D converter. It provides a low cost means of testing parameters which have historically been difficult to test.

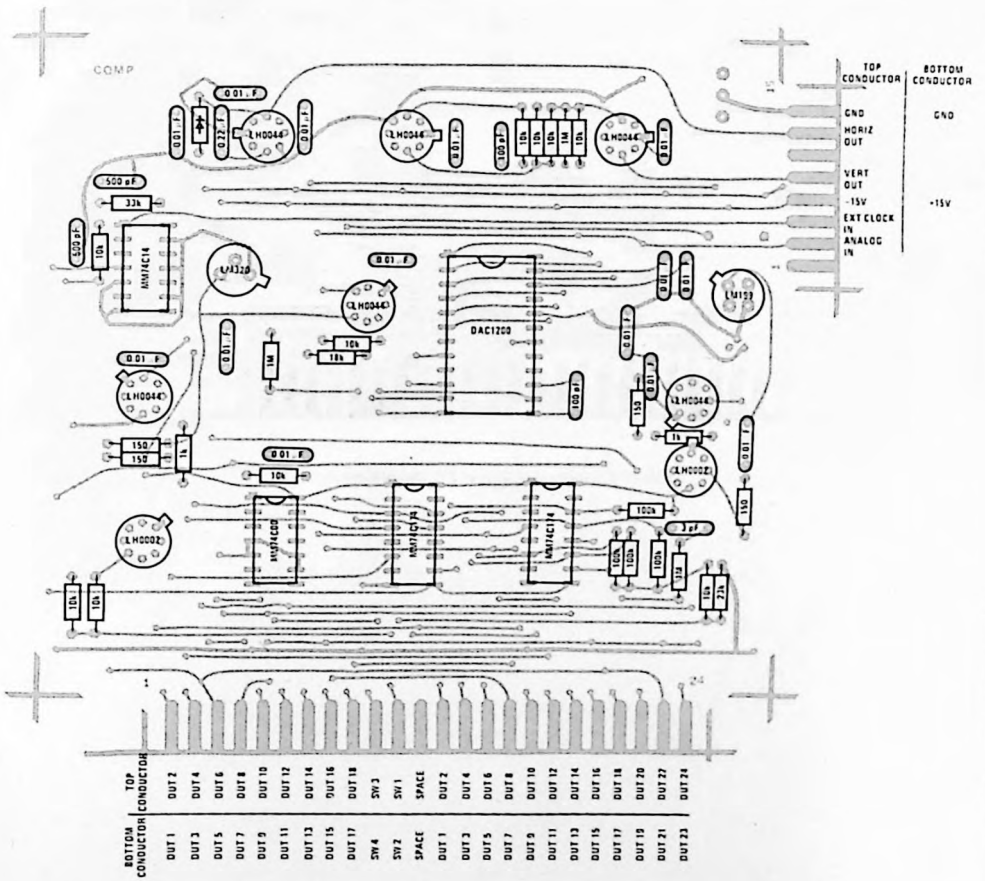


FIGURE 4. "Component Placement" on Component Side of P.C. Board

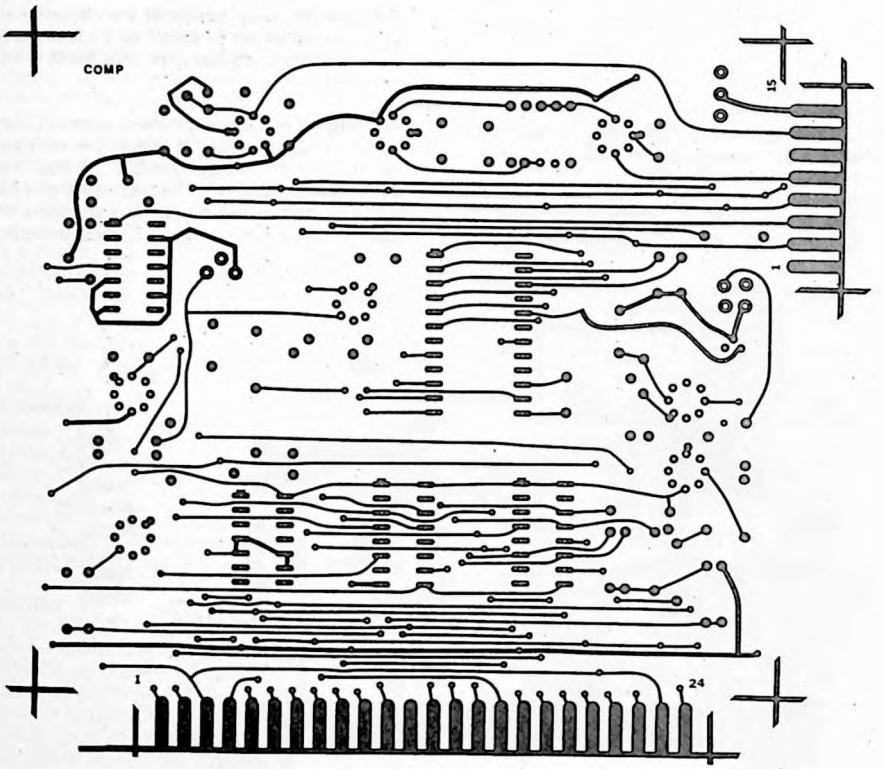


FIGURE 5. Component Side of P.C. Board Layout

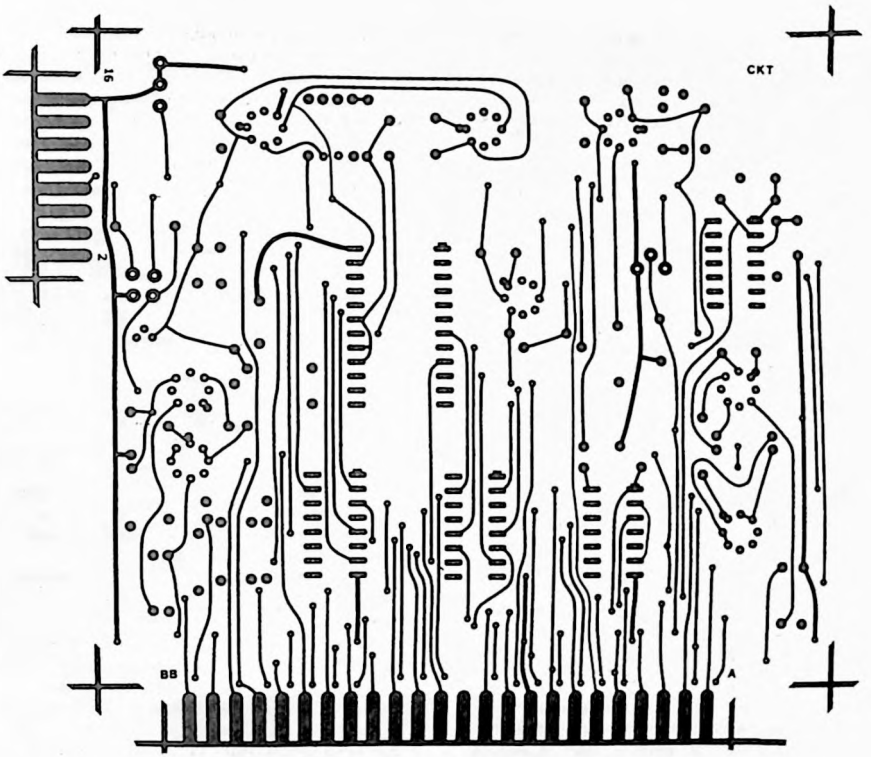


FIGURE 6. Backside of P.C. Board Layout

References for A/D Converters

National Semiconductor
Application Note 184
Robert C. Dobkin
July 1977

Interfacing between digital and analog signals is becoming increasingly important with the proliferation of digital signal processing. System accuracy is often limited by the accuracy of the converter and a limitation of the converter is the voltage reference. Design can be difficaul if the reference is external.

The accuracy of any converter is limited by the temperature dirft or long term drift of the voltage reference, even if conversion linearity is perfect. Assuming that the voltage reference is allowed to add 1/2 least significant bit error (LSB) to the converter, it is surprising how good the reference must be when even small temperature excursions are considered. When temperature changes are large, the reference design is a major problem. Table I shows the reference requirements for different converters while Table II shows how the same problems exist with digital panel meters.

The voltage reference circuitry is required to do several functions to maintain a stable output. First, input power supply changes must be rejected by the reference circuitry. Secondly, the zener used in the reference must be biased properly, while other parts of circuitry scale the typical zener voltage and provides a low impedance output. Finally, the reference circuitry must reject ambient temperature changes so that the temperature drift of the reference circuitry plus the drift of the zener does not exceed the desired drift limit.

While zener temperature coefficient is obviously critical to reference performance, other sources of drift can easily add as much error as zener — even in voltage references with modest performance of 20 ppm/°C temperature drift. Zener drift and op amp drift add directly to the drift error, while resistor error is only a function of how well the scaling resistors track. Resistors which have a high TC can be used if they track.

For a 10V output with a 6.9V zener, the drift contribution of resistor mistracking is about 0.4 since the gain is 1.4. The range of temperature coefficient errors for different components used to make a 10V reference from a 6.9V zener are shown in Table III. Another potential source of error, input supply variations, are negligible if the input is 1% regulated, and the resistor feeding the zener is stable to 1%.

Less frequently specified sources of error in voltage reference zeners are hysteresis and stress sensitivity. Stress on either a zener-diode junction or the series-temperature-compensating junction will cause voltage shifts. The axial leads on discrete devices can transmit stress from outside the package to the junction, causing 1 mV to 5 mV shifts.

Temperature cycling the discrete zener can also induce non-reversible changes in zener voltage. If a zener is heated from 25°C to 100°C and then back to 25°C, the zener voltage may not return to its original value. This is because the temperature cycle has permanently changed the stress in the die, changing the voltage. This effect can be as high as 5 mV in some diodes and may be cumulative with many temperature cycles. The new planar IC zeners, such as the LM199 (temperature stabilized) or the LM129 are insensitive to stress and show only about 50 μV of hysteresis for a 150°C temperature cycle since the package does not stress the silicon chip.

DESIGNING THE REFERENCE

If moderate temperature performance such as 20 ppm/°C is all that is needed, 2 different approaches can be used in the reference design. In the first, the temperature drift error is split equally between the zener and the amplifier or scaling resistors. This requires a moderately low drift zener and op amp with 10 ppm resistors.

TABLE I. Maximum Allowable Reference Drift for 1/2 Least Significant Bits Error of Binary Coded Converter

TEMP CHANGE	BITS					
	6	8	10	12	14	
25°C	310	80	20	5	1.25	ppm/°C
50°C	160	40	10	2.5	0.6	ppm/°C
100°C	80	20	5	1.2	0.3	ppm/°C
125°C	63	16	3	1	0.2	ppm/°C

TABLE II. Maximum Allowable Reference Drift for 1/2 Digit Error of Digital Meters

TEMP CHANGE	DIGITS								
	2	2 1/2	3	3 1/2	4	4 1/2	5	5 1/2	
25°C	200	100	20	10	2	1	0.2	0.1	ppm/°C
5°C			100	50	10	5	1	0.5	ppm/°C

*0.01%/°C = 100 ppm/°C, 0.001%/°C = 10 ppm/°C, 0.0001%/°C = 1 ppm/°C

TABLE III. Drift Error Contribution From Reference Components for a 10V Reference

DEVICE	ERROR	10V OUTPUT DRIFT
Zener	**Zener Drift**	
LM199A	0.5 ppm/°C	0.5 ppm/°C
LM199, LM399A	1 ppm/°C	1 ppm/°C
LM399	2 ppm/°C	2 ppm/°C
1N829, LM3999	5 ppm/°C	5 ppm/°C
LM129, 1N823A, 1N827A, LM329A	10–50 ppm/°C	10–50 ppm/°C
LM329, 1N821, 1N825	20–100 ppm/°C	20–100 ppm/°C
Op Amp	**Offset Voltage Drift**	
LM725, LH0044, LM121	1 μV/°C	0.15 ppm/°C
LM108A, LM208A, LM308A	5 μV/°C	0.7 ppm/°C
LM741, LM101A	15 μV/°C	2 ppm/°C
LM741C, LM301A, LM308	30 μV/°C	4 ppm/°C
Resistors	**Resistance Ratio Drift**	
1% (RN55D)	50–100 ppm	20–40 ppm/°C
0.1% (Wirewound)	5–10	2–4 ppm
Tracking 1 ppm Film or Wirewound	–	0.4 ppm/°C

The second approach uses a very low drift zener and allows the buffer amplifier or scaling resistor to cause most of the drift error. This type of design is now made economical by the availability of low cost temperature stabilized IC zeners with virtually no TC. Further, the temperature coefficient of this reference is easily upgraded, if necessary. The 2 reference circuits are shown in *Figure 1a and Figure 1b.*

In *Figure 1a*, an LM308 op amp is used to increase the typical zener output to 10V while adding a worst-case drift of 4 ppm/°C to the 10 ppm/°C of the zener. Resistors R3 and R4 should track to better than 10 ppm bringing the total error so far to 18 ppm. Since the output must be adjusted to eliminate the initial zener tolerance, a pot, R5 and R2 have been added. The loading on the pot by R2 is small, and there is no tracking requirement between the pot and R2. It is necessary for R2 to track R3 and R4 within 50 ppm.

In *Figure 1b*, a low drift reference and op amp are used to give a total drift, exclusive of resistors of 3 ppm/°C. Now the resistor tracking requirement is relaxed to about 50 ppm, allowing ordinary 1% resistors to be used. The circuit in *Figure 1b* is modified easily for applications requiring 3 ppm/°C to 5 ppm/°C overall drift by tightening the tracking of the resistors. For more accurate applications, the Kelvin sensing for both output and ground should be used. For even lower drifts, substituting a 1 μV/°C op amp, 1 ppm tracking resistors and an LM199A zener, overall drifts of 1 ppm/°C can be achieved. In both of the circuits, it is important to remember that the tracking of resistors can, at worst-case, be twice temperature drift of either resistance.

In both circuits, the zener is biased by a single resistor from the supply, rather than from the reference output. This eliminates possible start-up problems and, because of the 1Ω dynamic impedance of the IC zeners, only

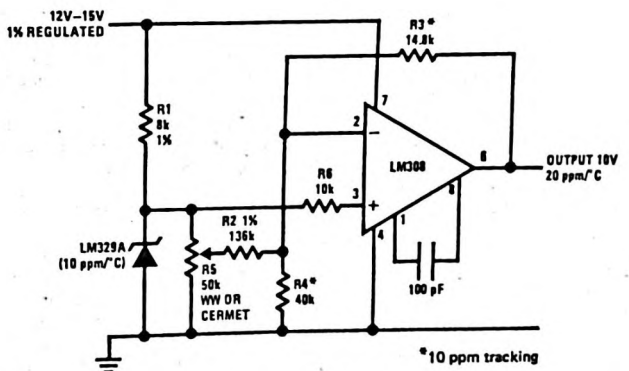


FIGURE 1a. 10V, 20 ppm Reference Using a Low Cost Zener and Low Drift Resistors

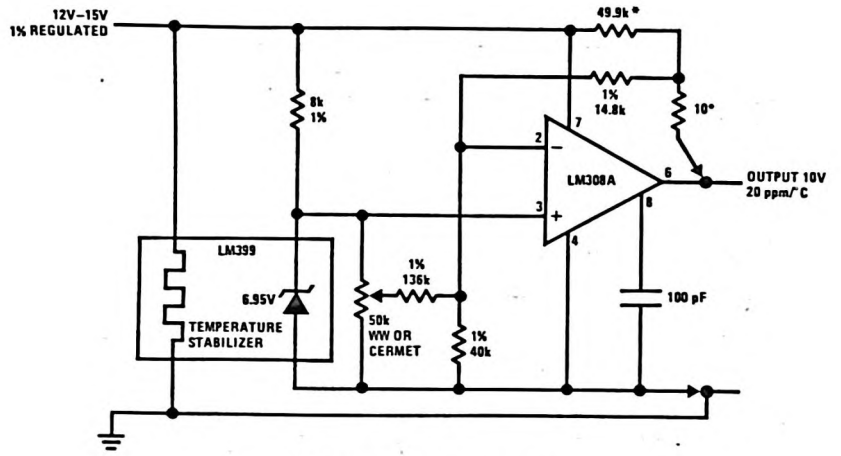


FIGURE 1b. 10V Reference has Low Drift Reference and Standard 1% Resistors. Kelvin Sensing is Shown with Compensation for Line Changes.

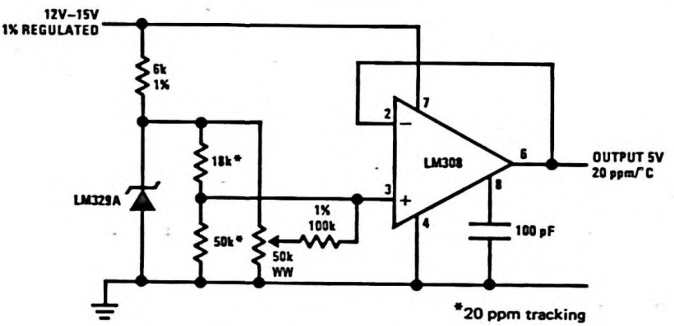


FIGURE 2. Low Voltage Reference

adds about 20 μV of error. Compensation for input changes is shown in *Figure 1b*. Conventional zeners do not allow this biasing. A conventional 5 ppm reference such as the 1N829 has a dynamic impedance of about 15Ω. If it is biased from a resistor from a 1% regulated 15V supply, the operating current can change by 1.7% or 127 μA. This will shift the zener voltage by 1.9 mV or 60 ppm. With the IC zeners operating at 1 mA, a 1% shift in the supply will change the reference by 20 μV or 3 ppm. Further, power dissipation in the IC is only 7 mW, giving low warm-up drift compared to 7.5 mA zeners. The biasing resistor for the IC zener need not be any better than an ordinary 1% resistor since performance is independent of current.

When output voltages less than the zener voltage are desired, the IC zeners significantly simplify circuit design since no auxiliary regulator is needed for biasing. *Figure 2* shows a 5V reference circuit for use with a 15V input. In this case, zener drift contributes proportionally to the output drift while op amp offset drift adds a greater rate. With the 10V reference, 15 μV/°C from the op amp contributed 2 ppm/°C drift, but for the 5V reference, 15 μV/°C adds 3 ppm/°C. This makes op amp choice more important as the output voltage is lowered. Of course, if a high output impedance is tolerable, the op amp can be eliminated.

APPROACHING THE ULTIMATE DRIFT

To obtain the lowest possible drifts, temperature coefficient trimming is necessary. With discrete zeners, the operating current can sometimes be trimmed to change the TC of the reference; however, the temperature coefficient is not always linear or predictable. With the new IC zeners, TC is independent of operating current so trimming must be done elsewhere in the circuit. The lowest drift components should be used since

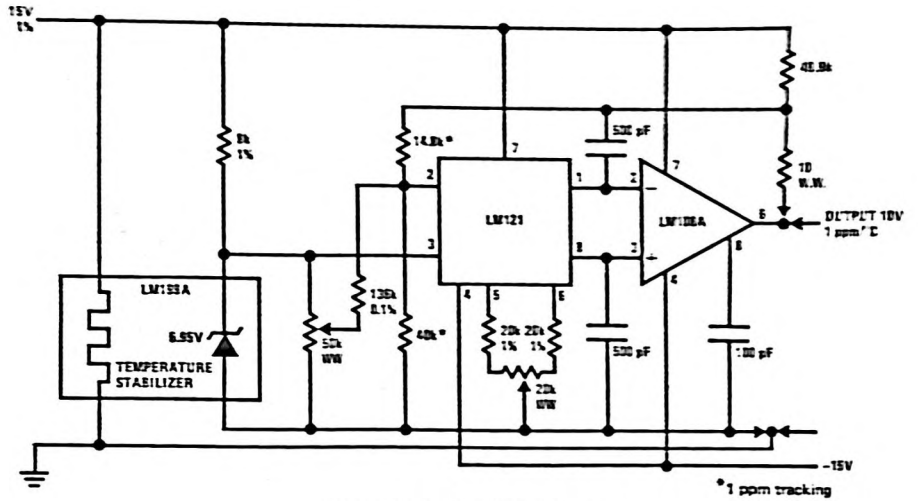


FIGURE 3. Ultra Low Drift Reference

trimming can only remove a linear component of drift. High TC devices can have a highly non-linear drift, making trimming difficult.

Figure 3 shows a circuit suitable for trimming. An LM199A reference with 0.5 ppm/°C drift is used with a 121/108 op amp. Resistors should be 1 ppm tracking to give overall untrimmed drifts of about 0.9 ppm. The 121/108 is a low drift amplifier combination where drift is predictably proportional to offset voltage. An offset can be set for the 108/121 combination to cancel the measured drift with 1 pass calibration.

Trimming procedure is as follows: the zener is disconnected and the input of the op amp grounded. Then the offset of the op amp is nulled out to zero. Reconnecting the zener, the output is adjusted to precisely 10V. A temperature run is made and the drift noted. The op amp will drift 3.6 μV/°C for every 1 mV of offset, so for every 5 μV/°C drift at the output, the offset of the op amp is adjusted 1 mV (1.4 mV measured at the output) in the opposite direction. The output is readjusted to 10V and the drift checked.

Although this trimming scheme was chosen since only a single adjustment is usually required, compensation is not always perfect. Hysteresis effects can appear in resistors or op amps as well as zeners. Best results can be obtained by cycling the circuit to temperature a few times before taking data to relieve assembly stresses on the components. Also, oven testing can sometimes cause thermal gradients across circuits, giving 50 μV to 100 μV of error. However, with careful layout and trimming, overall reference drifts of 0.1 ppm/°C to 0.2 ppm/°C can be achieved.

There are 2 other possible problem areas to be considered before final layout. Good single point grounding is important. Traces on a PC board can easily have 0.1Ω and only 10 mA will cause a 1 mV shift. Also, since these references are close to high-speed digital circuitry, shielding may be necessary to prevent pick-up at the inputs of the op amp. Transient response to pick-up or rapid loading changes can sometimes be improved by a large capacitor (1 μF–10 μF) directly on the op amp output; but this will depend on the stability of the op amp.

CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200
Jake Buurma
March 1978

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters—2 of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 1/2-digit DPM and ADD3701 3 3/4-digit DPM) while the other 2 (ADC3511 3 1/2-digit A/D and ADC3711 3 3/4-digit A/D) have addressable BCD outputs. These last 2 devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 1/2-digit types divide the input into 2,000 counts plus sign, while the 3 3/4-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 1/2-digit converters require 200 ms per conversion; 3 3/4-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the supply must be isolated from the inputs. Without an isolated supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

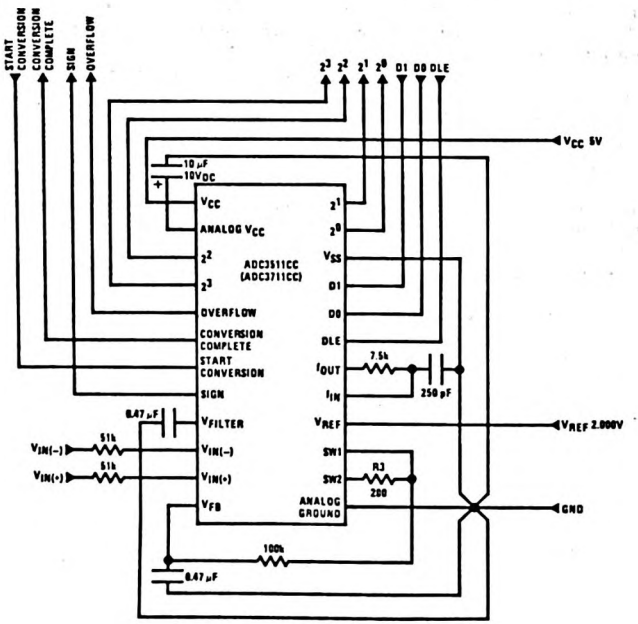


FIGURE 1. Basic A/D Converter

BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

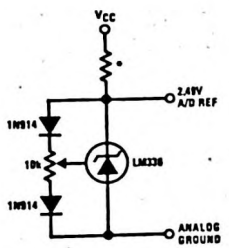
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*. One reference can be used for many A/D's. The value of the upper series resistor R1 depends on the number of converters used.



$$^{*}R = \frac{2.49V}{(2N+1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3 and 4*. *Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multichannel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The program then calls a subroutine which

goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

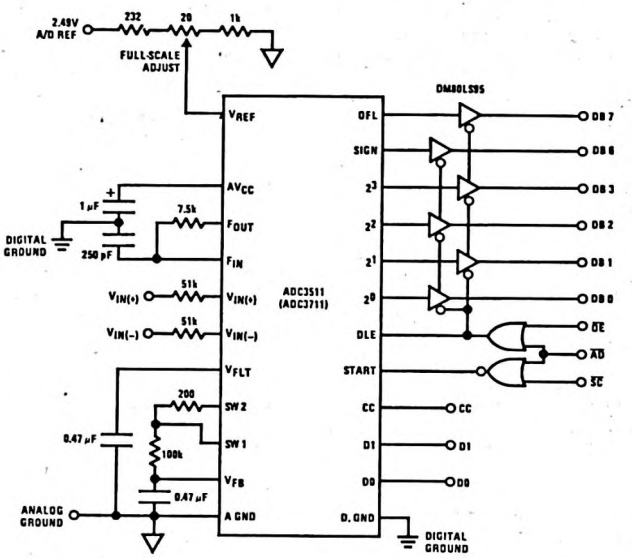


FIGURE 3. Dual Polarity A/D Requires that Inputs are Isolated from the Supply. Input Range is ±1.999V.

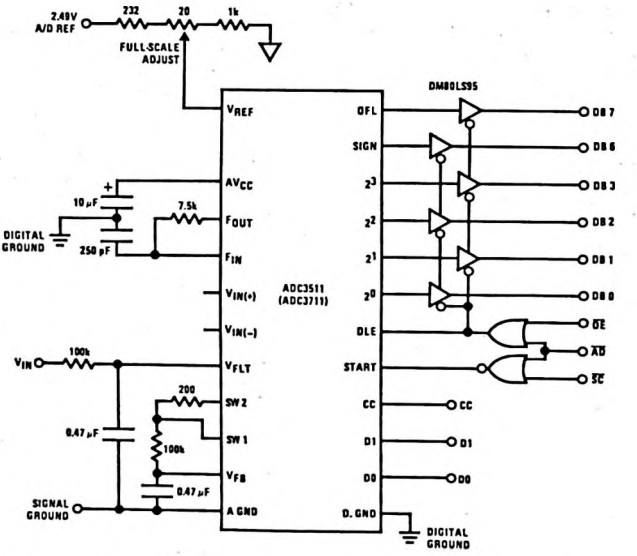


FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range is +1.999V.

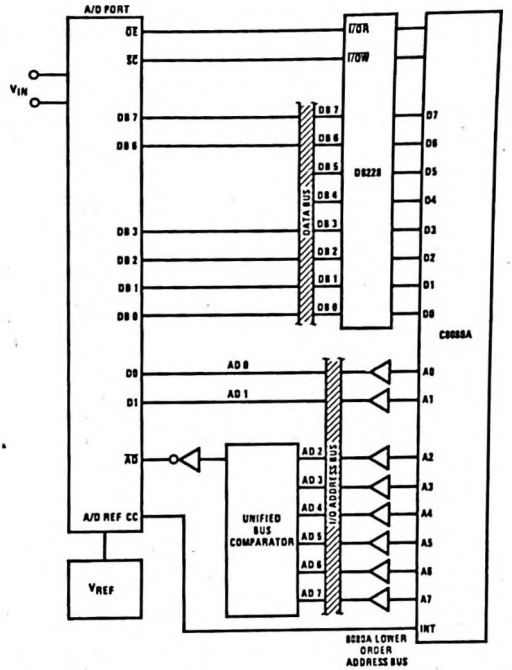


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

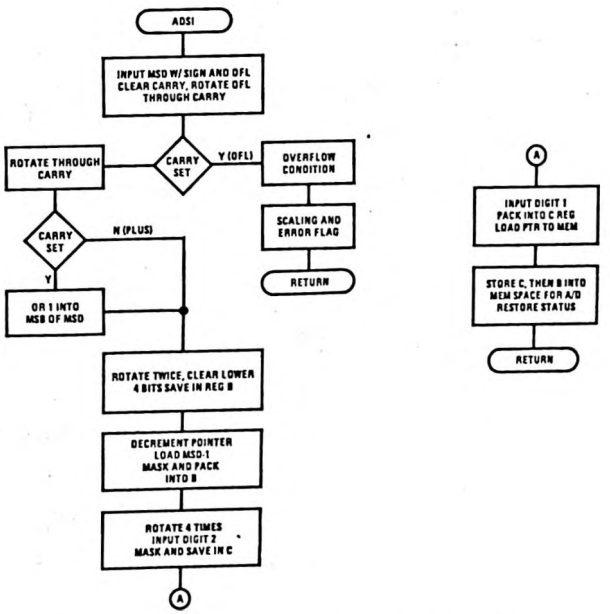

ADSI
INPUT MSD W/SIGN AND OFL CLEAR CARRY, ROTATE OFL THROUGH CARRY
ROTATE THROUGH CARRY
CARRY SET
Y (OFL)
OVERFLOW CONDITION
SCALING AND ERROR FLAG
RETURN
CARRY SET
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE, CLEAR LOWER 4 BITS SAVE IN REG B
DECREMENT POINTER LOAD MSD-1 MASK AND PACK INTO B
ROTATE 4 TIMES INPUT DIGIT 2 MASK AND SAVE IN C
A
A
INPUT DIGIT 1 PACK INTO C REG LOAD PTR TO MEM
STORE C, THEN B INTO MEM SPACE FOR A/D RESTORE STATUS
RETURN

FIGURE 6. Flow Chart for Single Channel A/D Converter

```
LABEL   OPCODE   OPERAND    COMMENT
ADIS:   PUSH     PSW        ; A/D interrupt
                            service
        PUSH     H          ; save
        PUSH     B          ; current status
        IN       ADD 4      ; input A/D digit 4
        IN       ADD 4      ; delay
        ORA                 ; reset carry
        RAL                 ; rotate OFL thru
                            carry
        JC       OFL        ; overflow condition
        RAL                 ; rotate sign thru
                            carry
        JC       PLUS       ; positive input
        ORI      20H        ; OR 1 into MSB,
                            neg input
PLUS:   RAL                 ; shift
        RAL                 ; into position
        ANI      FO         ; mask lower bits
        MOV      BA         ; save in B
        IN       ADD 3      ; input digit 3
        IN       ADD 3      ; delay
        ANI      OF         ; mask higher bits
        OR       B          ; pack into B
        MOV      B, A       ; save in B
        IN       ADD 2      ; input digit 2
        IN       ADD 2      ; delay
        RAL                 ; rotate
        RAL                 ; into
        RAL                 ; upper
        RAL                 ; 4 bits
        ANI      FO         ; mask lower bits
        MOV      C, A       ; save in C
        IN       ADD 1      ; in digit 1
        IN       ADD 1      ; delay
        ANI      OF         ; mask upper bits
        OR       C          ; pack
        MOV      C, A       ; save in C
        LXI      H, ADMS    ; load ptr to A/D
                            Mem, space
        MOV      M, C       ; save C in memory
        INX      H          ; point next
        MOV      M, B       ; save B in memory
        OUT      ADD 1      ; start new conver-
                            sion
        POP      B          ; restore
        POP      H          ; previous
        POP      PSW        ; status
        EI                  ; enable interrupts
        RET                 ; return to main
                            program
```

Routine 1. Single Channel Interrupt Service Routine

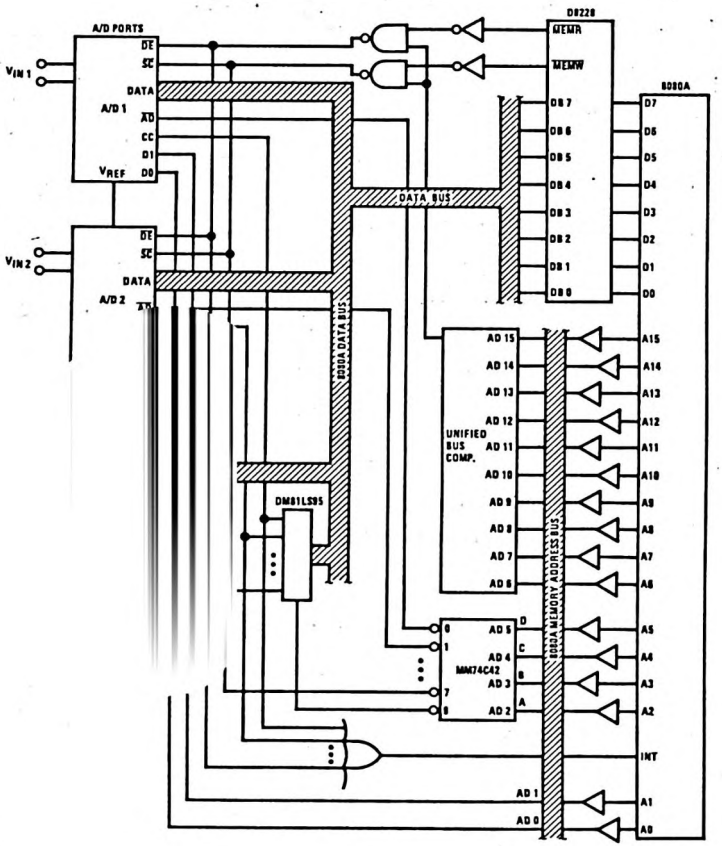


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

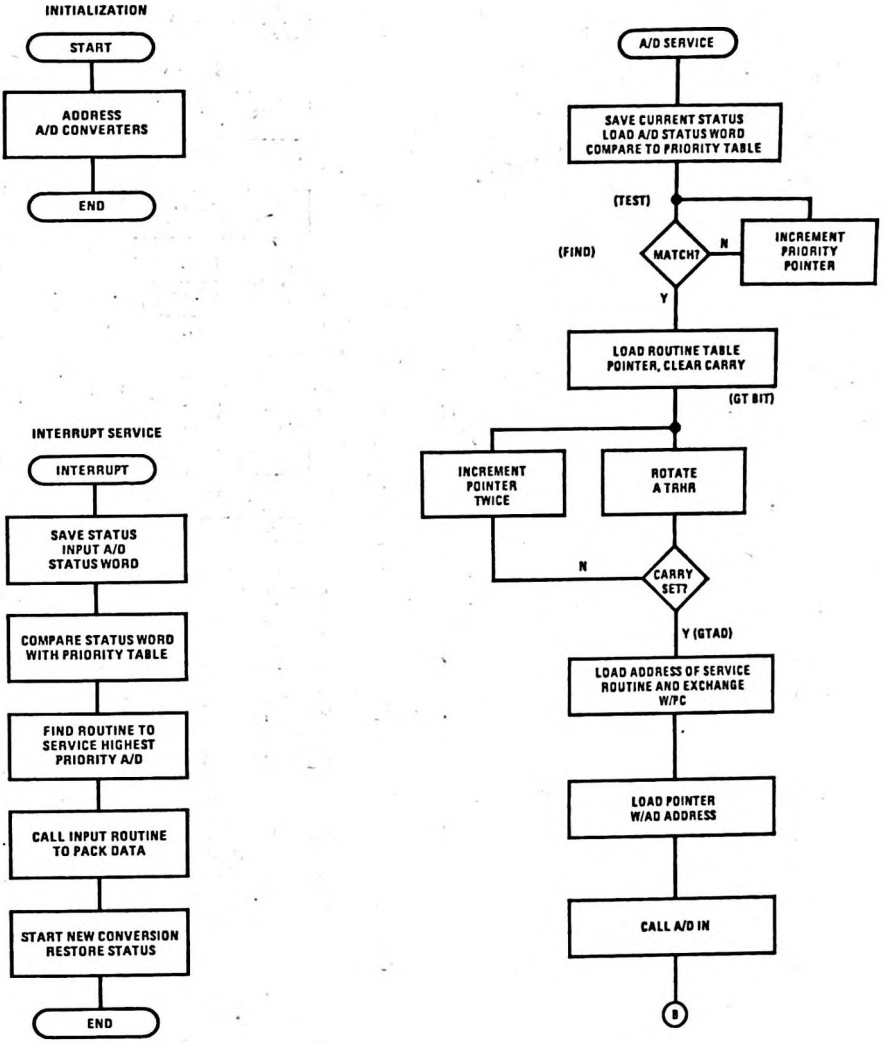


FIGURE 8. Flow Charts of A/D Routines

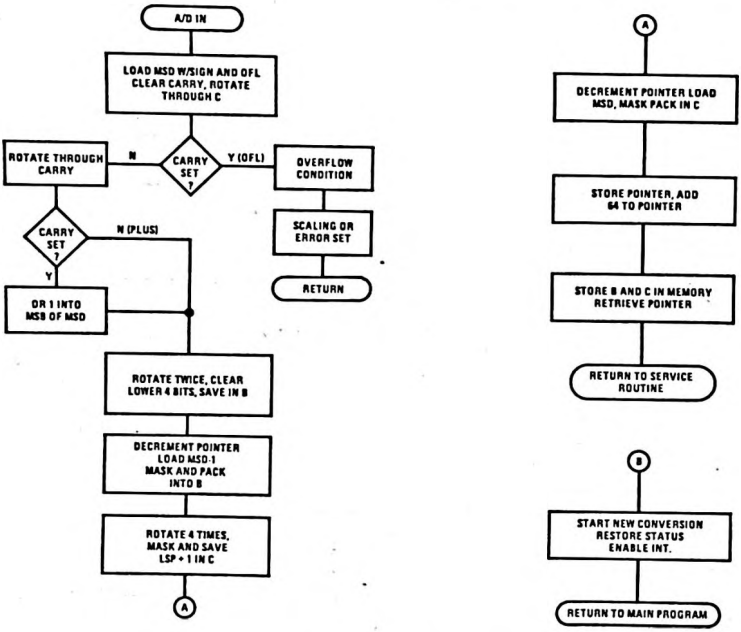

A/D IN
LOAD MSD W/SIGN AND OFL CLEAR CARRY, ROTATE THROUGH C
ROTATE THROUGH CARRY
N
CARRY SET ?
Y (OFL)
OVERFLOW CONDITION
SCALING OR ERROR SET
RETURN
CARRY SET ?
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE, CLEAR LOWER 4 BITS, SAVE IN B
DECREMENT POINTER LOAD MSD-1 MASK AND PACK INTO B
ROTATE 4 TIMES, MASK AND SAVE LSP + 1 IN C
A
A
DECREMENT POINTER LOAD MSD, MASK PACK IN C
STORE POINTER, ADD 64 TO POINTER
STORE B AND C IN MEMORY RETRIEVE POINTER
RETURN TO SERVICE ROUTINE
B
START NEW CONVERSION RESTORE STATUS ENABLE INT.
RETURN TO MAIN PROGRAM

FIGURE 8. Flow Charts of A/D Routines (Continued)

```
LABEL   OPCODE   OPERAND    COMMENT
IAD:    PUSH     PSW        ;interrupt from A/D
        PUSH     H          ;save H & L on
                            stack
        PUSH     B          ;save B & C on
                            stack
        PUSH     D          ;save D & E on
                            stack
        LXI      H, ADWD    ;pickup A/D status
                            word
        MOV      6, M       ;move word into B
        LXI      H, PRTBL   ;pickup priority tbl
                            pointer
TEST:   MOV      A, B       ;place status word
                            in accum.
        ANA      M          ;mask with priority
                            table
        JNZ      FIND       ;match jump to
                            Find
        INX      H          ;point to lower
                            priority
        JMP      TEST       ;try again
FIND:   LXI      H, RTBL    ;pickup routine tbl
                            pointer
        ORA      A          ;reset carry
GTBIT:  RAR                 ;rotate thru carry
        JC       GTAD       ;bit was found
        INX      H          ;point to
        INX      H          ;next routine
        JMP      GTBIT      ;try again
GTAD:   MOV      E, M       ;move first byte
                            into E
        INX      H          ;point to next byte
        MOV      D, M       ;move second byte
                            into D
```

```
LABEL   OPCODE   OPERAND    COMMENT
        XCGH                ;exchange DE, HL
        PCHL                ;jump to input
                            routine
INAD1:  LXI      H, AD1     ;pickup pointer to
                            A/D 1
        CALL     ADIN       ;call common input
                            routine
        MOV      M, A       ;start new conversion
        JMP      DONE       ;all done
INAD2:  LXI      H, AD2     ;pickup pointer to
                            A/D 2
        CALL     ADIN       ;call input routine
        MOV      M, A       ;start new conver-
                            sion
        JMP      DONE       ;all done
        .
        .
        .
DONE:   POP      D          ;restore D
        POP      B          ;restore B
        POP      H          ;restore H
        POP      PSW        ;restore PSW
        EI                  ;enable interrupts
        RET                 ;return to main
                            program
PRTBL:  DB       04H        ;0000C100 AD3
                            highest priority
        DB       03H        ;00000011 AD2 &
                            AD1 next priority
        .
        .
        .
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

```
LABEL   OPCODE  OPERAND   COMMENT
PRTBL:  DB      10H       ;00010000 AD5 lowest priority
RTBL:   DW      1000H     ;routine for A/D 1
        DW      100CH     ;routine for A/D 2
        .
        .
        .
        DW      1060H     ;routine for A/D 8
ADIN:   MOV     A, M      ;input MSD plus OFL & SIGN
        MOV     A, M      ;delay
        ORA     A         ;reset carry
        RAL               ;rotate left thru carry, OFL
        JC      OFL       ;jump to overflow if set
        RAL               ;rotate left thru carry, sign
        JC      PLUS      ;jump to plus if set
        OR1     20H       ;OR1 into BCD, MSB for minus
PLUS:   RAL
        RAL
        ANI     FO        ;mask lower order bits
        MOV     B, A      ;save in B
        DCR     H         ;point to MSD-1
        MOV     A, M      ;input MSD-1
        MOV     A, M      ;delay
        ANI     OF        ;mask higher 4 bits
        OR      B         ;pack MSD and MSD-1
        MOV     B, A      ;save in B
        DCR     H         ;point to LSD + 1
        MOV     A, M      ;input LSD + 1
        MOV     A, M      ;delay
        RAL               ;rotate
        RAL               ;into
        RAL               ;upper
        RAL               ;4 bits
        ANI     FO        ;mask lower bits
        MOV     C, A      ;save in C
        DCR     H         ;point to LSD
        MOV     A, M      ;input LSD
        MOV     A, M      ;delay
        ANI     OF        ;mask upper bits
        OR      C         ;pack
        MOV     C, A      ;save in C
        SHLD    TEMP      ;store HL in temp
        MOV     A, L      ;move L in accum.
        ACI     64        ;generate lower address
        MOV     L, A      ;above memory mapped
        MOV     A, H      ;converter addresses
        ACI     0         ;include carry
        MOV     H, A      ;to upper bits
        MOV     M, C      ;store C
        INX     H         ;then
        MOV     M, B      ;store B
        LHLD    TEMP      ;retrieve HL
        RET               ;return
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority (Continued)

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

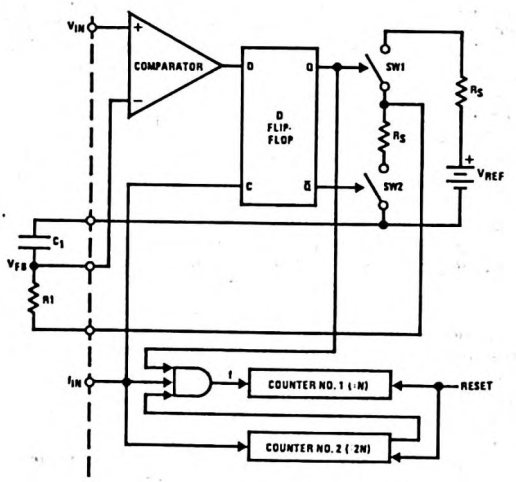
The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.
For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

ELECTRICAL CHARACTERISTICS

ADC3511CC, ADC3711CC $4.75 \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A + 85°C$, f_c = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	(Note 3)				
		V_{IN} = 0–2V Full-Scale	−0.05	±0.025	0.05	% of Full-Scale
		V_{IN} = 0–200 mV Full-Scale				
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = 1/2 counts and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

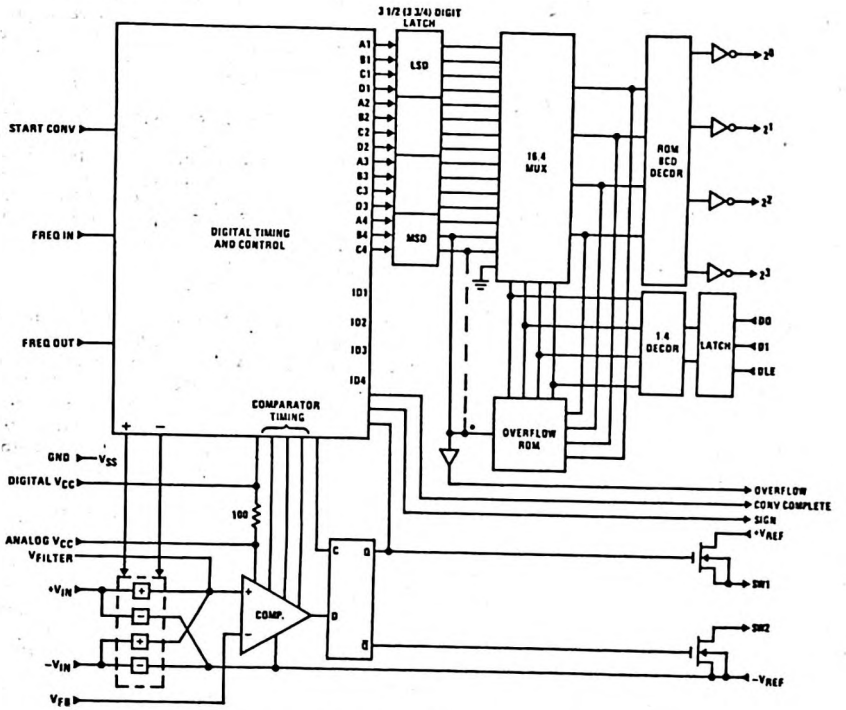


FIGURE A2. ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D) Block Diagram

A Digital Multimeter Using the ADD3501

National Semiconductor
Application Note 202
Carson Chen
July 1978

INTRODUCTION

National Semiconductor's ADD3501 is a monolithic CMOS IC designed for use as a 3 1/2-digit digital voltmeter. The IC makes use of a pulse-modulation analog-to-digital conversion scheme that operates from a 2V reference voltage, functions with inputs between 0V and ±1.999V and operates from a single supply.

The conversion rate is set by an external resistor/capacitor combination, which controls the frequency of an on-chip oscillator. The ADD3501 directly drives 7-segment multiplexed LED displays, aided only by segment resistors and external digit buffers. The ADD3501 blanks the most significant digit whenever the MSD is zero; and, during overrange conditions, the display will read either +OFL or −OFL (depending on the polarity of the input).

These characteristics make the ADD3501 suitable for use in low-cost instrumentation. An example of such use is the inexpensive, accurate, digital multimeter (DMM) presented here—an instrument that measures AC and DC voltages and currents, and resistance.

CIRCUIT DESCRIPTION

Figure 1 shows the circuit diagram of the ADD3501-based DMM, and Table I summarizes its measurement capabilities. Since the accuracy of the ADD3501 is ±0.05%, the DMM's performance is mainly determined by the choice of discrete components.

Supporting the ADD3501 is a DS75492 digit driver, an NSB5388 LED display, and an LM340 regulator for the V_{CC} supply. A 2V reference voltage—derived from the LM336 reference-diode circuitry—permits the 3 1/2-digit system a 1 mV/LSD resolution (i.e., the ADD3501's full-scale count of 1999 or 1999 mV).

DC Voltage Measurement. The DMM's user places the (+) and (−) probes across the voltage to be measured, and sets the voltage range switch as necessary. This switch scales the input voltage, dividing it down so that the maximum voltage across the ADD3501's V_{IN} and V_{IN-} pins is limited to 2 V full-scale on each input range. The ADD3501 performs an A/D conversion, and displays the value of the DMM's input voltage. The instrument's input impedance is at least 10 MΩ on all DC voltage ranges. Except for the 2V range, the DMM's survival voltage—the maximum safe DC input—is in excess of 1 kV. On the 2V range, the maximum allowable input is 700V.

AC Voltage Measurement. Switching the DMM to its AC VOLTS mode brings the circuit of *Figure 2* into function. This circuit operates as an averaging filter to generate a DC output proportional to the value of the rectified AC input; this value, in turn, is "tapped down" by R5 to a level equivalent to the input's rms value, which is the value displayed by the DMM.

Op amp A3 is simply a voltage follower that lowers the input-attenuator's source impedance to a value suitable to drive into A4. This impedance conversion helps eliminate some of the possible offset-voltage problems (the A4 input-offset-current source impedance IR drop, for example) and noise susceptibility problems as well. C1 blocks the DC offset voltage generated by A3.

A4 and A5 comprise the actual AC-to-DC converter; to see how it works refer again to *Figure 2*, and consider first its operation on the negative portion of an AC input signal. At the output of A4 are 2 diodes, D1 and D2, which act as switches. For a negative input to A4's inverting input, D1 turns on and clamps A4's output to 0.7V, while D2 opens, disconnecting A4's output from A5's summing point (the inverting input). A5 now operates as a simple inverter: R2 is its input resistor, R5 its feedback resistor, and its output is positive.

Now consider what happens during the positive portion of an AC input. A4's output swings negative, opening D1 and closing D2, and the op amp operates as an inverting unity-gain amplifier. Its input resistor is R1, its feedback resistor is R3, and its output now connects to A5's summing point through R4. D2 does not affect A4's accuracy because the diode is inside the feedback loop.

A positive input to A4 causes it to pull a current from A5's summing point through R4 and D2; the positive input also causes a current to be supplied to the A5 summing point through R2. Because A4 is a unity-gain inverter, the voltage drops across R2 and R4 are equal, but opposite in sign. Since the value of R2 is double that of R4, the net input current at A5's summing point is equal to, but opposite, the current through R2. A5 now operates as a summing inverter, and yields—again—a positive output. (R6 functions simply to reduce output errors due to input offset currents.)

Thus, the positive and negative portions of the DMM's AC voltage input both yield positive DC outputs from A5. With C2 connected across R5 as shown, the circuit becomes an averaging filter. As already mentioned, the tap on R5 is set so that the circuit's DC output is equivalent to the rms value of the DMM's AC voltage input, which is the value converted and displayed by the ADD3501.

DC Current Measurement. To make a DC current measurement, the user inserts the DMM's probes in series with the circuit current to be measured and selects a suitable scale. On any scale range, the DMM loads the measured circuit with a 2V drop for a full-scale

TECHNICAL SPECIFICATIONS

DC VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV
INPUT IMPEDANCE	2V RANGE, >10MΩ
	20V TO 2 kV RANGE, 10MΩ
AC RMS VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV
	(40 TO 5 kHz SINEWAVE)
DC AMPS	< ±1% ACCURACY
RANGES	200 μA, 2 mA, 20 mA, 200 mA, 2A
AC RMS AMPS	< ±1% ACCURACY
RANGES	200 μA, 2 mA, 20 mA, 200 mA, 2 A
OHMS	< ±1% ACCURACY
RANGES	200 Ω, 2 kΩ, 20 kΩ, 200 kΩ, 2 MΩ

Note 1: All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Note 2: All resistors are 1/4 watt unless otherwise specified.

Note 3: All capacitors are ±10%.

Note 4: All op amps have a 0.1 μF capacitor connected across the V+ and V− supplies.

Note 5: All diodes are 1N914.

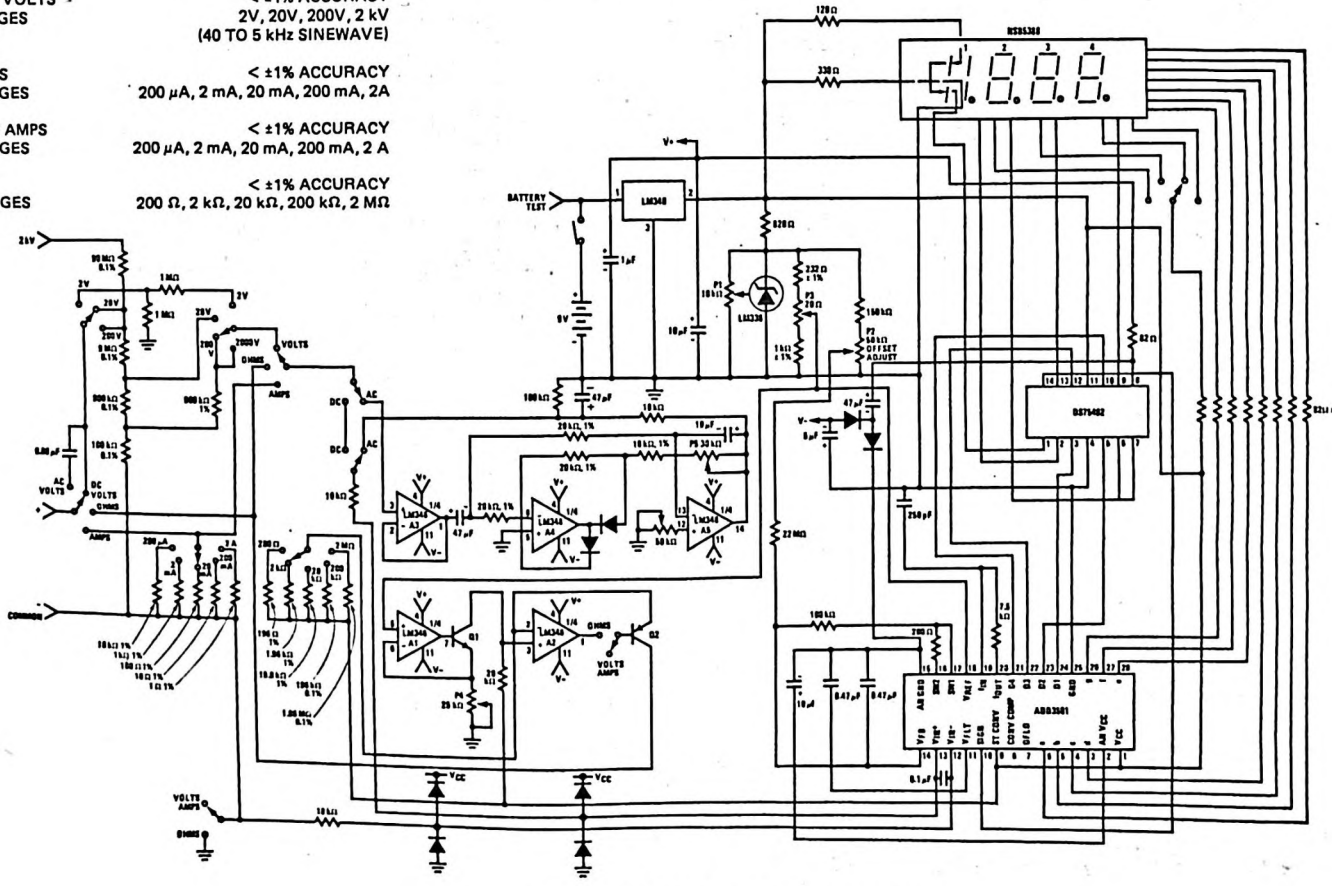


FIGURE 1. ADD3501 Low Cost Digital Multimeter

input.* The ADD3501 simply converts and displays the voltage drop developed across the DMM's current-sensing resistor.

AC Current Measurement. AC current measurements are made in a way similar to DC current measurements. The DMM is switched to its AMPS and AC settings. The in-circuit current is again measured by a drop across the DMM's current-sensing resistor, but now the AC voltage developed across this resistor is processed by A3, A4, and A5—exactly as described for AC voltage measurements—before being transferred to the ADD3501. Again, the DMM displays an rms value appropriate for the AC signal current being measured.

Resistance Measurement. This DMM measures resistance in the same way as do most multimeters: it measures the voltage drop developed across the unknown resistance by forcing a known, constant-current through it. Suitable scale calibration translates the voltage drop to a resistance value.

The resistance measurement requires the generation of a constant-current source that is independent of changes in V_{CC}, using the 2V, ground-referred reference voltage. The circuit of *Figure 3* accomplishes this.

In *Figure 3*, A1 establishes a constant-current sink by forcing node A to V_{REF}, the voltage level at A1's non-inverting input. With node A held constant at V_{REF} (2.000V), current through R2 is also fixed—since Q1's collector current is determined by the αI_E product— thus establishing V1 as

$$V1 = V_{CC} - \alpha(V_{REF}/R1)R2 \qquad (1)$$

Note that V_{REF} is derived from the LM336—a precision voltage source. Equation (1) shows, then, that (all else remaining constant) V1 varies directly with changes in V_{CC}; i.e., V1 tracks V_{CC}. The A1/Q1 pair thus establishes a voltage across R2 that floats, independent of changes in the ground-referenced potentials (V_{CC} and V_{REF}) that define it.

Now look at the A2/Q2 circuitry. The closed-loop operation of A2 tries to maintain a zero differential voltage between its input terminals. A2's non-inverting input is held at V1; thus, A2's inverting input is driven to V1. The current through R_L (Q2's emitter current) is therefore $(V_{CC} - V1)R_L$. Since V1 tracks V_{CC}, then $(V_{CC} - V1)$ — the voltage drop across R_L—is constant, thus producing I_{SOURCE} *(Figure 3)*—the constant source current needed for the resistance measurement.

Note, that varying R_X will not affect I_{SOURCE} so long as the voltage drop across R_X is less than $(V1 - V_{BE2})$. Should V_{RX} exceed $(V1 - V_{BE2})$, Q2 would saturate, invalidating the measurement. The ADD3501 eliminates this worry, however, because as soon as the drop across R_X equals or exceeds the 2V full-scale input voltage the ADD3501 will display an OFL condition.

Finally, SW1 *(Figure 3)* is required as part of the VOLTS/AMPS/OHMS mode selection circuitry; in the VOLTS/AMPS position it prevents Q2's base-emitter junction pulling the V− supply to ground through A2.

*This drop may be reduced to 200 mV; refer to the last section of this application note.

TABLE I. DMM PERFORMANCE

Measurement Mode	Range					Frequency Response	Accuracy	Overrange Display
	0.2	2	20	200	2000			
DC Volts	–	V	V	V	V	–	≤ 1% F.S.	± OFLO
AC Volts	–	V_{RMS}	V_{RMS}	V_{RMS}	V_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+ OFLO
DC Amps	mA	mA	mA	mA	mA		≤ 1% F.S.	±OFLO
AC Amps	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+OFLO
Ohms	kΩ	kΩ	kΩ	kΩ	kΩ	–	≤ 1% F.S.	+OFLO

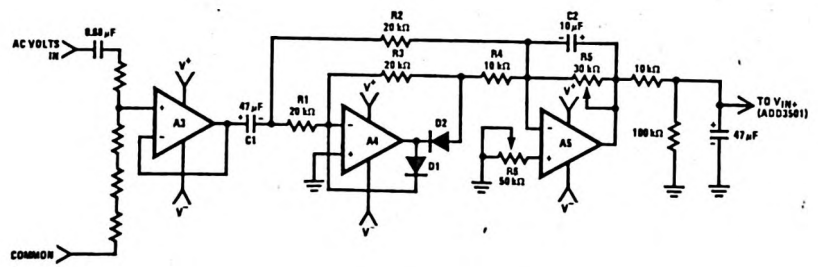


FIGURE 2. AC/DC Converter

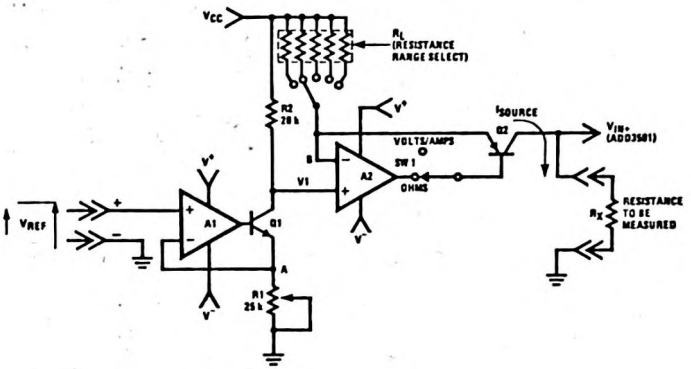


FIGURE 3. Constant-Current Source

CALIBRATION

Calibrate the DMM according to the following sequence of operations:

	1. Adjust P1 until the cathode voltage of the reference diode, LM336, equals 2.49V. This reduces the diode's temperature coefficient to its minimum value.
DC Volts 2V Range	2. Short the (+) and (−) probe inputs of the ADD3501 and adjust P2 until the display reads 0000.
DC Volts 2V Range	3. Apply 1.995 volts across the (+) and (−) probe inputs and adjust P3 until the display reads 1.995.
Ohms 2 MΩ Range	4. Select a precision resistor with a value near full-scale or the 2 MΩ range, and adjust P4 until the appropriate value is displayed.
AC Volts 2V Range	5. Apply a known 1.995V_{rms} sinewave signal to the DMM and adjust P5 until the display reads the same.

PC BOARD LAYOUT

It is imperative to have only one, single-point, analog signal ground connection for the entire system. In a multi-ground layout, the presence of ground-loop resistances will cause the op amps' offset currents and AC response to have a devastating effect on system gain, linearity, and display LSD flicker. Similar precautions must also be taken in the layout of the analog and high-switching-current (digital) paths of the ADD3501.

A FINAL NOTE

The digital multimeter described in this note was developed with the goals of accuracy and low cost. For the high-end DMM market segments, however, improvements to the basic circuit of *Figure 1* are possible in the following areas:

1. Expand the VOLTS mode to include a 200 mV full-scale range;
2. Decrease the full-scale current-measurement loading voltage from 2V to 200 mV; and,
3. Provide a true-rms measurement capability.
4. Increase resolution by substituting the ADD3701—3 3/4-digit DVM chip—which is interchangeable and provides a maximum display count of 3.999.

The first 2 improvements involve a dividing down of the ADD3501 feedback loop by a ratio of 10:1, which reduces the 2V full-scale input requirement to 200 mV. This not only allows a 200 mV signal between the ADD3501's V_{IN+} and V_{IN-} inputs to display a full-scale reading, but implies that the maximum voltage dropped across the current-measuring-mode resistance also will be 200 mV. Note, though, that the values of the current-measurement resistors must be scaled down by a factor of ten.

Additionally, a 200 mV full-scale input implies a resolution of 100 μV/LSD. At such low input levels, the DMM may require some clever circuitry to eliminate the gain and linearity distortions that can arise from the offset currents in the AC-to-DC converter.

The third possible improvement—the reading of true-rms values—can be implemented by replacing the AC-to-DC converter of *Figure 2* with National's LH0091, a true-rms-to-DC converter, and appropriate interface circuitry.

REFERENCES:

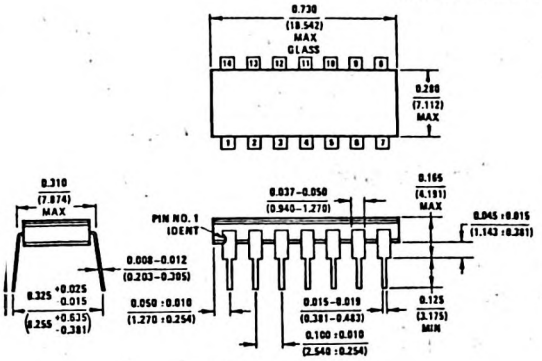
1. ADD3501 Data Sheet.
2. LH0091 Data Sheet.
3. LM336 Data Sheet.
4. Application Note AN-20.
5. ADD3701 Data Sheet.

Section 15

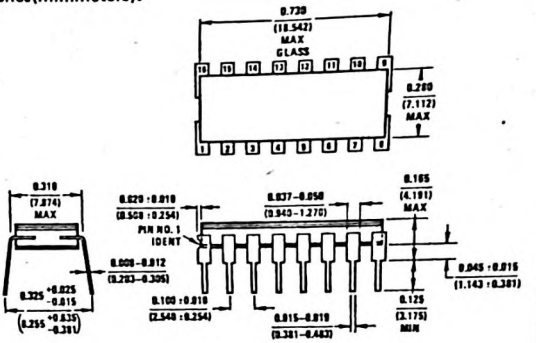
Physical Dimensions

15

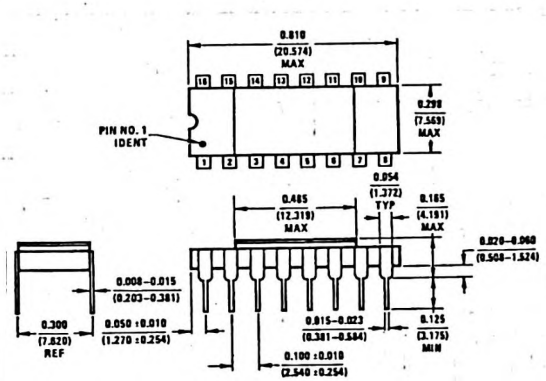
All dimensions in inches(millimeters).



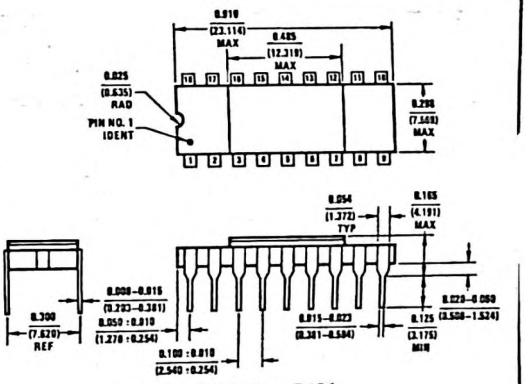
NS Package D14A
14-Lead Cavity DIP (D)



NS Package D16A
16-Lead Cavity DIP (D)



NS Package D16C
16-Lead Cavity DIP (D)
(Side Brazed)



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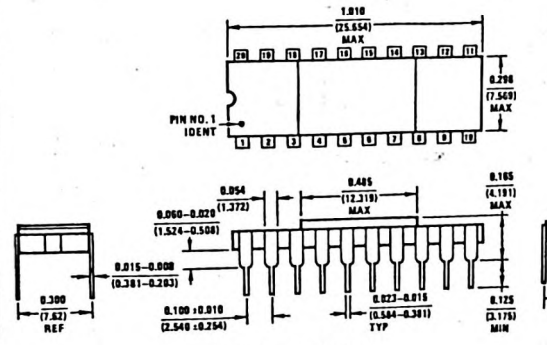

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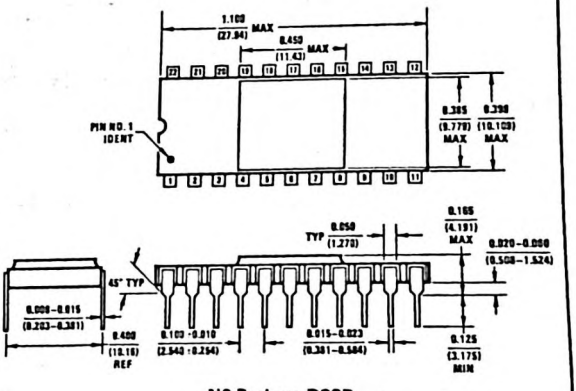

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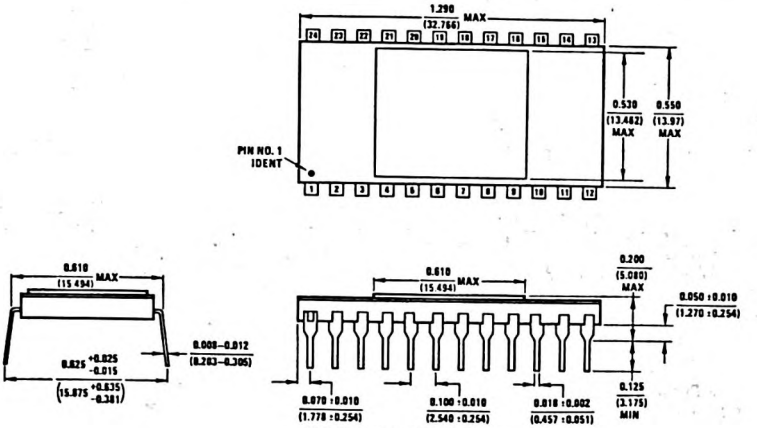
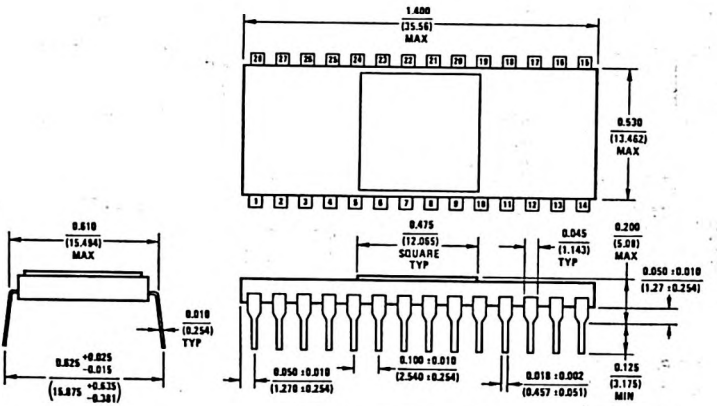


NS Package D24A
24-Lead Cavity DIP (D)



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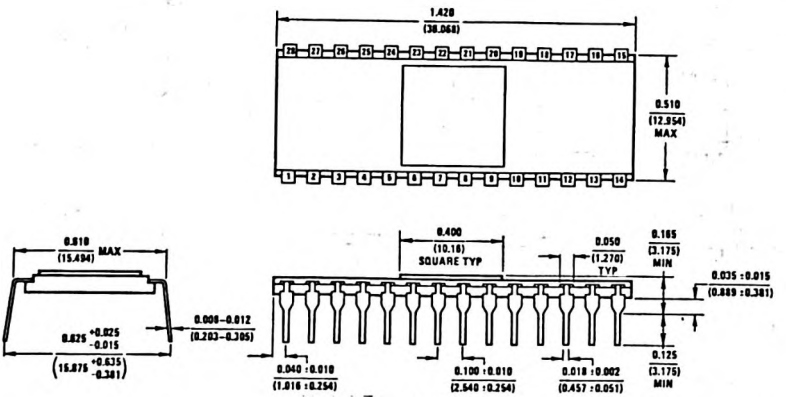

NS Package D28D
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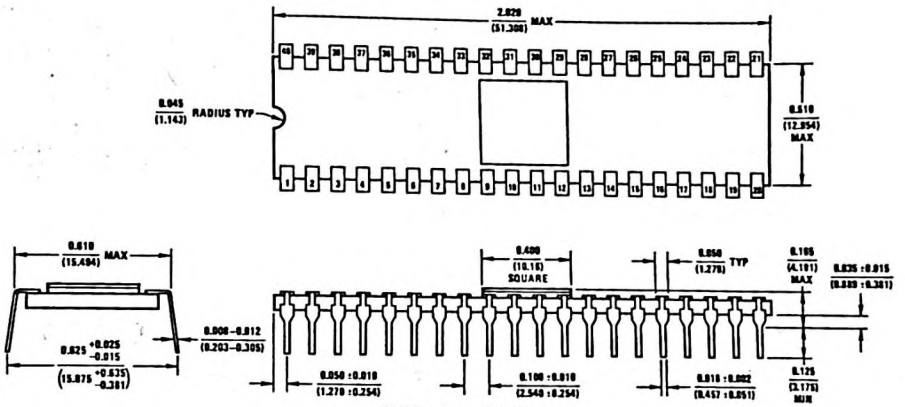

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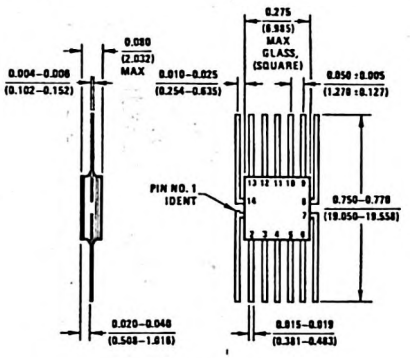
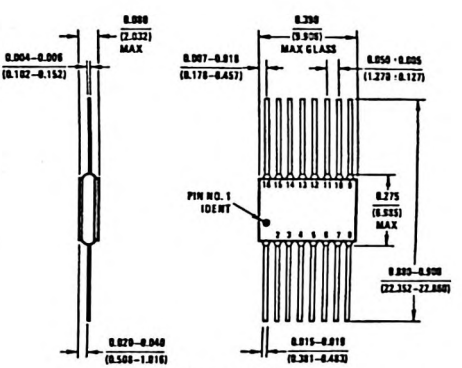


NS Package F14A
14-Lead Flat Package (F)



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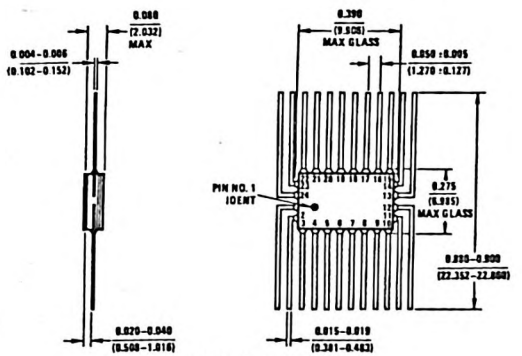

NS Package F24A
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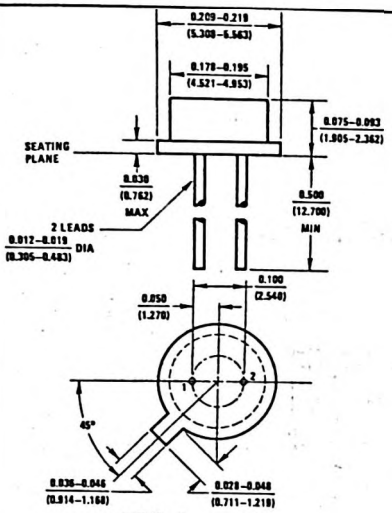

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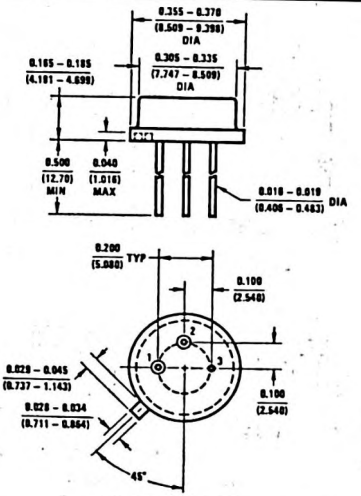
2-Lead TO-46 Metal Can Package (H)



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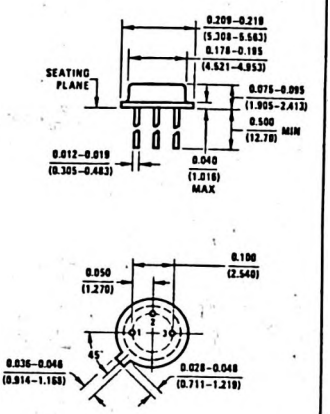

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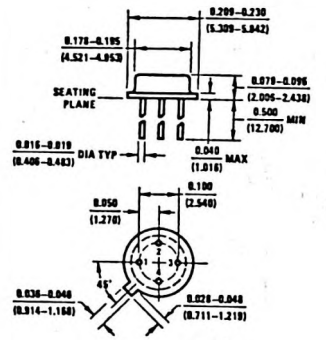

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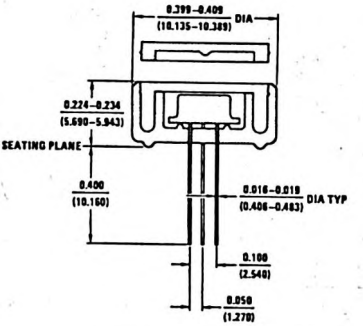
4-Lead TO-46 Metal Can Package (H)



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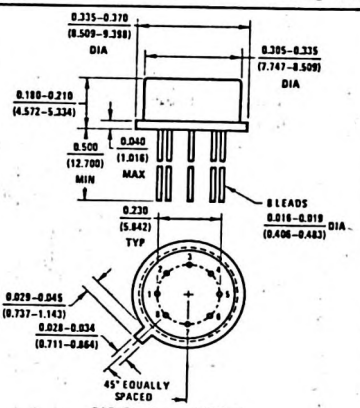
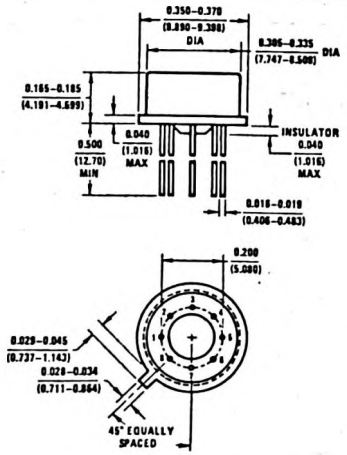
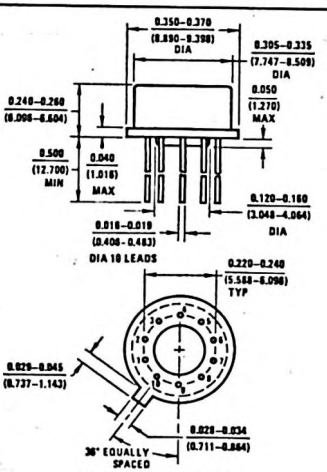
Thermal Shield for H04A



NS Package H08B
8-Lead TO-5 Metal Can Package (H)



NS Package H08C
8-Lead TO-5 Metal Can Package (H)



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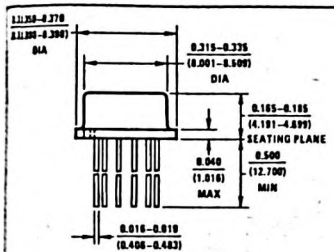
10-Lead TO-5 Metal Can Package (H) (High Profile)



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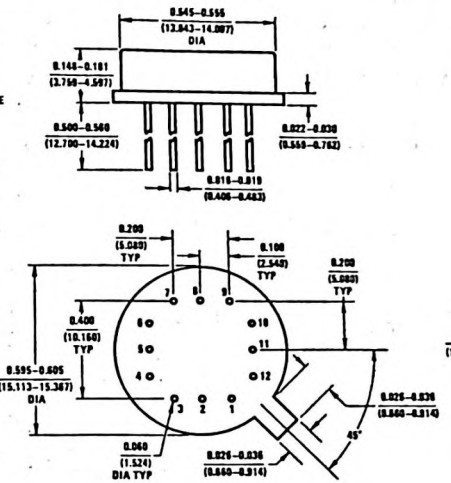
122-Lead TO-8 Metal Can Package (H)



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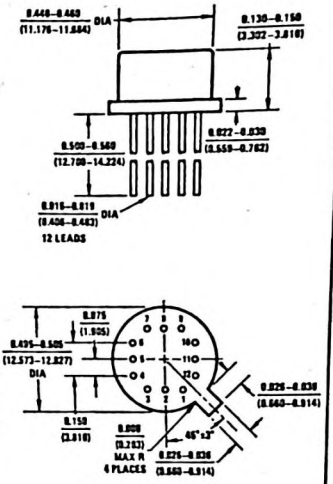

NS Package H12C
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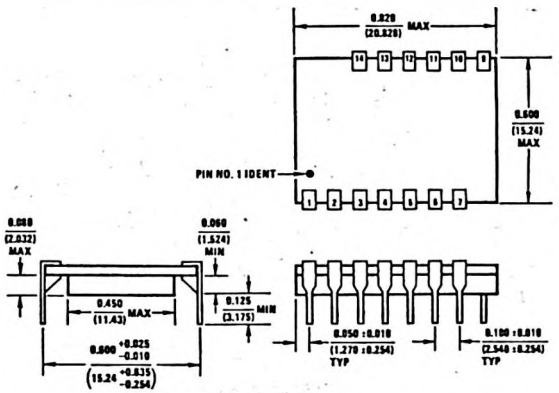

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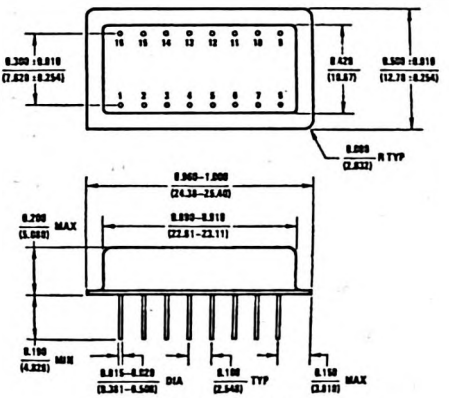

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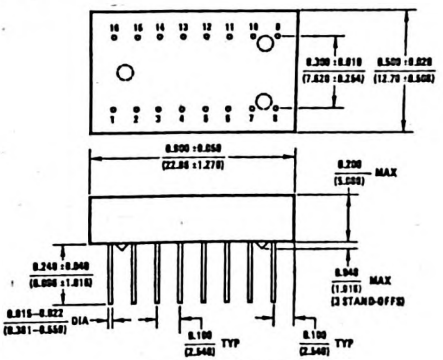

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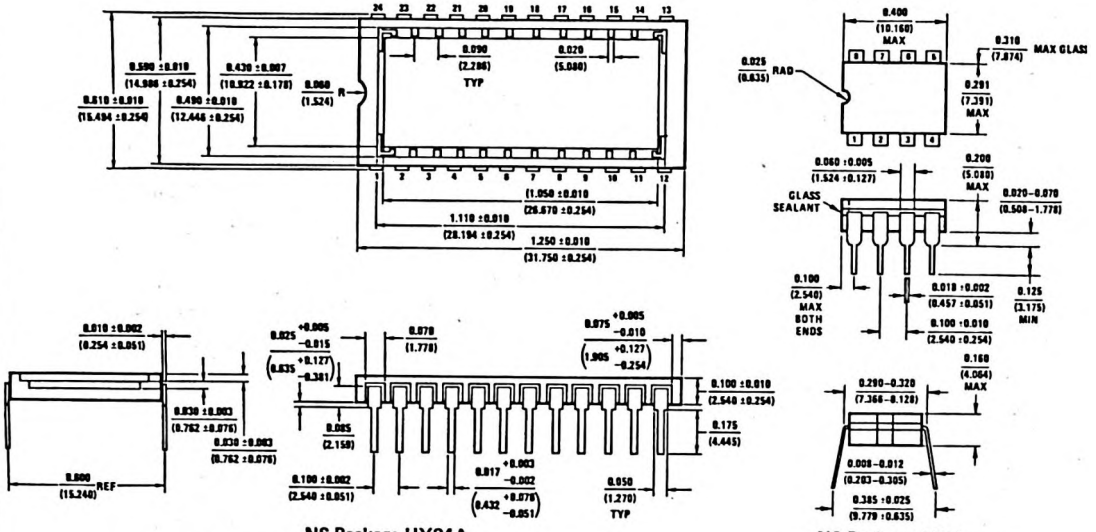
16-Lead DIP (J) (Hybrid)



NS Package HY24A
24-Lead Epoxy/Ceramic Package (J) (Hybrid)

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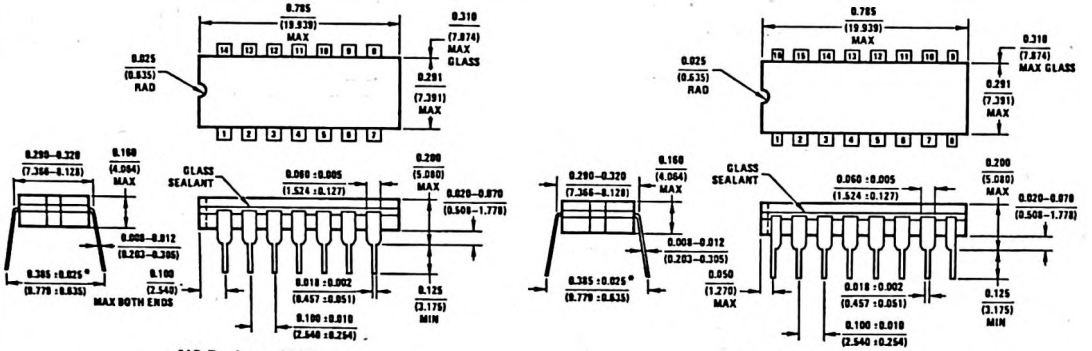
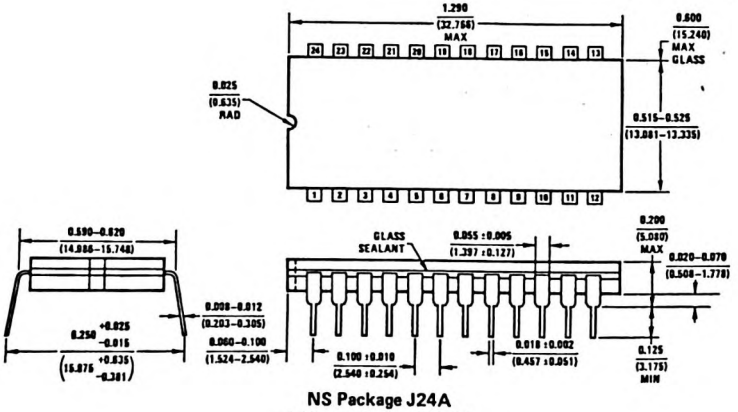
8-Lead Cavity DIP (J)



NS Package J14A
14-Lead Cavity DIP (J)

NS Package J16A
16-Lead Cavity DIP (J)



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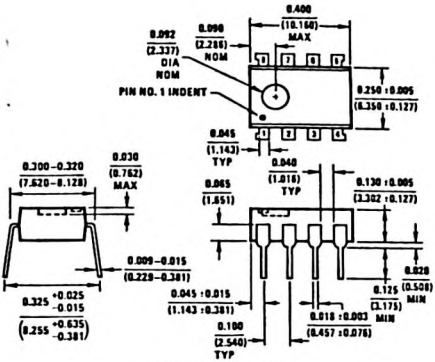

NS Package N08A
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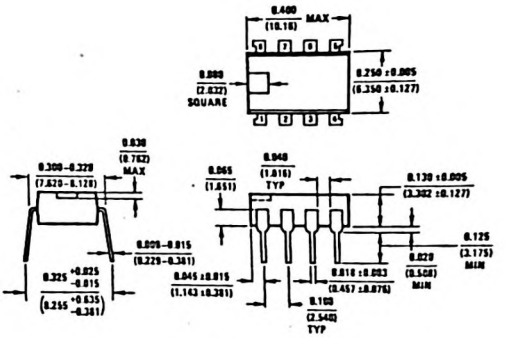

NS Package N08B
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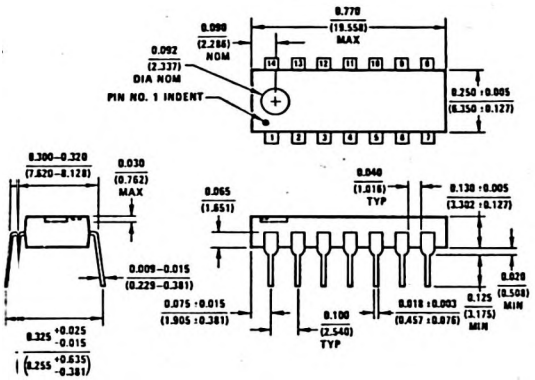

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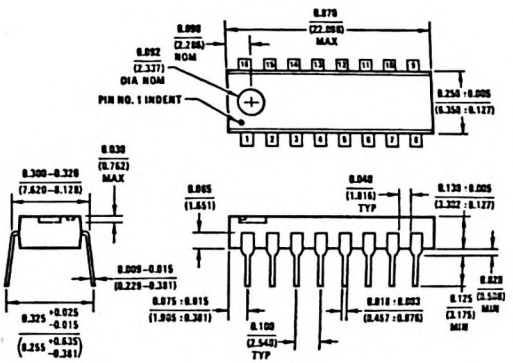

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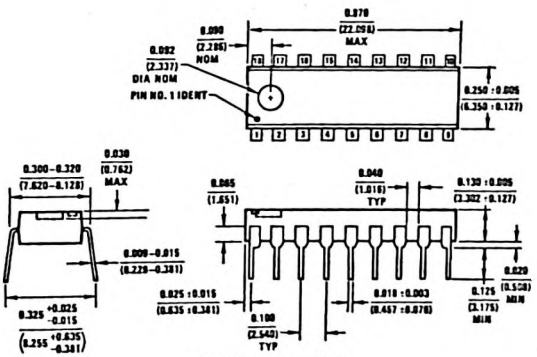

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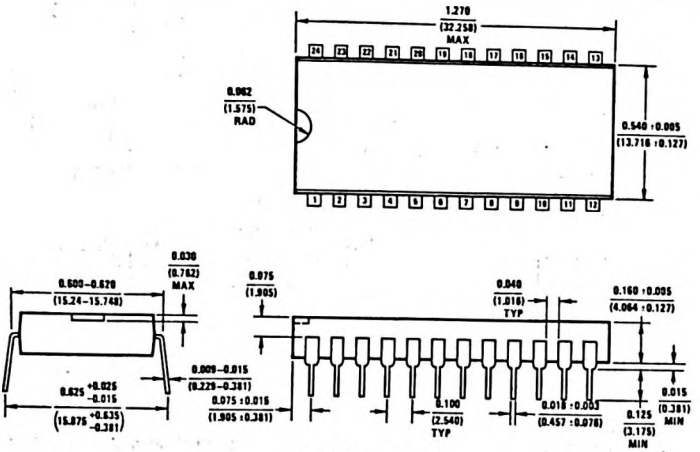

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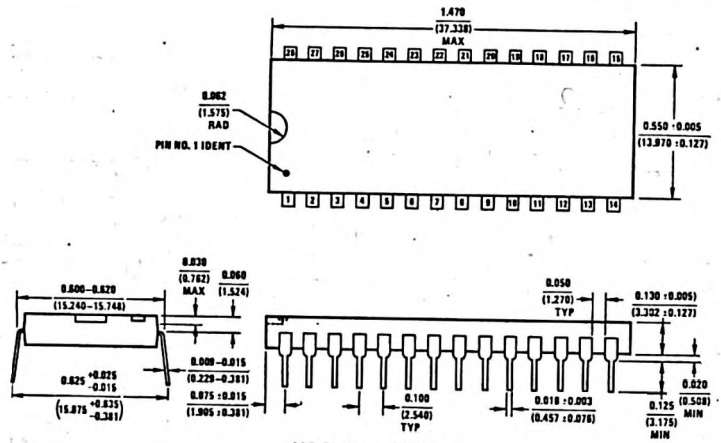

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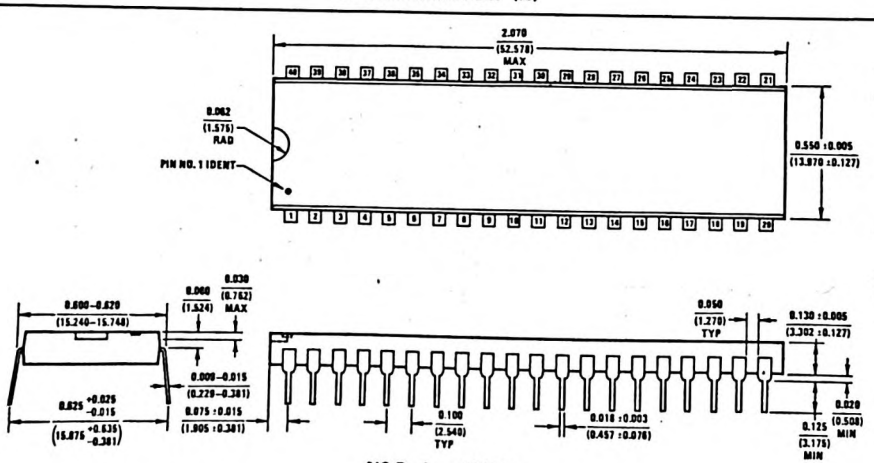

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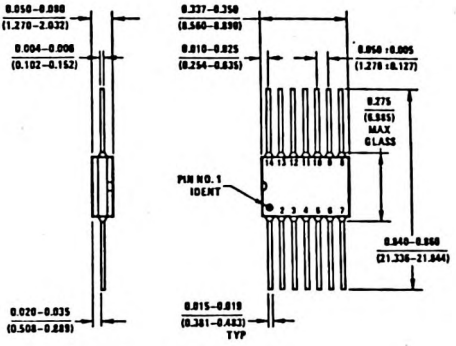

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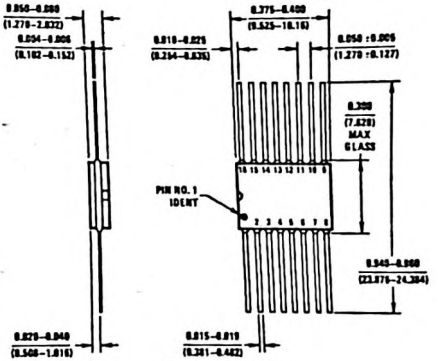
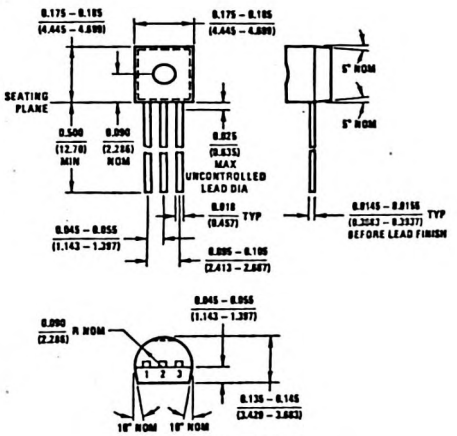


NS Package W16A
16-Lead Flat Package (W)



NS Package Z03A
3-Lead TO-92 Plastic Package (Z)

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